1. General description

Extremely low capacitance bidirectional ElectroStatic Discharge (ESD) protection diode, part of the TrEOS protection family. This device is housed in a DSN0603-2 (SOD962-2) leadless ultra small Surface-Mounted Device (SMD) package designed to protect one signal line from the damage caused by ESD and other transients.

2. Features and benefits

- Bidirectional ESD protection of one line
- Extremely low trigger-voltage $V_{t1}$ of 4.3 V TLP
- Extremely low diode capacitance $C_d = 0.69 \text{ pF}$
- Extremely low clamping voltage to protect sensitive I/Os
- Extremely low-inductance protection path to ground
- ESD protection up to ±20 kV according to IEC 61000-4-2
- Ultra small SMD package

3. Applications

- USB 3.2 and Universal Flash Storage (UFS) data lines
- Cellular handsets and accessories
- Portable electronics
- Communication systems
- Computers and peripherals

4. Quick reference data

| Table 1. Quick reference data | | | | | |
|---|---|---|---|---|
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
| $V_{RWM}$ | reverse standoff voltage | - | - | 2 | V |
| $C_d$ | diode capacitance | $f = 1 \text{ MHz}; V_R = 1 \text{ V}; T_{amb} = 25 \text{ °C}$ | - | 0.69 | 0.83 | pF |
5. Pinning information

Table 2. Pinning information

<table>
<thead>
<tr>
<th>Pin</th>
<th>Symbol</th>
<th>Description</th>
<th>Simplified outline</th>
<th>Graphic symbol</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>K1</td>
<td>cathode (diode 1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>K2</td>
<td>cathode (diode 2)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

6. Ordering information

Table 3. Ordering information

<table>
<thead>
<tr>
<th>Type number</th>
<th>Package</th>
<th>Name</th>
<th>Description</th>
<th>Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>PESD2V0Y1BSF</td>
<td>DSN0603-2</td>
<td>silicon, leadless ultra small package; 2 terminals; 0.4 mm pitch; 0.6 mm x 0.3 mm x 0.3 mm body</td>
<td>SOD962-2</td>
<td></td>
</tr>
</tbody>
</table>

7. Marking

Table 4. Marking codes

<table>
<thead>
<tr>
<th>Type number</th>
<th>Marking code</th>
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<tbody>
<tr>
<td>PESD2V0Y1BSF</td>
<td>C6</td>
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</table>

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_RWM</td>
<td>reverse standoff voltage</td>
<td></td>
<td>-</td>
<td>2</td>
<td>V</td>
</tr>
<tr>
<td>I_{PPM}</td>
<td>rated peak pulse current</td>
<td>t_p = 8/20 µs</td>
<td>-</td>
<td>6</td>
<td>A</td>
</tr>
<tr>
<td>T_{amb}</td>
<td>ambient temperature</td>
<td></td>
<td>-40</td>
<td>125</td>
<td>°C</td>
</tr>
<tr>
<td>T_{stg}</td>
<td>storage temperature</td>
<td></td>
<td>-65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

ESD maximum ratings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{ESD}</td>
<td>electrostatic discharge</td>
<td>IEC 61000-4-2; contact discharge</td>
<td>[3]</td>
<td>-20</td>
<td>20</td>
</tr>
<tr>
<td></td>
<td>voltage</td>
<td>IEC 61000-4-2; air discharge</td>
<td>[3]</td>
<td>-20</td>
<td>20</td>
</tr>
</tbody>
</table>

[1] Device stressed with 8/20 µs exponential decay waveform according to IEC 61000-4-5.
[2] In positive and negative direction.
Extremely low capacitance bidirectional ESD protection diode

9. Characteristics

Table 6. Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{BR}</td>
<td>breakdown voltage</td>
<td>I_{R} = 1 mA; T_{amb} = 25 °C</td>
<td>-</td>
<td>3.3</td>
<td>3.6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>I_{RM}</td>
<td>reverse leakage current</td>
<td>V_{RWM} = 2 V; T_{amb} = 25 °C</td>
<td>-</td>
<td>1</td>
<td>50</td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>C_{d}</td>
<td>diode capacitance</td>
<td>f = 1 MHz; V_{R} = 1 V; T_{amb} = 25 °C</td>
<td>-</td>
<td>0.69</td>
<td>0.83</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>V_{CL}</td>
<td>clamping voltage</td>
<td>I_{PPM} = 6 A; T_{amb} = 25 °C</td>
<td>[1]</td>
<td>-</td>
<td>3</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>R_{dyn}</td>
<td>dynamic resistance</td>
<td>I_{R} = 10 A; T_{amb} = 25 °C</td>
<td>[2]</td>
<td>0.2</td>
<td>-</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>I_{R} = -10 A; T_{amb} = 25 °C</td>
<td>[2]</td>
<td>0.2</td>
<td>-</td>
<td>Ω</td>
<td></td>
</tr>
</tbody>
</table>

[1] Device stressed with 8/20 µs exponential decay waveform according to IEC 61000-4-5.
Fig. 3. Insertion loss; typical values

\[ a = \frac{C_d}{C_d(V_{RWM} = 0 \, V)} \]

Fig. 4. Relative capacitance as a function of input voltage; typical values

Fig. 5. Differential Time Domain Reflectometer (TDR) plot; typical values
Fig. 6. USB 3.2 eye diagram, PCB with device; typical values

Fig. 7. USB 3.2 eye diagram, PCB without device; typical values
Extremely low capacitance bidirectional ESD protection diode

Fig. 8. USB 3.2 eye diagram, PCB with device; typical values

Fig. 9. USB 3.2 eye diagram, PCB without device; typical values
Fig. 10. Universal Flash Storage (UFS) eye diagram, PCB with device; typical values

Fig. 11. Universal Flash Storage (UFS) eye diagram, PCB without device; typical values
Extremely low capacitance bidirectional ESD protection diode

**Fig. 12.** Dynamic resistance with positive clamping; typical values

\[ I_{pp} \text{ (A)} \]

\[ V_{CL} \text{ (V)} \]

\[ t_r = 1 \text{ ns} \]
\[ t_p = 100 \text{ ns}; \text{ Transmission Line Pulse (TLP)} \]

**Fig. 13.** Dynamic resistance with negative clamping; typical values

\[ I_{pp} \text{ (A)} \]

\[ V_{CL} \text{ (V)} \]

\[ t_r = 1 \text{ ns} \]
\[ t_p = 100 \text{ ns}; \text{ Transmission Line Pulse (TLP)} \]

**Fig. 14.** Dynamic resistance with positive clamping; typical values

\[ I_{pp} \text{ (A)} \]

\[ V_{CL} \text{ (V)} \]

\[ t_r = 600 \text{ ps} \]
\[ t_p = 5 \text{ ns}; \text{ Transmission Line Pulse (TLP)} \]

**Fig. 15.** Dynamic resistance with negative clamping; typical values

\[ I_{pp} \text{ (A)} \]

\[ V_{CL} \text{ (V)} \]

\[ t_r = 600 \text{ ps} \]
\[ t_p = 5 \text{ ns}; \text{ Transmission Line Pulse (TLP)} \]
Extreme low capacitance bidirectional ESD protection diode

**Fig. 16.** Dynamic resistance with positive clamping; typical values

IEC 61000-4-5; \( t_p = 8/20 \) µs; positive pulse

**Fig. 17.** Dynamic resistance with negative clamping; typical values

IEC 61000-4-5; \( t_p = 8/20 \) µs; negative pulse

**Fig. 18.** TLP voltage and current over time, typical values

\( t_r = 1 \) ns  
(1) TLP current  
(2) TLP voltage
10. Application information

The device is designed for the protection of one bidirectional data line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both positive and negative with respect to ground.

The device uses an advanced clamping structure showing a negative dynamic resistance. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).

---

Fig. 19. Application diagram

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.
11. Package outline

Leadless ultra small package; 2 terminals; body 0.6 x 0.3 x 0.3 mm  

Dimensions (mm are the original dimensions)

<table>
<thead>
<tr>
<th>Unit</th>
<th>A</th>
<th>A₁</th>
<th>b</th>
<th>D</th>
<th>E</th>
<th>e₁</th>
<th>L</th>
</tr>
</thead>
<tbody>
<tr>
<td>mm max</td>
<td>0.32</td>
<td>0.03</td>
<td>0.25</td>
<td>0.325</td>
<td>0.625</td>
<td>0.15</td>
<td></td>
</tr>
<tr>
<td>mm nom</td>
<td>0.28</td>
<td>0.23</td>
<td>0.275</td>
<td>0.575</td>
<td>0.4</td>
<td>0.13</td>
<td></td>
</tr>
</tbody>
</table>

Note 1. The marking bar indicates the cathode.

Fig. 20. Package outline DSN0603-2 (SOD962-2)
12. Soldering

Footprint information for reflow soldering of leadless ultra small package; 2 terminals

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Fig. 21. Reflow soldering footprint for DSN0603-2 (SOD962-2)
## 13. Revision history

### Table 7. Revision history

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<tr>
<th>Data sheet ID</th>
<th>Release date</th>
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<th>Change notice</th>
<th>Supersedes</th>
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<td>PESD2V0Y1BSF v.3</td>
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<td></td>
<td></td>
<td>- Table &quot;Characteristics&quot;: updated ( C_d )</td>
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<td></td>
<td></td>
<td>- Updated Package outline drawing</td>
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14. Legal information

Data sheet status

<table>
<thead>
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<th>Document status</th>
<th>Product status</th>
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<td>Preliminary</td>
<td>Qualification</td>
<td>This document contains data from the preliminary specification.</td>
</tr>
<tr>
<td>Objective</td>
<td>Development</td>
<td>This document contains data from the objective specification for product development.</td>
</tr>
<tr>
<td>Product</td>
<td>Production</td>
<td>This document contains the product specification.</td>
</tr>
</tbody>
</table>

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