



PESD2IVN24T-Q

ESD protection for In-vehicle networks

19 November 2025

Product data sheet

1. General description

ESD protection device in a small SOT23 Surface-Mounted Device (SMD) plastic package, designed to protect two automotive In-vehicle network bus lines from the damage caused by ElectroStatic discharge (ESD) and other transients.

2. Features and benefits

- Reverse stand-off voltage: $V_{RWM} = 24\text{ V}$
- Low clamping voltage: $V_{CL} = 33\text{ V}$ at $I_{PPM} = 3.5\text{ A}$
- Typ. diode capacitance matching: $\Delta C_d/C_d = 0.1\%$
- ESD protection up to 30 kV (IEC 61000-4-2)
- ESD protection up to 30 kV (ISO 10605; $C = 330\text{ pF}$, $R = 330\ \Omega$)
- ISO 7637-3: Pulse a: $V_S = -150\text{ V}$ / Pulse b: $V_S = +100\text{ V}$
- Ultra low leakage current: $I_{RM} = 1\text{ nA}$
- Qualified according to AEC-Q101 and recommended for use in automotive applications

3. Applications

ESD protection for In-vehicle network lines in automotive environments

- CAN
- LIN
- FlexRay
- SENT

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	$T_{amb} = 25\text{ }^\circ\text{C}$		-	-	24	V
I_{PPM}	rated peak pulse current	$t_p = 8/20\ \mu\text{s}$	[1] [2]	-	-	3.5	A
V_{CL}	clamping voltage	$I_{PPM} = 3.5\text{ A}$; $t_p = 8/20\ \mu\text{s}$; $T_{amb} = 25\text{ }^\circ\text{C}$	[3] [2]	-	33	42	V

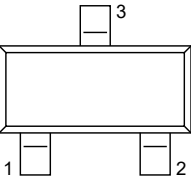
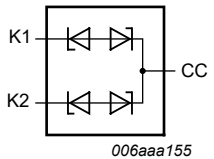
[1] According to IEC 61000-4-5.

[2] Measured from pin 1 or 2 to pin 3.

[3] Device stressed with 8/20 μs exponential decay waveform according to IEC 61000-4-5.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode (diode 1)	 <p style="text-align: center;">SOT23</p>	 <p style="text-align: center;"><small>006aaa155</small></p>
2	K2	cathode (diode 2)		
3	K	common cathode		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD2IVN24T-Q	SOT23	plastic, surface-mounted package; 3 terminals; 1.9 mm pitch; 2.9 mm x 1.3 mm x 1 mm body	SOT23

7. Marking

Table 4. Marking codes

Type number	Marking code ^[1]
PESD2IVN24T-Q	BV%

[1] % = placeholder for manufacturing site code

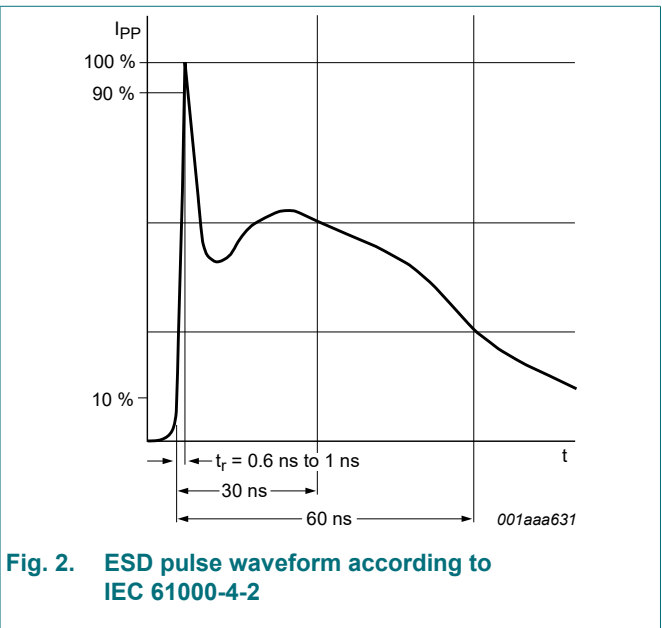
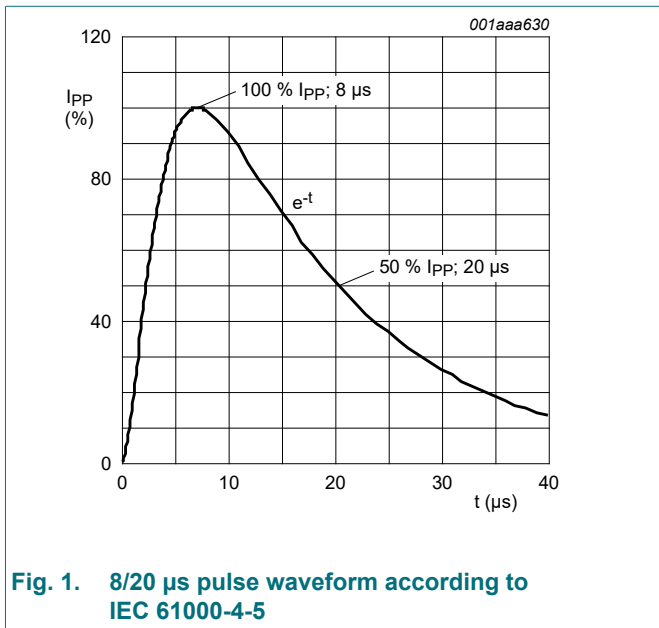
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
I_{PPM}	rated peak pulse current	$t_p = 8/20 \mu s$	[1] [2]	-	3.5	A
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
ESD maximum ratings						
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2; contact discharge	[2] [3]	-	30	kV
		ISO 10605; contact discharge; C = 330 pF, R = 330 Ω	[2] [3]	-	30	kV
		ISO 10605; contact discharge; C = 150 pF, R = 330 Ω	[2] [3]	-	30	kV

- [1] According to IEC 61000-4-5.
- [2] Measured from pin 1 or 2 to pin 3.
- [3] Device stressed with ten non-repetitive ESD pulses.



9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	$T_{amb} = 25\text{ }^{\circ}\text{C}$		-	-	24	V
V_{BR}	breakdown voltage	$I_R = 10\text{ mA}; T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	25.5	30.5	35.5	V
I_{RM}	reverse leakage current	$V_{RWM} = 24\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-	1	50	nA
C_d	diode capacitance	$f = 1\text{ MHz}; V_R = 0\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-	14	17	pF
$\Delta C_d/C_d$	diode capacitance matching	$f = 1\text{ MHz}; V_R = 2.5\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$	[2]	-	0.1	-	%
V_{CL}	clamping voltage	$I_{PPM} = 1\text{ A}; t_p = 8/20\text{ }\mu\text{s}; T_{amb} = 25\text{ }^{\circ}\text{C}$	[3] [1]	-	31	40	V
		$I_{PPM} = 3.5\text{ A}; t_p = 8/20\text{ }\mu\text{s}; T_{amb} = 25\text{ }^{\circ}\text{C}$	[3] [1]	-	33	42	V
		$I_{PP} = 16\text{ A}; t_p = \text{TLP}; T_{amb} = 25\text{ }^{\circ}\text{C}$	[4] [1]	-	32	-	V
R_{dyn}	dynamic resistance	$I_R = 10\text{ A}; T_{amb} = 25\text{ }^{\circ}\text{C}$	[4] [1]	-	0.2	-	Ω

- [1] Measured from pin 1 or 2 to pin 3.
- [2] ΔC_d is the difference of the capacitance measured between pin 1 and pin 3 and the capacitance measured between pin 2 and pin 3.
- [3] Device stressed with 8/20 μs exponential decay waveform according to IEC 61000-4-5.
- [4] Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008

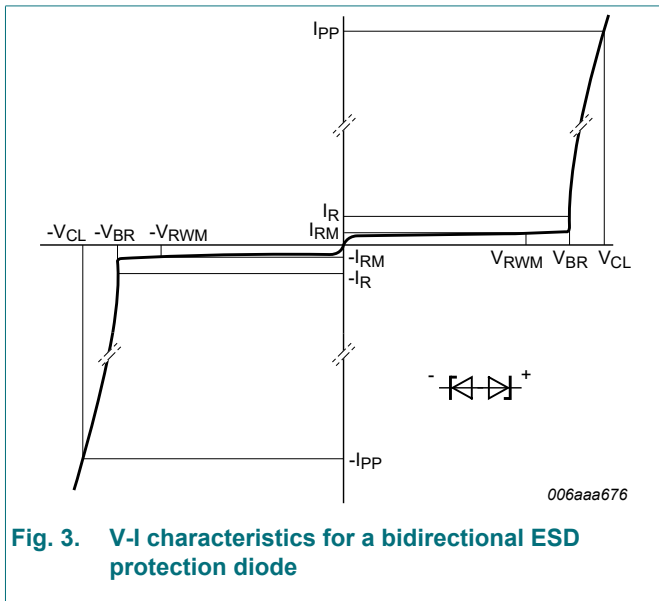


Fig. 3. V-I characteristics for a bidirectional ESD protection diode

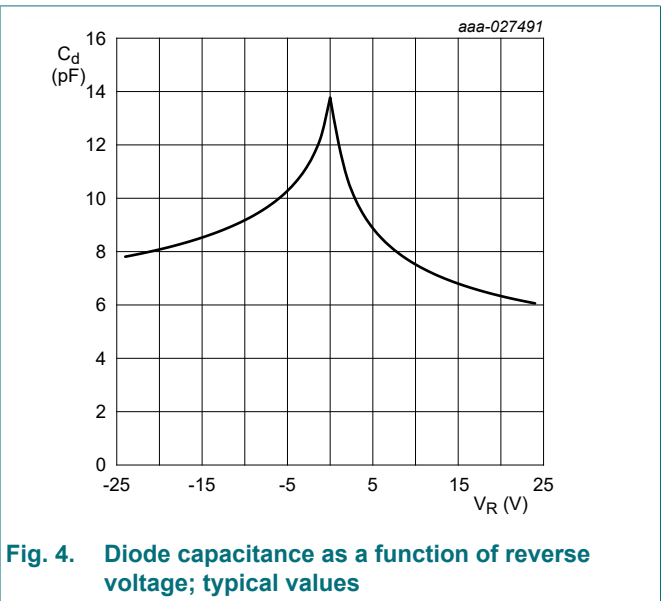


Fig. 4. Diode capacitance as a function of reverse voltage; typical values

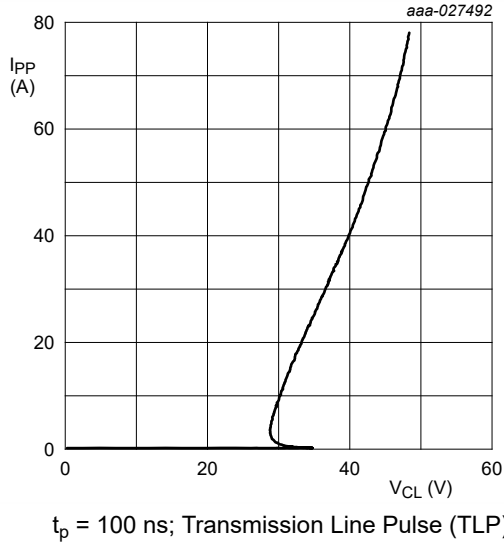


Fig. 5. Positive clamping voltage (TLP); typical values

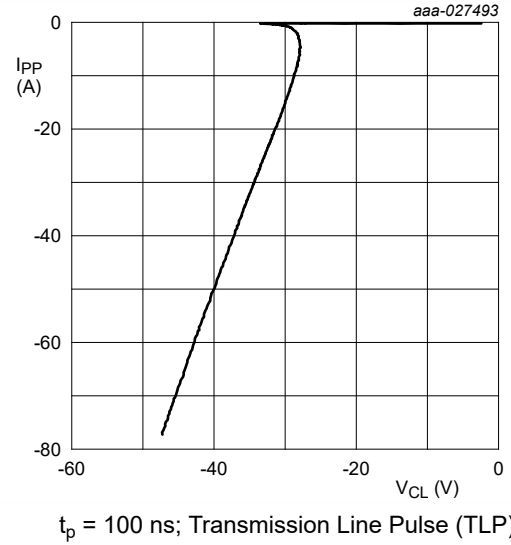


Fig. 6. Negative clamping voltage (TLP); typical values

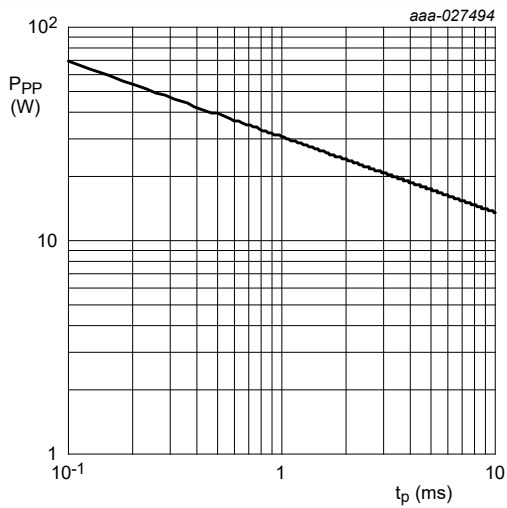


Fig. 7. Peak pulse power as a function of exponential pulse duration; typical values

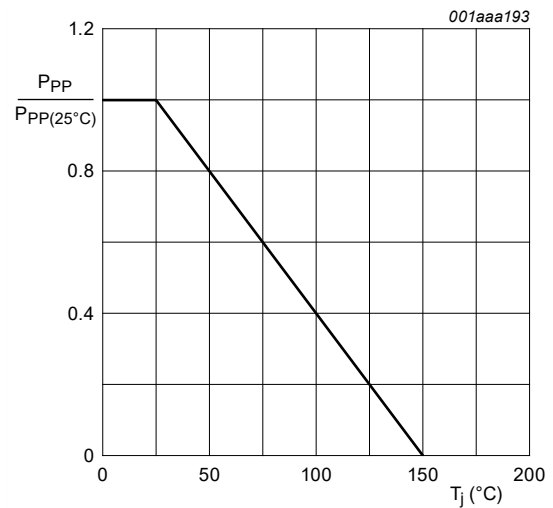


Fig. 8. Relative variation of peak pulse power as a function of junction temperature; typical values

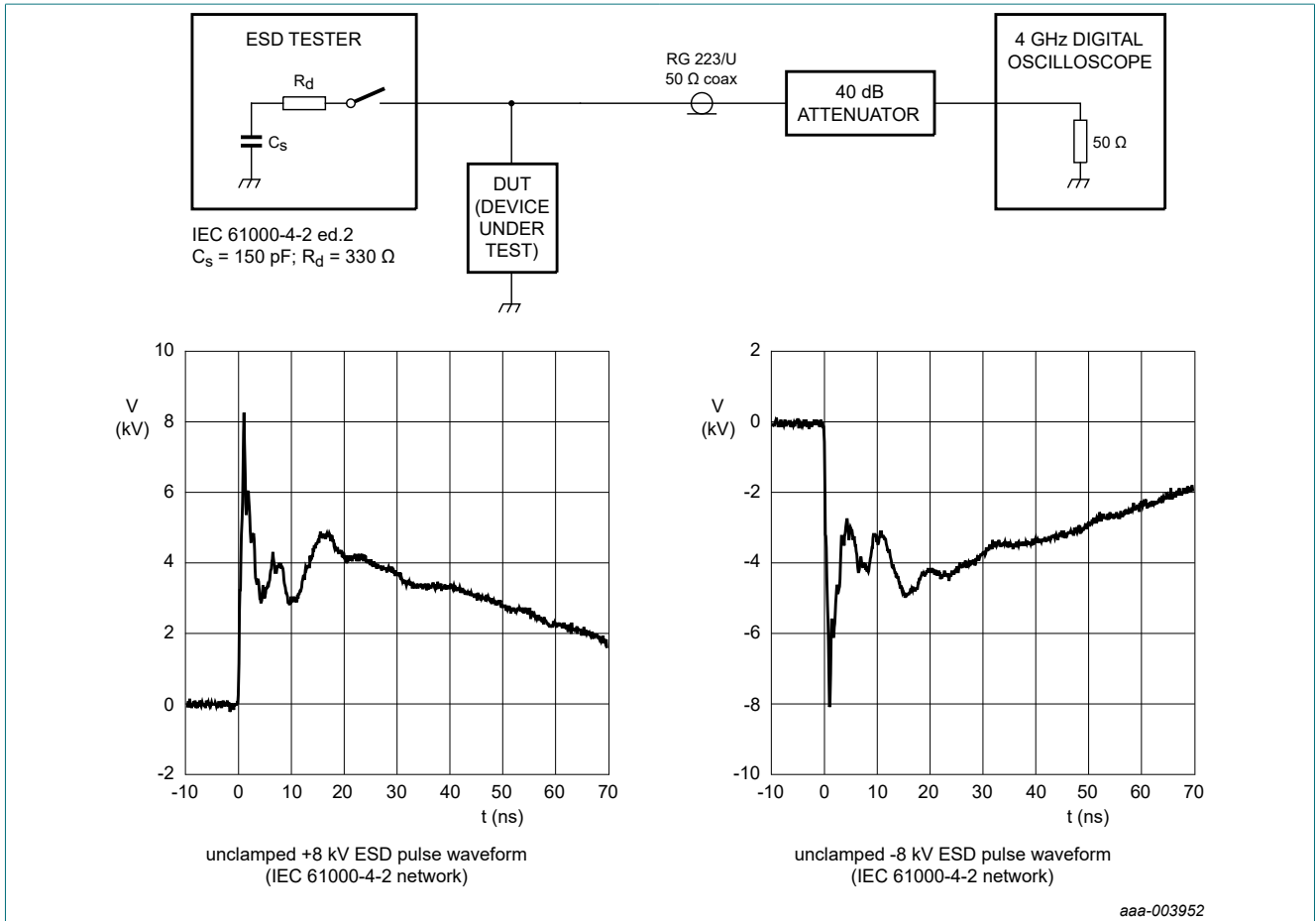


Fig. 9. ESD clamping test setup and waveforms

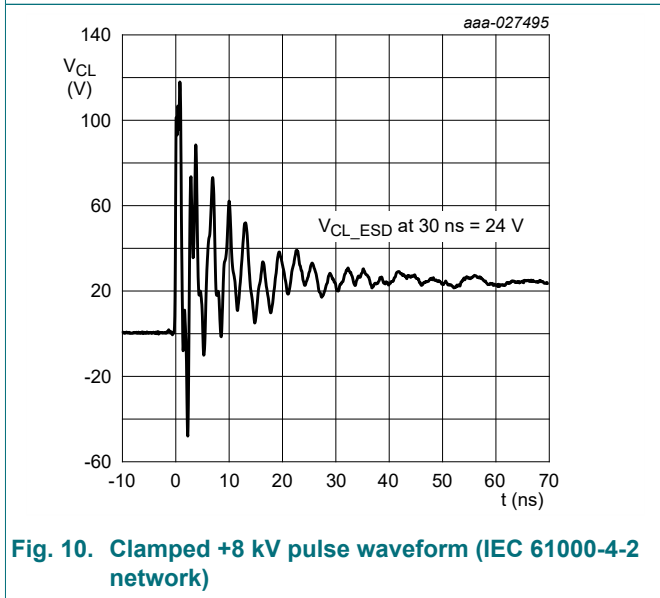


Fig. 10. Clamped +8 kV pulse waveform (IEC 61000-4-2 network)

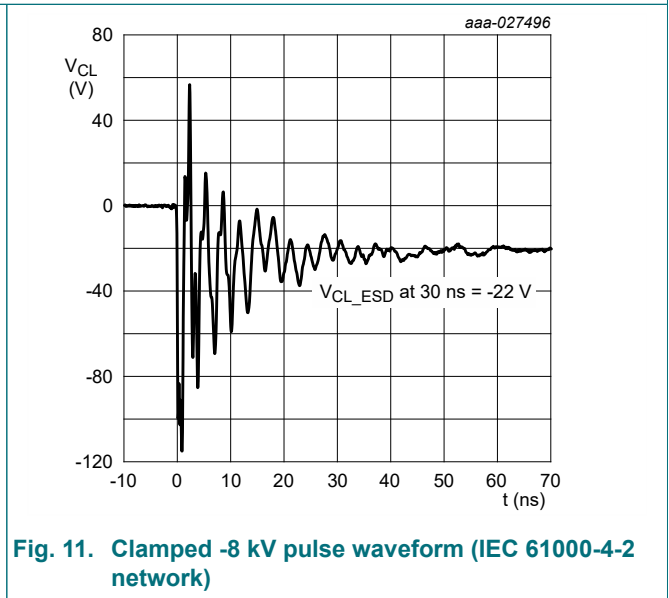


Fig. 11. Clamped -8 kV pulse waveform (IEC 61000-4-2 network)

10. Application information

The device is designed for the protection of two automotive IVN bus lines from the damage caused by ESD and surge pulses.

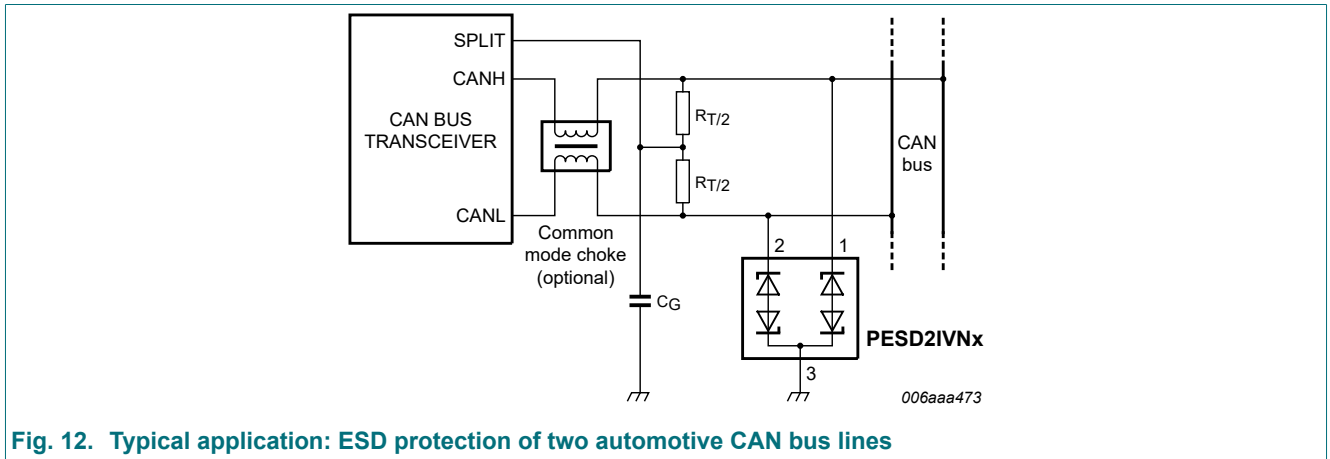


Fig. 12. Typical application: ESD protection of two automotive CAN bus lines

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

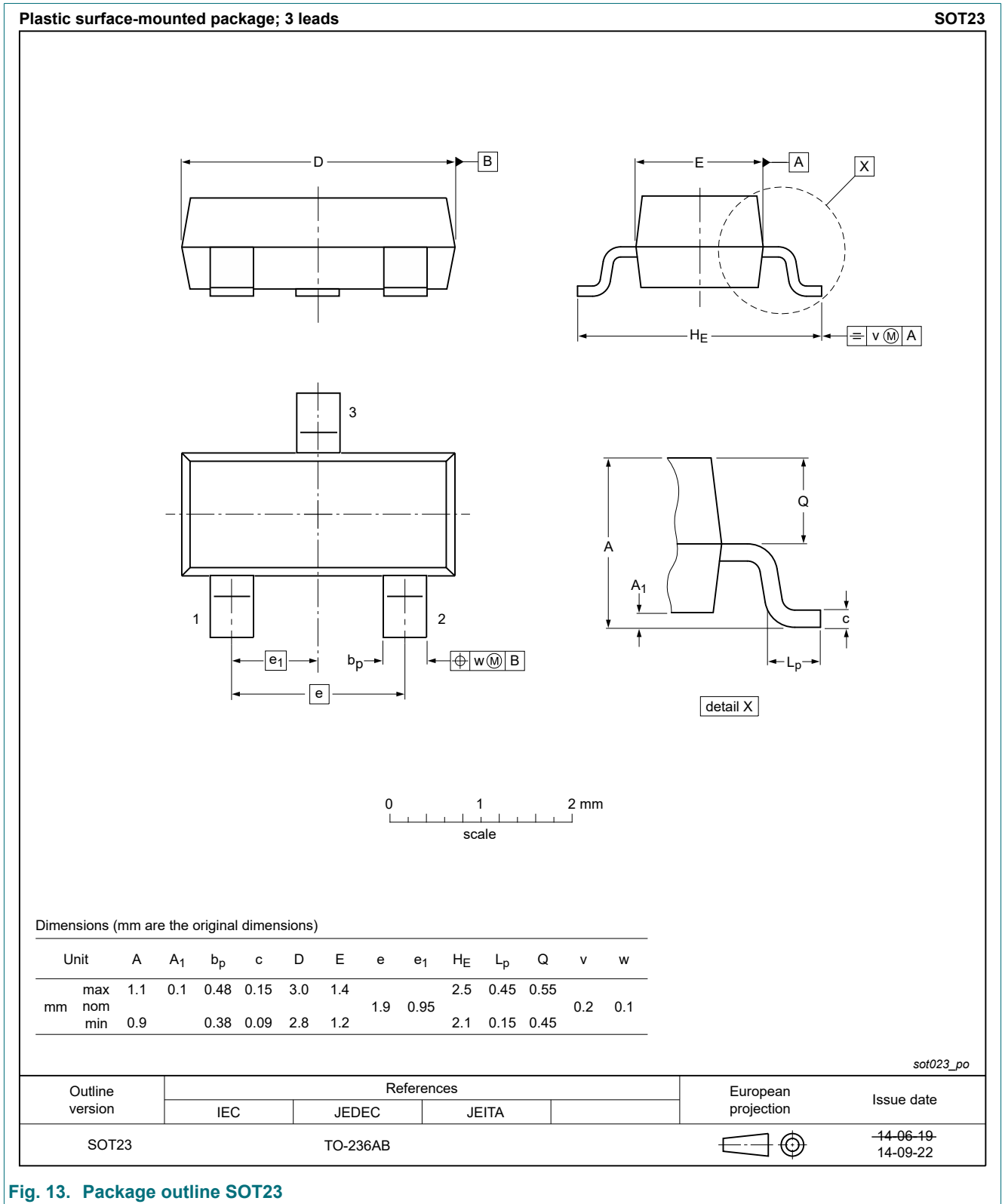


Fig. 13. Package outline SOT23

13. Soldering

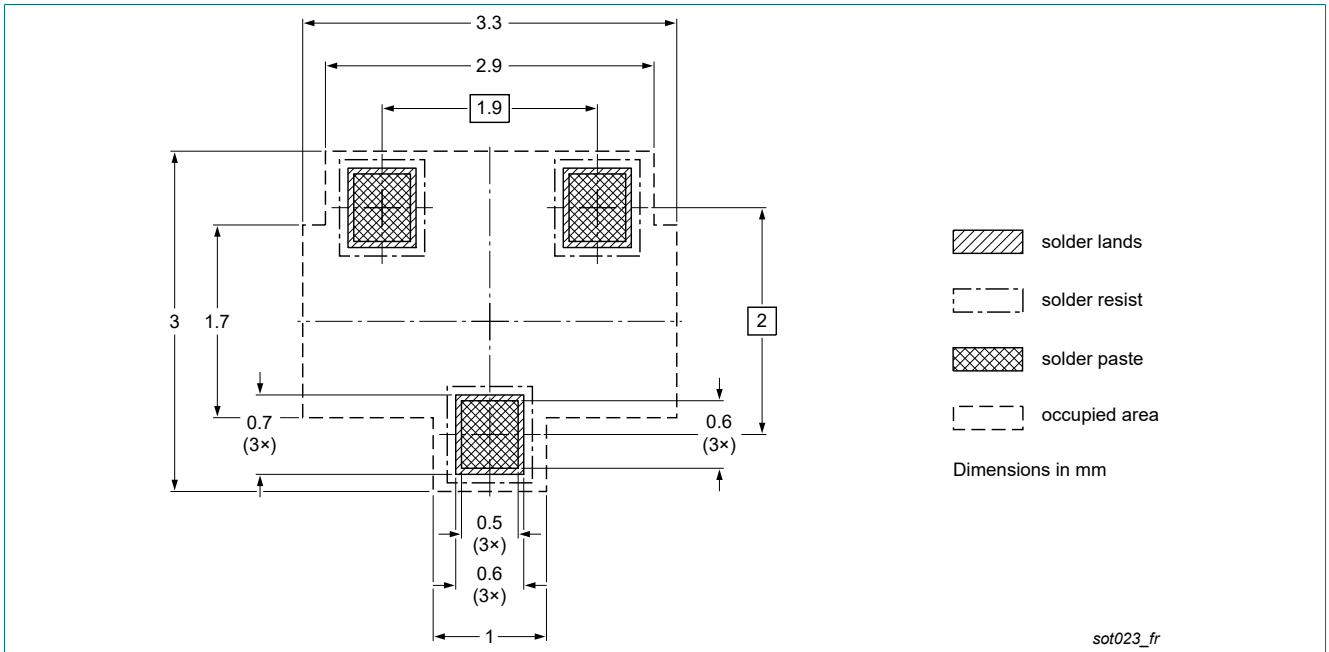


Fig. 14. Reflow soldering footprint for SOT23

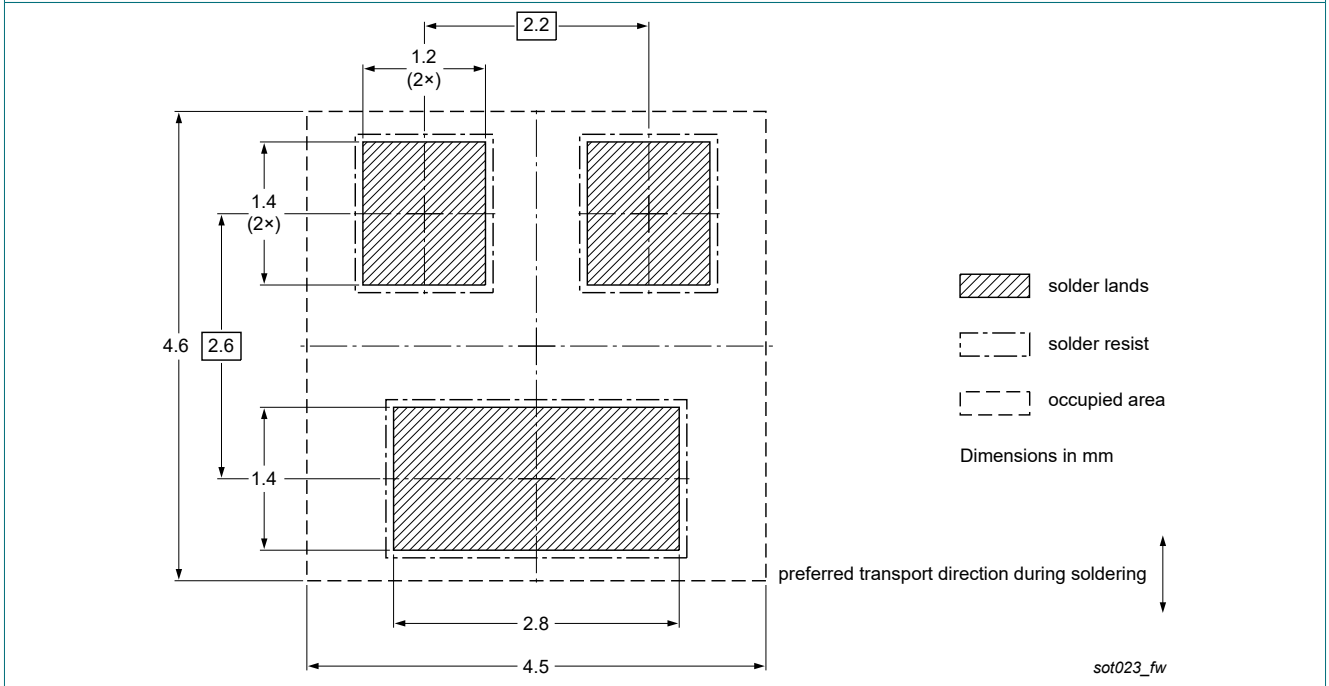


Fig. 15. Wave soldering footprint for SOT23

14. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD2IVN24T-Q v.2	20251119	Product data sheet	-	PESD2IVN24T-Q v.1
Modifications:	• Chapter "Characteristics": Update of Fig. 4 to 6			
PESD2IVN24T-Q v.1	20220704	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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