1. General description

Unidirectional ElectroStatic Discharge (ESD) protection diode designed to protect one signal line from the damage caused by ESD and other transients. The device is housed in a leadless ultra small DFN1006BD-2 (SOD882BD) Surface-Mounted Device (SMD) plastic package with side-wettable flanks (SWF).

2. Features and benefits

- ESD protection of one line
- Ultra small SMD plastic package
- Side wettable flanks
- Low clamping voltage: $V_{CL} = 23\ \text{V}$
- ESD protection up to 30 kV
- IEC 61000-4-2; level 4 (ESD)
- IEC 61000-4-5 (surge); $I_{pp} = 5\ \text{A}$
- Ultra low leakage current: $I_{RM} = 1\ \text{nA}$ typ.
- AEC-Q101 qualified

3. Applications

- Computers and peripherals
- Audio and video equipment
- Communication systems
- Portable electronics

4. Quick reference data

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{RWM}$</td>
<td>reverse standoff voltage</td>
<td>$T_{amb} = 25\ \text{°C}$</td>
<td>-</td>
<td>-</td>
<td>15</td>
<td>V</td>
</tr>
<tr>
<td>$C_d$</td>
<td>diode capacitance</td>
<td>$f = 1\ \text{MHz}; V_R = 0\ \text{V}; T_{amb} = 25\ \text{°C}$</td>
<td>-</td>
<td>32</td>
<td>70</td>
<td>pF</td>
</tr>
</tbody>
</table>
5. Pinning information

Table 2. Pinning information

<table>
<thead>
<tr>
<th>Pin</th>
<th>Symbol</th>
<th>Description</th>
<th>Simplified outline</th>
<th>Graphic symbol</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>K</td>
<td>cathode[1]</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>A</td>
<td>anode</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

[1] The marking bar indicates the cathode.

6. Ordering information

Table 3. Ordering information

<table>
<thead>
<tr>
<th>Type number</th>
<th>Package</th>
<th>Description</th>
<th>Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>PESD15VS1ULS</td>
<td>DFN1006BD-2</td>
<td>Leadless ultra small plastic package with side-wettable flanks (SWF); 2 terminals; 0.65 mm pitch; 1 mm x 0.6 mm x 0.47 mm body</td>
<td>SOD882BD</td>
</tr>
</tbody>
</table>

7. Marking

Table 4. Marking codes

<table>
<thead>
<tr>
<th>Type number</th>
<th>Marking code</th>
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<tbody>
<tr>
<td>PESD15VS1ULS</td>
<td>3V</td>
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</table>
### 8. Limiting values

Table 5. Limiting values

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>I_{PPM}</td>
<td>rated peak pulse current</td>
<td>$t_p = 8/20$ µs</td>
<td>[1]</td>
<td>-5A</td>
<td></td>
</tr>
<tr>
<td>$T_j$</td>
<td>junction temperature</td>
<td></td>
<td>-</td>
<td>150°C</td>
<td></td>
</tr>
<tr>
<td>$T_{amb}$</td>
<td>ambient temperature</td>
<td></td>
<td>-55°C</td>
<td>150°C</td>
<td></td>
</tr>
<tr>
<td>$T_{stg}$</td>
<td>storage temperature</td>
<td></td>
<td>-65°C</td>
<td>150°C</td>
<td></td>
</tr>
</tbody>
</table>

**ESD maximum ratings**

| $V_{ESD}$ | electrostatic discharge voltage | IEC 61000-4-2; contact discharge | [2] [3] | - | 30 kV |

[1] Non-repetitive current pulse 8/20 µs exponential decay waveform according to IEC61000-4-5.

---

Fig. 1. 8/20 µs pulse waveform according to IEC 61000-4-5

Fig. 2. ESD pulse waveform according to IEC 61000-4-2
9. Characteristics

Table 6. Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{RWM}$</td>
<td>reverse standoff voltage</td>
<td>$T_{amb} = 25 ^\circ C$</td>
<td>-</td>
<td>-</td>
<td>15</td>
<td>V</td>
</tr>
<tr>
<td>$V_{BR}$</td>
<td>breakdown voltage</td>
<td>$I_R = 5$ mA; $T_{amb} = 25 ^\circ C$</td>
<td>17.6</td>
<td>18</td>
<td>18.4</td>
<td>V</td>
</tr>
<tr>
<td>$I_{RM}$</td>
<td>reverse leakage current</td>
<td>$V_{RWM} = 15$ V; $T_{amb} = 25 ^\circ C$</td>
<td>-</td>
<td>1</td>
<td>50</td>
<td>nA</td>
</tr>
<tr>
<td>$C_d$</td>
<td>diode capacitance</td>
<td>$f = 1$ MHz; $V_R = 0$ V; $T_{amb} = 25 ^\circ C$</td>
<td>-</td>
<td>32</td>
<td>70</td>
<td>pF</td>
</tr>
<tr>
<td>$V_{CL}$</td>
<td>clamping voltage</td>
<td>$I_{PP} = 1$ A; $T_{amb} = 25 ^\circ C$</td>
<td>[1] [2]</td>
<td>-</td>
<td>-</td>
<td>23</td>
</tr>
<tr>
<td>$R_{dyn}$</td>
<td>dynamic resistance</td>
<td>$I_R = 10$ A; $T_{amb} = 25 ^\circ C$</td>
<td>[3]</td>
<td>-</td>
<td>0.6</td>
<td>Ω</td>
</tr>
</tbody>
</table>

[1] Non-repetitive current pulse 8/20 µs exponential decay waveform according to IEC61000-4-5.
[3] Non-repetitive current pulse, Transmission Line Pulse (TLP) $t_p = 100$ ns; square pulse; ANSI / ESD STM5.5.1-2008.

Fig. 3. Peak pulse power dissipation as a function of pulse duration; typical values

Fig. 4. Relative variation of peak pulse power as a function of junction temperature; typical values

Fig. 5. Diode capacitance as a function of reverse voltage; typical values
Unidirectional ESD protection diode

Transmission Line Pulse (TLP); $t_p = 100$ ns; $t_r = 1$ ns

**Fig. 6.** Dynamic resistance with positive clamping; typical values

IEC 61000-4-5; $t_p = 8/20$ µs; positive pulse

**Fig. 8.** Dynamic resistance with positive clamping; typical values

Transmission Line Pulse (TLP); $t_p = 100$ ns; $t_r = 1$ ns

**Fig. 7.** Dynamic resistance with negative clamping; typical values

IEC 61000-4-5; $t_p = 8/20$ µs; negative pulse

**Fig. 9.** Dynamic resistance with negative clamping; typical values
10. Application information

The device is designed for the protection of one unidirectional data or signal line from the damage caused by ESD and surge pulses. The device may be used on lines where the signal polarities are either positive or negative with respect to ground.

![Application diagram](aaa-002440)

**Fig. 10. Application diagram**

**Circuit board layout and protection device placement**

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. The path length between the device and the protected line should be minimized.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

11. Test information

**Quality information**

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.
### 12. Package outline

DFN1006BD-2  Leadless ultra small plastic package with side-wettable flanks (SWF); 2 terminals; 0.65 mm pitch; 1 mm x 0.6 mm x 0.47 mm body

![Package outline diagram](image)

#### Dimensions

<table>
<thead>
<tr>
<th>Unit</th>
<th>A(1)</th>
<th>A1</th>
<th>b(f(1))</th>
<th>b</th>
<th>D</th>
<th>E</th>
<th>e</th>
<th>L</th>
<th>T(1)</th>
<th>u</th>
<th>v</th>
<th>w</th>
<th>y</th>
<th>y1</th>
</tr>
</thead>
<tbody>
<tr>
<td>mm</td>
<td>0.50</td>
<td>0.04</td>
<td>0.55</td>
<td>0.55</td>
<td>0.60</td>
<td>1.00</td>
<td>0.65</td>
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<td>0.30</td>
<td>0.22</td>
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<tr>
<td>nom</td>
<td>0.47</td>
<td>0.20</td>
<td>0.46</td>
<td>0.60</td>
<td>1.00</td>
<td>0.65</td>
<td>0.25</td>
<td>0.16</td>
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<td>0.10</td>
<td>0.05</td>
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<tr>
<td>min</td>
<td>0.44</td>
<td>0.20</td>
<td>0.46</td>
<td>0.60</td>
<td>1.00</td>
<td>0.65</td>
<td>0.25</td>
<td>0.16</td>
<td>0.05</td>
<td>0.10</td>
<td>0.05</td>
<td>0.05</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note**
1. Dimension including plating thickness.
2. The marking bar indicates the cathode.
3. Solderable lead end, protrusion max. 0.02 mm.

#### Outline version

<table>
<thead>
<tr>
<th>Outline version</th>
<th>References</th>
<th>European projection</th>
<th>Issue date</th>
</tr>
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<tbody>
<tr>
<td>SOD882BD</td>
<td>IEC</td>
<td>JEDEC</td>
<td>JEITA</td>
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<tr>
<td></td>
<td>MO-343AA</td>
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</tbody>
</table>

Fig. 11. Package outline DFN1006BD-2 (SOD882BD)
13. Soldering

Footprint information for reflow soldering of DFN1006BD-2 package

Fig. 12. Reflow soldering footprint for DFN1006BD-2 (SOD882BD)
## 14. Revision history

Table 7. Revision history

<table>
<thead>
<tr>
<th>Data sheet ID</th>
<th>Release date</th>
<th>Data sheet status</th>
<th>Change notice</th>
<th>Supersedes</th>
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</thead>
<tbody>
<tr>
<td>PESD15VS1ULS</td>
<td>20210203</td>
<td>Product data sheet</td>
<td>-</td>
<td>-</td>
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</table>
15. Legal information

Data sheet status

<table>
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<tr>
<th></th>
<th></th>
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</thead>
<tbody>
<tr>
<td>Objective [short] data sheet</td>
<td>Development</td>
<td>This document contains data from the objective specification for product development.</td>
</tr>
<tr>
<td>Preliminary [short] data sheet</td>
<td>Qualification</td>
<td>This document contains data from the preliminary specification.</td>
</tr>
<tr>
<td>Product [short] data sheet</td>
<td>Production</td>
<td>This document contains the product specification.</td>
</tr>
</tbody>
</table>

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term "short data sheet" is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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