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Team Nexperia



NPN resistor-equipped transistor; R1 = 100 kΩ, R2 = 100 kΩRev. 1 — 1 June 2012Product data she

Product data sheet

#### 1. **Product profile**

#### **1.1 General description**

NPN Resistor-Equipped Transistor (RET) in a leadless ultra small DFN1006B-3 (SOT883B) Surface-Mounted Device (SMD) plastic package.

PNP complement: PDTA115EMB.

#### 1.2 Features and benefits

- 20 mA output current capability
- Reduces component count
- Built-in bias resistors
- Reduces pick and place costs

#### **1.3 Applications**

- Low-current peripheral driver
- Control of IC inputs

- Simplifies circuit design
- AEC-Q101 qualified
- Leadless ultra small SMD plastic package
- Low package height of 0.37 mm
- Replaces general-purpose transistors in digital applications
- Mobile applications

#### 1.4 Quick reference data

Table 1.	Quick reference data					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>CEO</sub>	collector-emitter voltage	open base	-	-	50	V
lo	output current		-	-	20	mA
R1	bias resistor 1 (input)	T <sub>amb</sub> = 25 °C	70	100	130	kΩ
R2/R1	bias resistor ratio		0.8	1	1.2	



NPN resistor-equipped transistor; R1 = 100 k $\Omega$ , R2 = 100 k $\Omega$ 

### 2. Pinning information

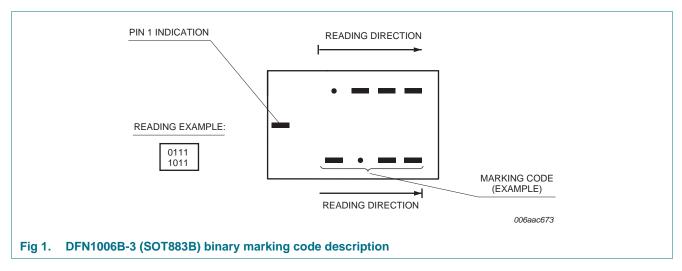
Table 2.	Pinning	j information		
Pin	Symbol	Description	Simplified outline	Graphic symbol
1	I	input (base)		
2	G	GND (emitter)		3
3	0	output (collector)	2 Transparent top view SOT883B (DFN1006B-3)	1 R2 R2 sym007

### 3. Ordering information

Table 3. Ordering information						
Type number	Package					
	Name	Description	Version			
PDTC115EMB	DFN1006B-3	Leadless ultra small plastic package; 3 solder lands; body 1.0 x 0.6 x 0.37 mm	SOT883B			

### 4. Marking

Type number	Marking code
PDTC115EMB	0011 0001



NPN resistor-equipped transistor; R1 = 100 k $\Omega$ , R2 = 100 k $\Omega$ 

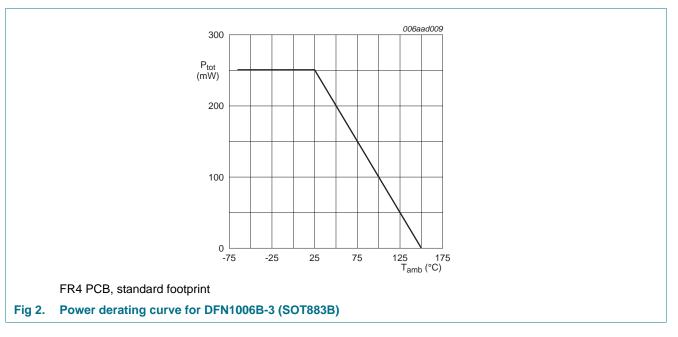
### 5. Limiting values

#### Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>CBO</sub>	collector-base voltage	open emitter		-	50	V
V <sub>CEO</sub>	collector-emitter voltage	open base		-	50	V
V <sub>EBO</sub>	emitter-base voltage	open collector		-	10	V
VI	input voltage	positive		-	40	V
		negative		-	-10	V
lo	output current			-	20	mA
I <sub>CM</sub>	peak collector current	pulsed; t <sub>p</sub> ≤ 1 ms		-	100	mA
P <sub>tot</sub>	total power dissipation	$T_{amb} \le 25 \ ^{\circ}C$	<u>[1]</u>	-	250	mW
Tj	junction temperature			-	150	°C
T <sub>amb</sub>	ambient temperature			-65	150	°C
T <sub>stg</sub>	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.



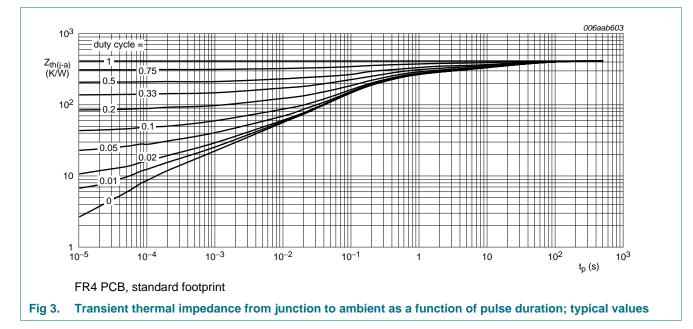
### 6. Thermal characteristics

Table 6.	Thermal characteristics						
Symbol	Parameter	Conditions		Min	Тур	Max	Unit
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air	[1]	-	-	500	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

# PDTC115EMB

NPN resistor-equipped transistor; R1 = 100 k $\Omega$ , R2 = 100 k $\Omega$ 



### 7. Characteristics

#### Table 7. Characteristics

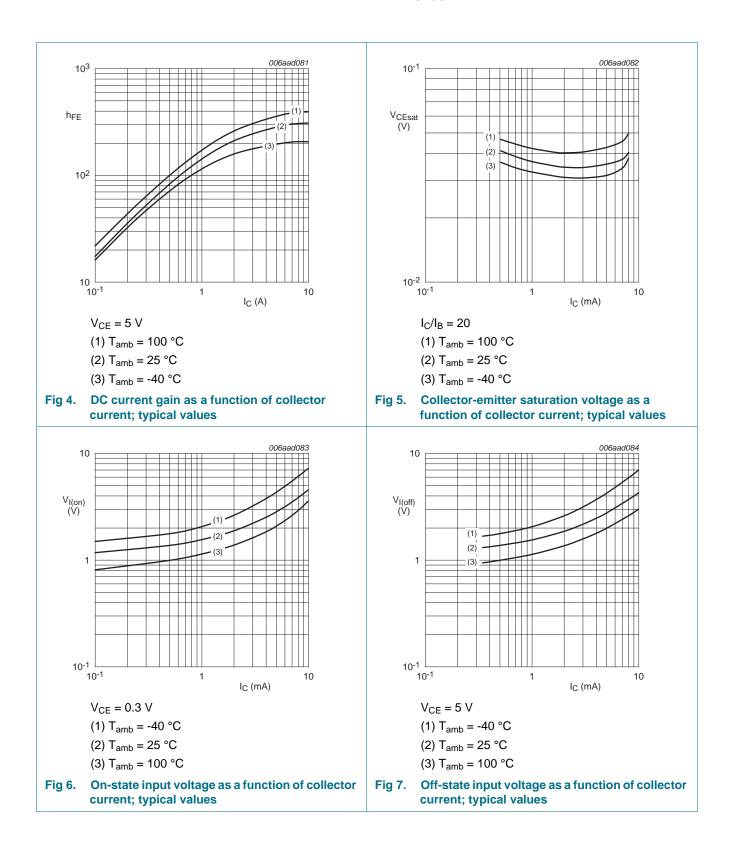
Table 7.	Characteristics						
Symbol	Parameter	Conditions		Min	Тур	Мах	Unit
I <sub>CBO</sub>	collector-base cut-off current	$V_{CB}$ = 50 V; I <sub>E</sub> = 0 A; T <sub>amb</sub> = 25 °C		-	-	100	nA
I <sub>CEO</sub>	collector-emitter cut-off	$V_{CE} = 30 \text{ V}; \text{ I}_{B} = 0 \text{ A}; \text{ T}_{amb} = 25 \text{ °C}$		-	-	1	μΑ
	current	$V_{CE} = 30 \text{ V}; I_B = 0 \text{ A}; T_j = 150 \text{ °C}$		-	-	5	μΑ
I <sub>EBO</sub>	emitter-base cut-off current	$V_{EB}$ = 5 V; I <sub>C</sub> = 0 A; T <sub>amb</sub> = 25 °C		-	-	50	μA
h <sub>FE</sub>	DC current gain	$V_{CE}$ = 5 V; I <sub>C</sub> = 5 mA; T <sub>amb</sub> = 25 °C		80	-	-	
V <sub>CEsat</sub>	collector-emitter saturation voltage	$I_{C}$ = 5 mA; $I_{B}$ = 0.25 mA; $T_{amb}$ = 25 °C		-	-	150	mV
V <sub>I(off)</sub>	off-state input voltage	$V_{CE} = 5 \text{ V}; \text{ I}_{C} = 100 \mu\text{A}; \text{ T}_{amb} = 25 ^{\circ}\text{C}$		-	1.1	0.5	V
V <sub>I(on)</sub>	on-state input voltage	$V_{CE}$ = 0.3 V; $I_{C}$ = 1 mA; $T_{amb}$ = 25 °C		3	1.5	-	V
R1	bias resistor 1 (input)	T <sub>amb</sub> = 25 °C		70	100	130	kΩ
R2/R1	bias resistor ratio			0.8	1	1.2	
C <sub>C</sub>	collector capacitance	$V_{CB} = 10 \text{ V}; I_E = 0 \text{ A}; i_e = 0 \text{ A};$ f = 1 MHz; T <sub>amb</sub> = 25 °C		-	-	2.5	pF
f <sub>T</sub>	transition frequency	$V_{CE}$ = 5 V; I <sub>C</sub> = 10 mA; f = 100 MHz; T <sub>amb</sub> = 25 °C	<u>[1]</u>	-	230	-	MHz

[1] Characteristics of built-in transistor.

PDTC115EMB Product data sheet

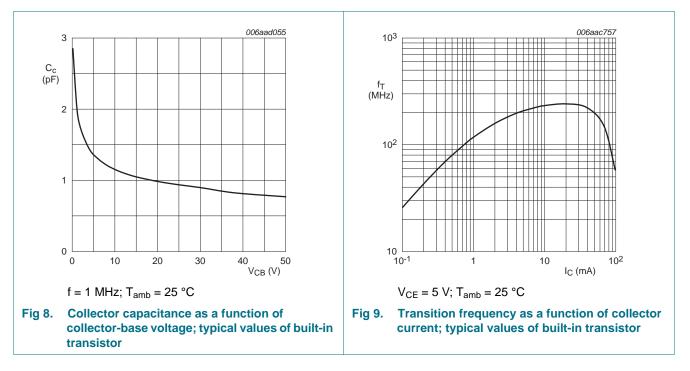
# PDTC115EMB

NPN resistor-equipped transistor; R1 = 100 k $\Omega$ , R2 = 100 k $\Omega$ 



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NPN resistor-equipped transistor; R1 = 100 k $\Omega$ , R2 = 100 k $\Omega$ 



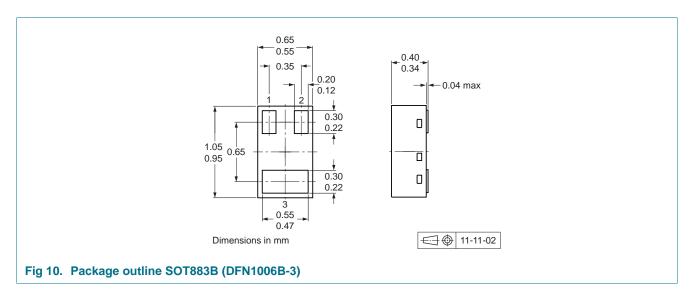
### 8. Test information

#### 8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

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#### **Package outline** 9.



### 10. Soldering

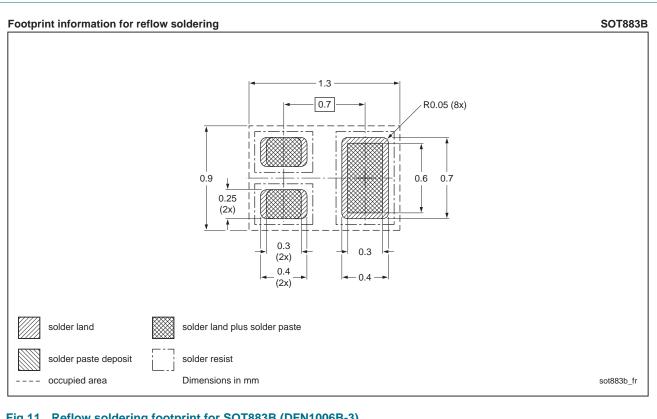


Fig 11. Reflow soldering footprint for SOT883B (DFN1006B-3)

PDTC115EMB **Product data sheet** 

NPN resistor-equipped transistor; R1 = 100 k $\Omega$ , R2 = 100 k $\Omega$ 

## **11. Revision history**

Table 8. Revision I	Revision history						
Document ID	Release date	Data sheet status	Change notice	Supersedes			
PDTC115EMB v.1	20120601	Product data sheet	-	-			

NPN resistor-equipped transistor; R1 = 100 k $\Omega$ , R2 = 100 k $\Omega$ 

### 12. Legal information

#### **12.1 Data sheet status**

Document status <sup>[1]</sup> <sup>[2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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**Product data sheet** 

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# PDTC115EMB

NPN resistor-equipped transistor; R1 = 100 k $\Omega$ , R2 = 100 k $\Omega$ 

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