



PDTC115EM

50 V, 20 mA NPN resistor-equipped transistor;
R1 = 100 k Ω , R2 = 100 k Ω

10 October 2024

Product data sheet

1. General description

NPN Resistor-Equipped Transistor (RET) in an leadless ultra small SOT883 (SC-101) Surface-Mounted Device (SMD) plastic package.

PNP complement: PDTA115EM

2. Features and benefits

- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- AEC-Q101 qualified

3. Applications

- General purpose switching and amplification
- Inverter and interface circuits
- Circuit driver

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CEO}	collector-emitter voltage	open base	-	-	50	V
I _O	output current		-	-	20	mA
R1	bias resistor 1 (input)	T _{amb} = 25 °C	70	100	130	k Ω
R2/R1	bias resistor ratio		0.8	1	1.2	

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	I	input (base)	<p>Transparent top view DFN1006-3 (SOT883)</p>	<p>sym007</p>
2	GND	ground (emitter)		
3	O	output (collector)		

50 V, 20 mA NPN resistor-equipped transistor; R1 = 100 kΩ, R2 = 100 kΩ

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PDTC115EM	DFN1006-3	plastic, leadless ultra small package; 3 terminals; 0.35 mm pitch; 1 mm x 0.6 mm x 0.48 mm body	SOT883

7. Marking

Table 4. Marking codes

Type number	Marking code
PDTC115EM	DV

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CBO}	collector-base voltage	open emitter	-	50	V
V_{CEO}	collector-emitter voltage	open base	-	50	V
V_{EBO}	emitter-base voltage	open collector	-	10	V
V_i	input voltage		-10	40	V
I_O	output current		-	20	mA
I_{CM}	peak collector current	$t_p \leq 1$ ms; single pulse	-	100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1] [2]	250	mW
T_j	junction temperature		-	150	°C
T_{amb}	ambient temperature		-65	150	°C
T_{stg}	storage temperature		-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), with 60 μm copper strip line, standard footprint.

[2] Reflow soldering is the only recommended soldering method.

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1] [2]	-	500	K/W

[1] Device mounted on an FR4 PCB, with 60 μm copper strip line, standard footprint.

[2] Reflow soldering is the only recommended soldering method.

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CBO}	collector-base cut-off current	$V_{CB} = 50\text{ V}$; $I_E = 0\text{ A}$; $T_{amb} = 25\text{ °C}$	-	-	100	nA
I_{CEO}	collector-emitter cut-off current	$V_{CE} = 30\text{ V}$; $I_B = 0\text{ A}$; $T_{amb} = 25\text{ °C}$	-	-	100	nA
		$V_{CE} = 30\text{ V}$; $I_B = 0\text{ A}$; $T_j = 150\text{ °C}$	-	-	5	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = 5\text{ V}$; $I_C = 0\text{ A}$; $T_{amb} = 25\text{ °C}$	-	-	50	μA
h_{FE}	DC current gain	$V_{CE} = 5\text{ V}$; $I_C = 5\text{ mA}$; $T_{amb} = 25\text{ °C}$	80	-	-	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 5\text{ mA}$; $I_B = 0.25\text{ mA}$; $T_{amb} = 25\text{ °C}$	-	-	150	mV
$V_{I(off)}$	off-state input voltage	$V_{CE} = 5\text{ V}$; $I_C = 100\text{ μA}$; $T_{amb} = 25\text{ °C}$	-	1.1	0.5	V
$V_{I(on)}$	on-state input voltage	$V_{CE} = 0.3\text{ V}$; $I_C = 1\text{ mA}$; $T_{amb} = 25\text{ °C}$	3	1.5	-	V
R1	bias resistor 1 (input)	$T_{amb} = 25\text{ °C}$	70	100	130	kΩ
R2/R1	bias resistor ratio		0.8	1	1.2	
C_c	collector capacitance	$V_{CB} = 10\text{ V}$; $I_E = 0\text{ A}$; $i_e = 0\text{ A}$; $f = 1\text{ MHz}$; $T_{amb} = 25\text{ °C}$	-	-	2.5	pF

11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

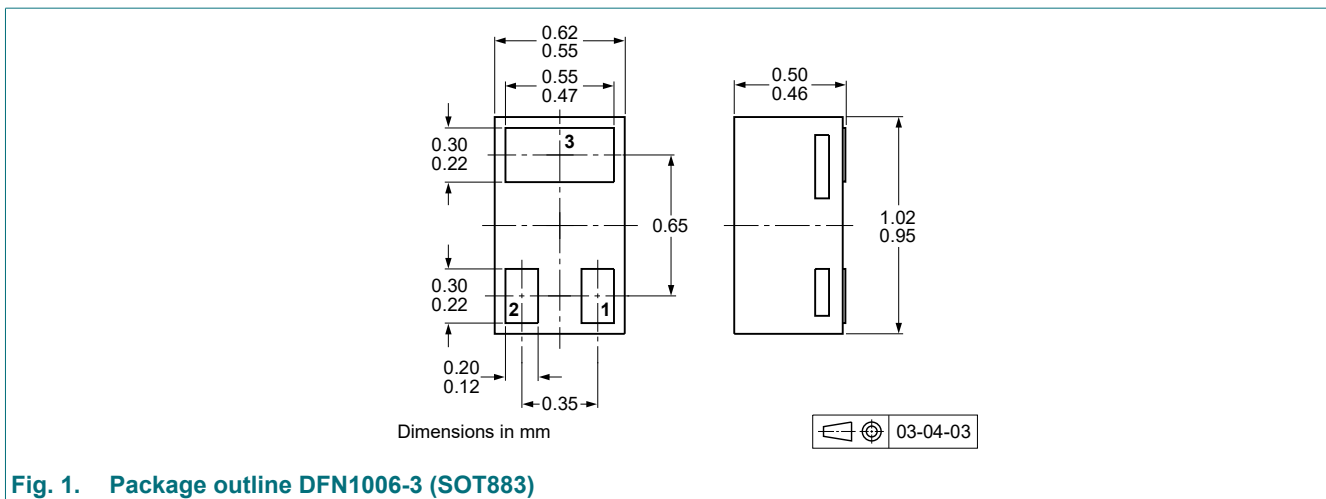


Fig. 1. Package outline DFN1006-3 (SOT883)

13. Soldering

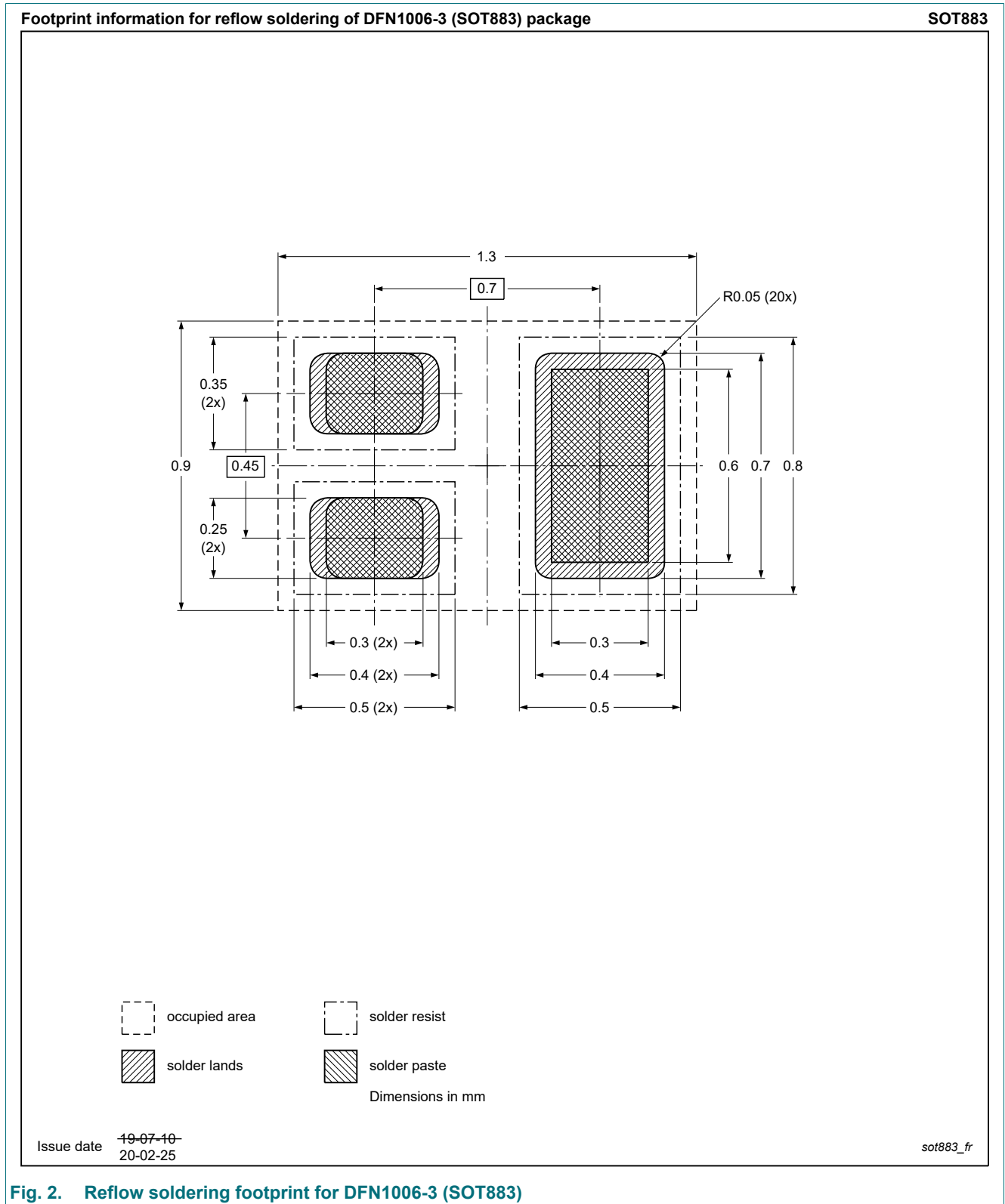


Fig. 2. Reflow soldering footprint for DFN1006-3 (SOT883)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PDTC115EM v.3	20241010	Product data sheet	-	PDTC115E series v.2
Modification:	<ul style="list-style-type: none">The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.Legal texts have been adapted to the new company name where appropriate.Family data sheet reduced to single type data sheet.Packing information removed.			
PDTC115E series v.2	20040806	Product data sheet	-	PDTC115E series v.1
PDTC115E series v.1	20040406	Product specification	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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For sales office addresses, please send an email to: salesaddresses@nexperia.com
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