Product data sheet

1. General description

PNP low V_{CEsat} transistor in DFN2020D-3 (SOT1061D) leadless small Surface-Mounted Device (SMD) plastic package with visible and solderable side pads.

NPN complement: PBSS4350PAS

2. Features and benefits

- DFN2020D-3 (SOT1061D) package
- Low collector-emitter saturation voltage V_{CEsat}
- High collector current capability: I_C and I_{CM}
- Higher efficiency leading to less heat generation
- Reduced printed-circuit board requirements
- Leadless small SMD plastic package with solderable side pads
- · Exposed heat sink for excellent thermal and electrical conductivity
- Suitable for Automatic Optical Inspection (AOI) of solder joint

3. Applications

- Loadswitch
 - · Battery-driven devices
 - Power management
 - Charging circuits
 - · Power switches (e.g. motors, fans)

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{CEO}	collector-emitter voltage	open base	-	-	-50	V
I _C	collector current		-	-	-3	А
I _{CM}	peak collector current	limited by T _{j(max)}	-	-	-5	Α
R _{CEsat}	collector-emitter saturation resistance	I_C = -2 A; I_B = -200 mA; pulsed; $t_p \le$ 300 μs; δ ≤ 0.02; T_{amb} = 25 °C	-	90	135	mΩ



50 V, 3 A PNP low VCEsat transistor

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	В	base	3	
2	E	emitter		С
3	С	collector	Transparent top view DFN2020D-3 (SOT1061D)	B E sym021

6. Ordering information

Table 3. Ordering information

Type number	Package					
	Name	Description	Version			
PBSS5350PAS	DFN2020D-3	plastic, leadless thermal enhanced ultra thin small outline package with side-wettable flanks (SWF); no leads; 3 terminals; 1.3 mm pitch; 2 mm x 2 mm x 0.65 mm body	<u>SOT1061D</u>			

7. Marking

Table 4. Marking codes

Type number	Marking code
PBSS5350PAS	G4

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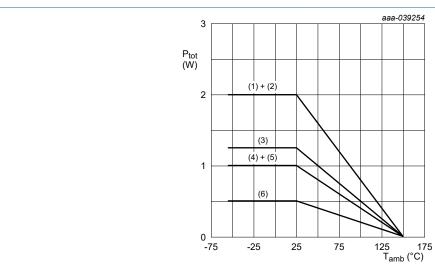
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CBO}	collector-base voltage	open emitter		-	-50	V
V _{CEO}	collector-emitter voltage	open base		-	-50	V
V _{EBO}	emitter-base voltage	open collector		-	-5	V
I _C	collector current			-	-3	Α
I _{CM}	peak collector current	limited by T _{j(max)}		-	-5	Α
I _B	base current			-	-0.5	Α
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	0.5	W
			[2] [3]	-	1	W
			[4]	-	1.2	W
			[5] [6]	-	2	W
Tj	junction temperature			-	150	°C
T _{amb}	ambient temperature			-65	150	°C
T _{stg}	storage temperature			-65	150	°C

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm².
- [3] Device mounted on an FR4 PCB, 4-layer copper, tin-plated and standard footprint.
- [4] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 6 cm².
- [5] Device mounted on a ceramic PCB, Al₂O₃, standard footprint.
- [6] Device mounted on a FR4 PCB, 4-layer copper, tin-plated and mounting pad for collector 1 cm².



- (1) Ceramic PCB, single-sided copper, standard footprint
- (2) FR4 PCB, 4-layer copper, 1 cm²
- (3) FR4 PCB, single-sided copper, 6 cm²
- (4) FR4 PCB, single-sided copper, 1 cm²
- (5) FR4 PCB, 4-layer copper, standard footprint
- (6) FR4 PCB, single-sided copper, standard footprint

Fig. 1. Power derating curves

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9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
uiy-a)	thermal resistance from	-	[1]	-	-	250	K/W
	junction to ambient		[2] [3]	-	-	125	K/W
			[4]	-	-	100	K/W
			[5] [6]	-	-	60	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm².
- [3] Device mounted on an FR4 PCB, 4-layer copper, tin-plated and standard footprint.
- [4] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 6 cm²
- [5] Device mounted on a ceramic PCB, Al₂O₃, standard footprint.
- [6] Device mounted on a FR4 PCB, 4-layer copper, tin-plated and mounting pad for collector 1 cm².

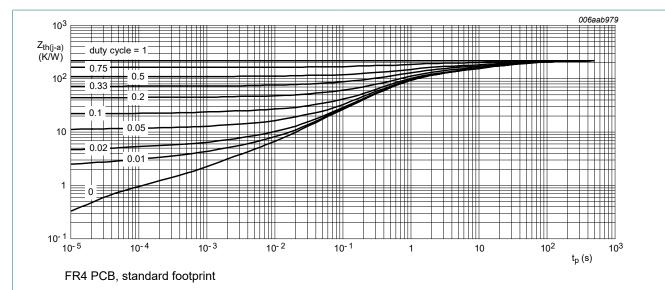


Fig. 2. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

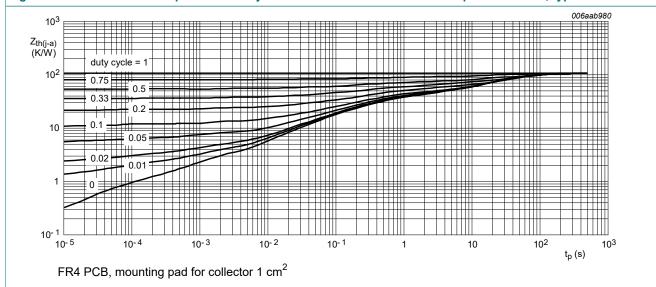


Fig. 3. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

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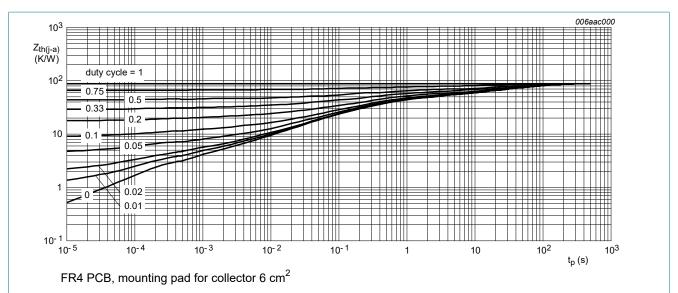
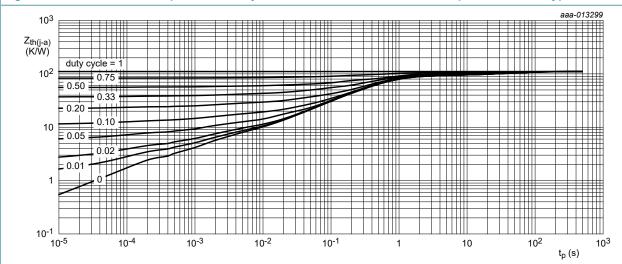
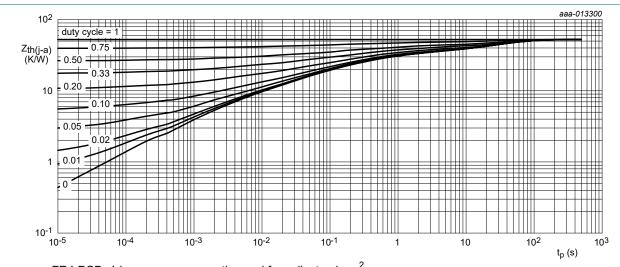


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, 4-layer copper, standard footprint

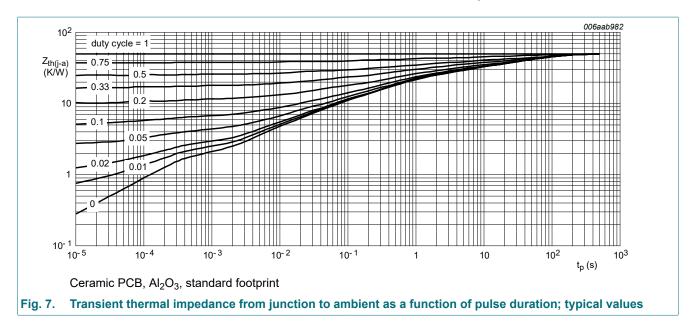
Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, 4-layer copper, mounting pad for collector 1 cm²

Fig. 6. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

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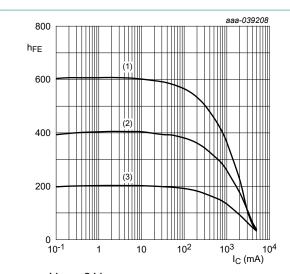
50 V, 3 A PNP low VCEsat transistor

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{(BR)CBO}	collector-base breakdown voltage	$I_C = -100 \ \mu A; I_E = 0 \ A; T_{amb} = 25 \ ^{\circ}C$	-50	-	-	V
V _{(BR)CEO}	collector-emitter breakdown voltage	$I_C = -10 \text{ mA}; I_B = 0 \text{ A}; T_{amb} = 25 \text{ °C}$	-50	-	-	V
J _{(BR)EBO}	emitter-base breakdown voltage (collector open)	$I_E = -100 \mu A; I_C = 0 A; T_{amb} = 25 °C$	-5	-	-	V
СВО	collector-base cut-off	V _{CB} = -50 V; I _E = 0 A; T _{amb} = 25 °C	-	-	-100	nA
	current	$V_{CB} = -50 \text{ V}; I_E = 0 \text{ A}; T_j = 150 \text{ °C}$	-	-	-50	μΑ
EBO	emitter-base cut-off current	$V_{EB} = -5 \text{ V}; I_{C} = 0 \text{ A}; T_{amb} = 25 \text{ °C}$	-	-	-100	nA
CES	collector-emitter cut-off current	$V_{CE} = -50 \text{ V}; V_{BE} = 0 \text{ V}; T_{amb} = 25 \text{ °C}$	-	-	-100	nA
J ^{EE}	DC current gain	V_{CE} = -2 V; I_{C} = 0.1 A; single pulse; t_{p} ≤ 300 μs; δ ≤ 0.02; T_{amb} = 25 °C	200	-	-	
		V_{CE} = -2 V; I_{C} = -0.5 A; pulsed; t_{p} ≤ 300 μs; δ ≤ 0.02; T_{amb} = 25 °C	200	-	-	
		V_{CE} = -2 V; I_{C} = -1 A; pulsed; t_{p} ≤ 300 μs; δ ≤ 0.02; T_{amb} = 25 °C	200	-	450	
		V_{CE} = -2 V; I_{C} = -2 A; pulsed; t_{p} ≤ 300 μs; δ ≤ 0.02; T_{amb} = 25 °C	130	-	-	
		V_{CE} = -2 V; I_{C} = -3 A; pulsed; t_{p} ≤ 300 μs; δ ≤ 0.02; T_{amb} = 25 °C	80	-	-	
/ _{CEsat}	collector-emitter	$I_C = -0.5 \text{ A}; I_B = -50 \text{ mA}; T_{amb} = 25 \text{ °C}$	-	-	-90	mV
	saturation voltage	$I_C = -1 \text{ A}; I_B = -50 \text{ mA}; T_{amb} = 25 ^{\circ}\text{C}$	-	-	-180	mV
		I _C = -2 A; I _B = -100 mA; T _{amb} = 25 °C	-	-	-320	mV
		I_C = -2 A; I_B = -200 mA; pulsed; t_p ≤ 300 μs; δ ≤ 0.02; T_{amb} = 25 °C	-	-	-270	mV
		I_C = -3 A; I_B = -300 mA; pulsed; t_p ≤ 300 μs; δ ≤ 0.02; T_{amb} = 25 °C	-	-	-390	mV
RCEsat	collector-emitter saturation resistance	I_C = -2 A; I_B = -200 mA; pulsed; t_p ≤ 300 μs; δ ≤ 0.02; T_{amb} = 25 °C	-	90	135	mΩ
/ _{BEsat}	base-emitter saturation	$I_C = -2 \text{ A}; I_B = -100 \text{ mA}; T_{amb} = 25 ^{\circ}\text{C}$	-	-	-1.1	V
	voltage	I_C = -3 A; I_B = -300 mA; pulsed; t_p ≤ 300 μs; δ ≤ 0.02; T_{amb} = 25 °C	-	-	-1.2	V
/ _{BE}	base-emitter voltage	V _{CE} = -2 V; I _C = -1 A; T _{amb} = 25 °C	-	-	-1.1	V
T	transition frequency	V_{CE} = -5 V; I_{C} = -100 mA; f = 100 MHz; T_{amb} = 25 °C	100	-	-	MHz
C _c	collector capacitance	$V_{CB} = -10 \text{ V}; I_E = 0 \text{ A}; i_e = 0 \text{ A};$ f = 1 MHz; $T_{amb} = 25 ^{\circ}\text{C}$	-	-	35	pF

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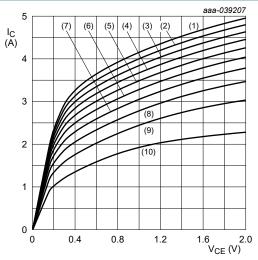
 $V_{CE} = 2 V$

 $(1) T_{amb} = 100 °C$

(2) T_{amb} = 25 °C

(3) $T_{amb} = -55 \, ^{\circ}C$

Fig. 8. DC current gain as a function of collector current; typical values



 T_{amb} = 25 °C

(1) $I_B = 130 \text{ mA}$

(2) $I_B = 117 \text{ mA}$ (3) $I_B = 104 \text{ mA}$ (4) $I_B = 91 \text{ mA}$ (5) $I_B = 78 \text{ mA}$

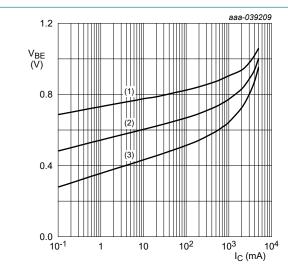
 $(6) I_B = 65 \text{ mA}$

 $(7) I_B = 52 \text{ mA}$

(8) $I_B = 39 \text{ mA}$

(9) $I_B = 26 \text{ mA}$ $(10) I_B = 13 \text{ mA}$

Collector current as a function of collector-Fig. 9. emitter voltage; typical values



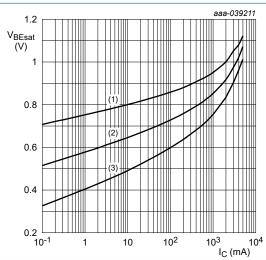
 $V_{CE} = 2 V$

(1) $T_{amb} = -55 \, ^{\circ}C$

(2) $T_{amb} = 25 \, ^{\circ}C$

(3) $T_{amb} = 100 \, ^{\circ}C$

Fig. 10. Base-emitter voltage as a function of collector current; typical values



 $I_{\rm C}/I_{\rm B} = 20$

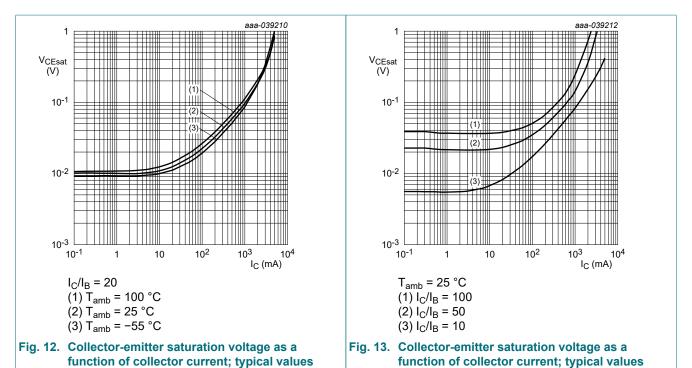
(1) $T_{amb} = -55$ °C

(2) $T_{amb} = 25 \, ^{\circ}C$

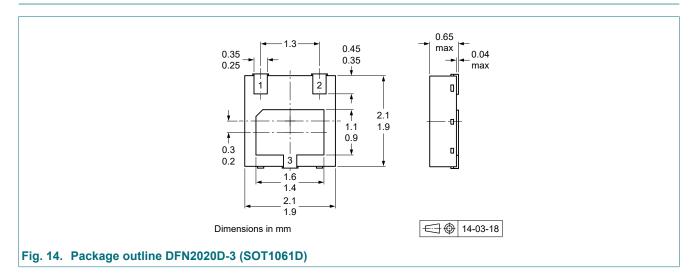
(3) $T_{amb} = 100 \, ^{\circ}C$

Fig. 11. Base-emitter saturation voltage as a function of collector current; typical values

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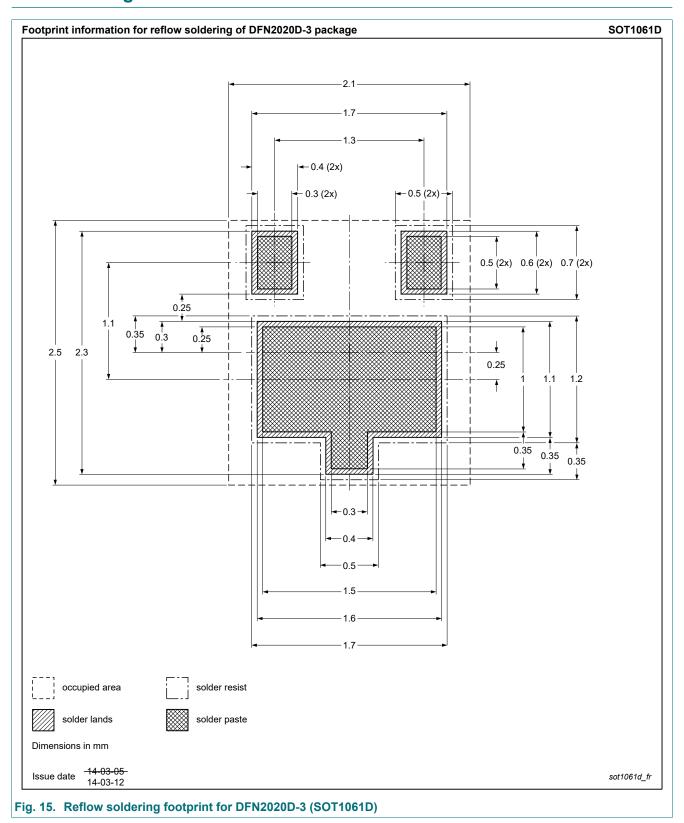


11. Package outline



50 V, 3 A PNP low VCEsat transistor

12. Soldering



50 V, 3 A PNP low VCEsat transistor

13. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PBSS5350PAS v.1	20240516	Product data sheet	-	-

50 V, 3 A PNP low VCEsat transistor

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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PBSS5350PAS

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