**Product data sheet** 

## 1. General description

NPN low  $V_{CEsat}$  DFN2020D-3 (SOT1061D) leadless small Surface-Mounted Device (SMD) plastic package.

PNP complement: PBSS5350PAS

### 2. Features and benefits

- DFN2020D-3 (SOT1061D) package
- Low collector-emitter saturation voltage V<sub>CEsat</sub>
- High collector current capability: I<sub>C</sub> and I<sub>CM</sub>
- Higher efficiency leading to less heat generation
- Reduced printed-circuit board requirements
- Leadless small SMD plastic package with solderable side pads
- · Exposed heat sink for excellent thermal and electrical conductivity
- Suitable for Automatic Optical Inspection (AOI) of solder joint

## 3. Applications

- Loadswitch
  - Battery-driven devices
  - Power management
  - Charging circuits
  - · Power switches (e.g. motors, fans)

## 4. Quick reference data

#### Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>CEO</sub>	collector-emitter voltage	open base	-	-	50	V
I <sub>C</sub>	collector current		-	-	3	А
I <sub>CM</sub>	peak collector current	limited by T <sub>j(max)</sub>	-	-	5	A
R <sub>CEsat</sub>	collector-emitter saturation resistance	$I_C$ = 2 A; $I_B$ = 200 mA; pulsed; $t_p$ ≤ 300 μs; δ ≤ 0.02; $T_{amb}$ = 25 °C	-	100	130	mΩ



50 V, 3 A PNP low VCEsat transistor

# 5. Pinning information

### **Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	В	base	3	
2	Е	emitter		С
3	С	collector	Transparent top view DFN2020D-3 (SOT1061D)	B — E sym021

# 6. Ordering information

## **Table 3. Ordering information**

Type number			
	Name	Description	Version
PBSS4350PAS		plastic, leadless thermal enhanced ultra thin small outline package with side-wettable flanks (SWF); no leads; 3 terminals; 1.3 mm pitch; 2 mm x 2 mm x 0.65 mm body	<u>SOT1061D</u>

# 7. Marking

### Table 4. Marking codes

Type number	Marking code
PBSS4350PAS	G6

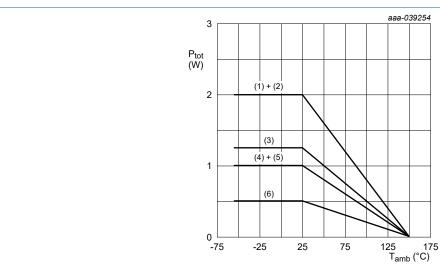
## 8. Limiting values

#### **Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>CBO</sub>	collector-base voltage	open emitter		-	50	V
$V_{CEO}$	collector-emitter voltage	open base		-	50	V
V <sub>EBO</sub>	emitter-base voltage	open collector		-	5	V
I <sub>C</sub>	collector current			-	3	Α
I <sub>CM</sub>	peak collector current	limited by T <sub>j(max)</sub>		-	5	Α
I <sub>B</sub>	base current			-	0.5	Α
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C	[1]	-	0.5	W
			[2] [3]	-	1	W
			[4]	-	1.2	W
			[5] [6]	-	2	W
Tj	junction temperature			-	150	°C
T <sub>amb</sub>	ambient temperature			-65	150	°C
T <sub>stg</sub>	storage temperature			-65	150	°C

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.
- [3] Device mounted on an FR4 PCB, 4-layer copper, tin-plated and standard footprint.
- [4] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 6 cm<sup>2</sup>.
- [5] Device mounted on a ceramic PCB, Al<sub>2</sub>O<sub>3</sub>, standard footprint.
- [6] Device mounted on a FR4 PCB, 4-layer copper, tin-plated and mounting pad for collector 7 cm<sup>2</sup>.



- (1) Ceramic PCB, single-sided copper, standard footprint
- (2) FR4 PCB, 4-layer copper, 1 cm<sup>2</sup>
- (3) FR4 PCB, single-sided copper, 6 cm<sup>2</sup>
- (4) FR4 PCB, single-sided copper, 1 cm<sup>2</sup>
- (5) FR4 PCB, 4-layer copper, standard footprint
- (6) FR4 PCB, single-sided copper, standard footprint

Fig. 1. Power derating curves

## 9. Thermal characteristics

**Table 6. Thermal characteristics** 

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	ient	[1]	-	-	250	K/W
			[2] [3]	-	-	125	K/W
			[4]	-	-	100	K/W
			[5] [6]	-	-	60	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.
- [3] Device mounted on an FR4 PCB, 4-layer copper, tin-plated and standard footprint.
- [4] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 6 cm<sup>2</sup>.
- [5] Device mounted on a ceramic PCB, Al<sub>2</sub>O<sub>3</sub>, standard footprint.
- [6] Device mounted on a FR4 PCB, 4-layer copper, tin-plated and mounting pad for collector 1 cm<sup>2</sup>.

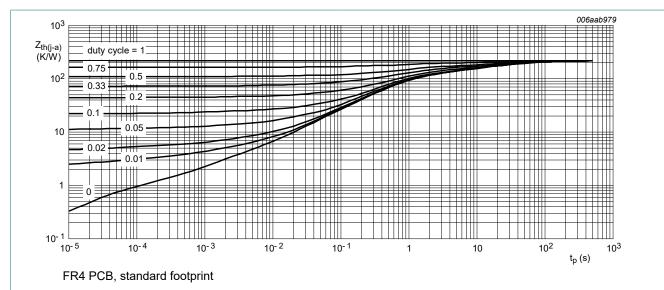


Fig. 2. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

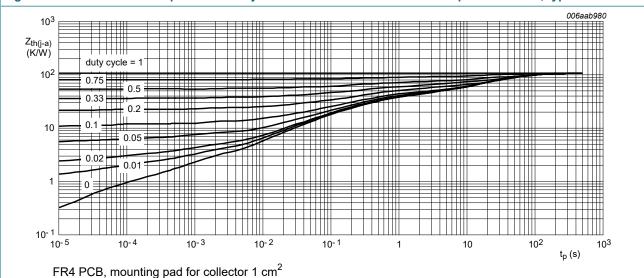


Fig. 3. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

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#### 50 V, 3 A PNP low VCEsat transistor

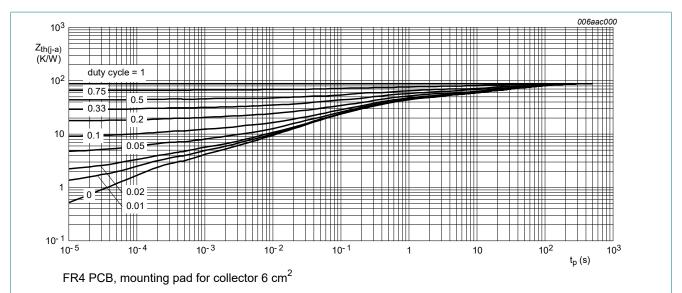
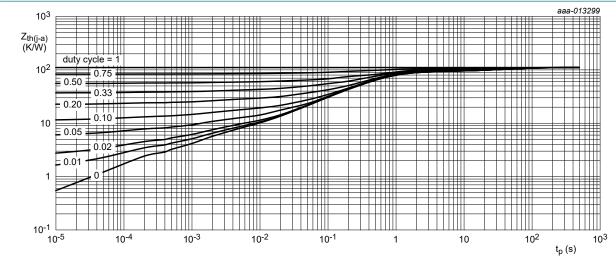
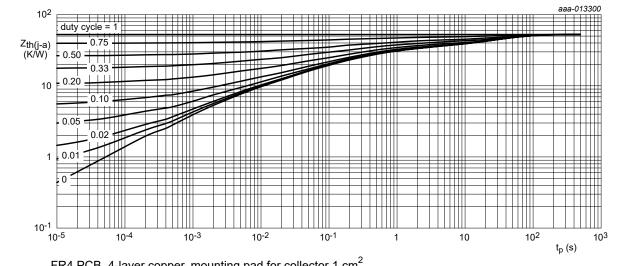


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, 4-layer copper, standard footprint

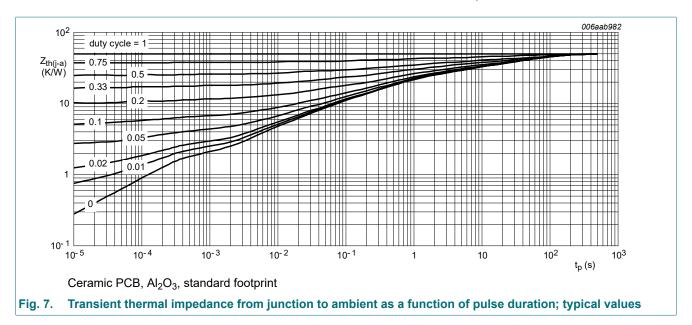
Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, 4-layer copper, mounting pad for collector 1 cm<sup>2</sup>

Transient thermal impedance from junction to ambient as a function of pulse duration; typical values Fig. 6.

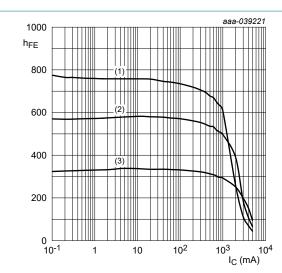
## 50 V, 3 A PNP low VCEsat transistor



# 10. Characteristics

#### **Table 7. Characteristics**

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>(BR)CBO</sub>	collector-base breakdown voltage	$I_C = 100 \ \mu A; I_E = 0 \ A; T_{amb} = 25 \ ^{\circ}C$	50	-	-	V
V <sub>(BR)CEO</sub>	collector-emitter breakdown voltage	$I_C = 10 \text{ mA}; I_B = 0 \text{ A}; T_{amb} = 25 \text{ °C}$	50	-	-	V
V <sub>(BR)EBO</sub>	emitter-base breakdown voltage (collector open)	$I_E = 100 \mu A; I_C = 0 A; T_{amb} = 25 °C$	5	-	-	V
СВО	collector-base cut-off	V <sub>CB</sub> = 50 V; I <sub>E</sub> = 0 A; T <sub>amb</sub> = 25 °C	-	-	100	nA
	current	$V_{CB} = 50 \text{ V}; I_E = 0 \text{ A}; T_j = 150 ^{\circ}\text{C}$	-	-	50	μΑ
I <sub>EBO</sub>	emitter-base cut-off current	V <sub>EB</sub> = 5 V; I <sub>C</sub> = 0 A; T <sub>amb</sub> = 25 °C	-	-	100	nA
CES	collector-emitter cut-off current	V <sub>CE</sub> = 50 V; V <sub>BE</sub> = 0 V; T <sub>amb</sub> = 25 °C	-	-	100	nA
h <sub>FE</sub>	DC current gain	$V_{CE}$ = 2 V; $I_{C}$ = 0.1 A; single pulse; $t_{p}$ ≤ 300 μs; δ ≤ 0.02; $T_{amb}$ = 25 °C	300	-	-	
		$V_{CE}$ = 2 V; $I_{C}$ = 0.5 A; pulsed; $t_{p}$ ≤ 300 μs; δ ≤ 0.02; $T_{amb}$ = 25 °C	300	-	-	
		$V_{CE}$ = 2 V; $I_{C}$ = 1 A; pulsed; $t_{p} \le 300 \ \mu s$ ; δ ≤ 0.02; $T_{amb}$ = 25 °C	300	-	700	
		$V_{CE}$ = 2 V; $I_{C}$ = 2 A; pulsed; $t_{p} \le 300 \ \mu s$ ; δ ≤ 0.02; $T_{amb}$ = 25 °C	200	-	-	
		$V_{CE}$ = 2 V; $I_{C}$ = 3 A; pulsed; $t_{p} \le 300 \ \mu s$ ; δ ≤ 0.02; $T_{amb}$ = 25 °C	100	-	-	
V <sub>CEsat</sub>	t collector-emitter	I <sub>C</sub> = 0.5 A; I <sub>B</sub> = 50 mA; T <sub>amb</sub> = 25 °C	-	-	80	mV
	saturation voltage	I <sub>C</sub> = 1 A; I <sub>B</sub> = 50 mA; T <sub>amb</sub> = 25 °C	-	-	160	mV
		I <sub>C</sub> = 2 A; I <sub>B</sub> = 100 mA; T <sub>amb</sub> = 25 °C	-	-	280	mV
		$I_C$ = 2 A; $I_B$ = 200 mA; pulsed; $t_p \le$ 300 μs; δ ≤ 0.02; $T_{amb}$ = 25 °C	-	-	260	mV
		$I_C$ = 3 A; $I_B$ = 300 mA; pulsed; $t_p \le$ 300 μs; δ ≤ 0.02; $T_{amb}$ = 25 °C	-	-	370	mV
R <sub>CEsat</sub>	collector-emitter saturation resistance	$I_C$ = 2 A; $I_B$ = 200 mA; pulsed; $t_p \le$ 300 μs; δ ≤ 0.02; $T_{amb}$ = 25 °C	-	100	130	mΩ
V <sub>BEsat</sub>	base-emitter saturation	I <sub>C</sub> = 2 A; I <sub>B</sub> = 100 mA; T <sub>amb</sub> = 25 °C	-	-	1.1	V
	voltage	$I_C$ = 3 A; $I_B$ = 300 mA; pulsed; $t_p \le$ 300 μs; δ ≤ 0.02; $T_{amb}$ = 25 °C	-	-	1.2	V
$V_{BEon}$	base-emitter turn-on voltage	V <sub>CE</sub> = 2 V; I <sub>C</sub> = 1 A; T <sub>amb</sub> = 25 °C	-	-	1.1	V
f <sub>T</sub>	transition frequency	$V_{CE}$ = 5 V; $I_{C}$ = 100 mA; f = 100 MHz; $T_{amb}$ = 25 °C	100	-	-	MHz
C <sub>c</sub>	collector capacitance	$V_{CB}$ = 10 V; $I_{E}$ = 0 A; $i_{e}$ = 0 A; f = 1 MHz; $T_{amb}$ = 25 °C	-	-	25	pF



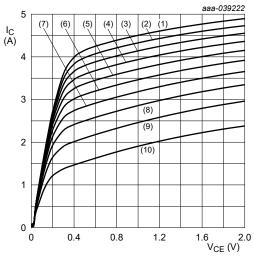
 $V_{CE} = 2 V$ 

 $(1) T_{amb} = 100 °C$ 

(2)  $T_{amb}$  = 25 °C

(3)  $T_{amb} = -55 \, ^{\circ}C$ 

Fig. 8. DC current gain as a function of collector current; typical values



T<sub>amb</sub> = 25 °C

(1)  $I_B = 82 \text{ mA}$ 

(2)  $I_B = 72 \text{ mA}$ (3)  $I_B = 64 \text{ mA}$ (4)  $I_B = 56 \text{ mA}$ (5)  $I_B = 48 \text{ mA}$ 

 $(6) I_B = 40 \text{ mA}$ 

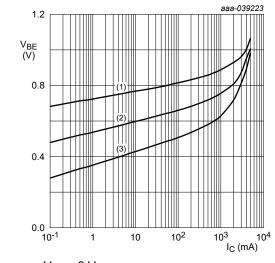
 $(7) I_B = 32 \text{ mA}$ 

(8)  $I_B = 24 \text{ mA}$ 

(9)  $I_B = 16 \text{ mA}$  $(10) I_B = 8 mA$ 

Collector current as a function of collector-Fig. 9.

emitter voltage; typical values



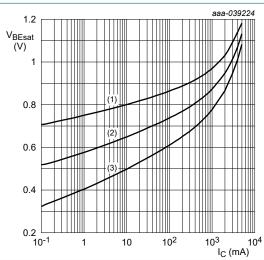
 $V_{CE} = 2 V$ 

(1)  $T_{amb} = -55 \, ^{\circ}C$ 

(2)  $T_{amb} = 25 \, ^{\circ}C$ 

(3)  $T_{amb} = 100 \, ^{\circ}C$ 

Fig. 10. Base-emitter voltage as a function of collector current; typical values



 $I_{\rm C}/I_{\rm B} = 20$ 

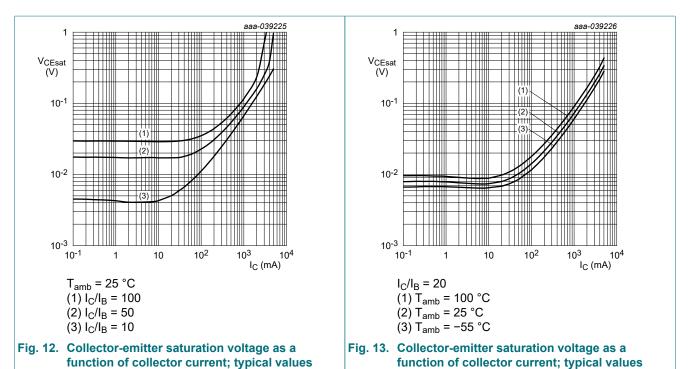
(1)  $T_{amb} = -55$  °C

(2)  $T_{amb} = 25 \, ^{\circ}C$ 

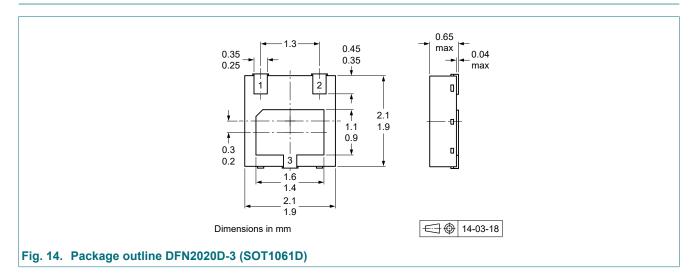
(3)  $T_{amb} = 100 \, ^{\circ}C$ 

Fig. 11. Base-emitter saturation voltage as a function of collector current; typical values

### 50 V, 3 A PNP low VCEsat transistor

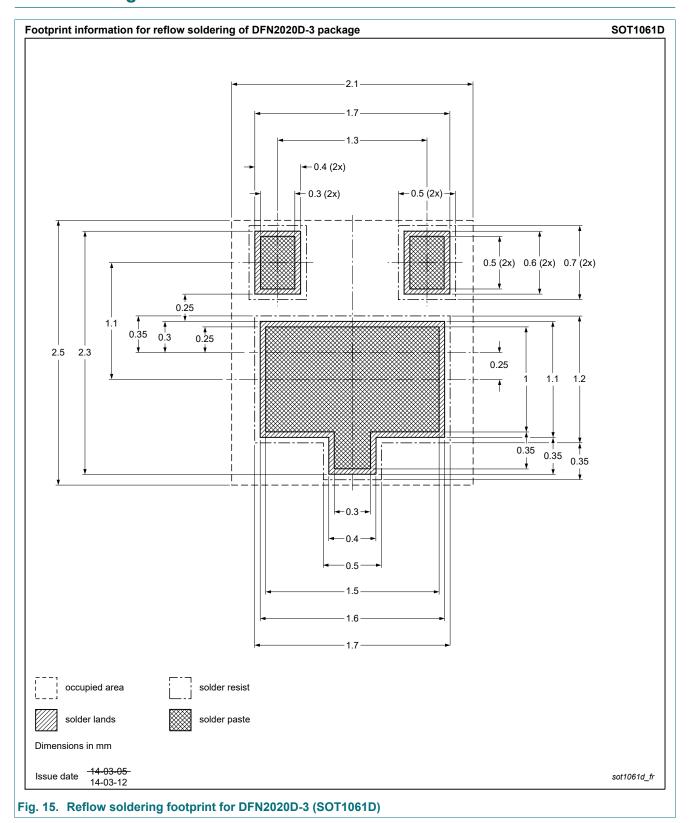


# 11. Package outline



50 V, 3 A PNP low VCEsat transistor

# 12. Soldering



50 V, 3 A PNP low VCEsat transistor

# 13. Revision history

### **Table 8. Revision history**

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PBSS4350PAS v.1	20240516	Product data sheet	-	-

## 50 V, 3 A PNP low VCEsat transistor

## 14. Legal information

#### **Data sheet status**

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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# PBSS4350PAS

## 50 V, 3 A PNP low VCEsat transistor

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