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Kind regards,

Team Nexperia
PBSS2515YPN
15 V low $V_{CE(sat)}$ NPN/PNP transistor

Product data sheet
Supersedes data of 2002 May 08
FEATURES

- Low collector-emitter saturation voltage
- High current capability
- Replaces two SC-70 packaged low $V_{CE_{sat}}$ transistors on same PCB area
- Reduces required PCB area
- Reduced pick and place costs.

APPLICATION

- General purpose switching and muting
- Low frequency driver circuits
- LCD backlighting
- Supply line switching circuits
- Battery driven equipment (mobile phones, video cameras and hand-held devices).

DESCRIPTION

NPN/PNP low $V_{CE_{sat}}$ transistor pair in a SC-88 plastic package.

MARKING

<table>
<thead>
<tr>
<th>TYPE NUMBER</th>
<th>MARKING CODE</th>
</tr>
</thead>
<tbody>
<tr>
<td>PBSS2515YPN</td>
<td>N8*</td>
</tr>
</tbody>
</table>

Note
1. *=: made in Hong Kong
2. *=: made in Malaysia

QUICK REFERENCE DATA

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MAX.</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CEO}$</td>
<td>collector-emitter voltage</td>
<td>15</td>
<td>V</td>
</tr>
<tr>
<td>$I_{CM}$</td>
<td>peak collector current</td>
<td>1</td>
<td>A</td>
</tr>
<tr>
<td>$R_{CE_{sat}}$</td>
<td>equivalent on-resistance</td>
<td>&lt;500</td>
<td>mΩ</td>
</tr>
</tbody>
</table>

PINNING

<table>
<thead>
<tr>
<th>PIN</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1, 4</td>
<td>emitter TR1; TR2</td>
</tr>
<tr>
<td>2, 5</td>
<td>base TR1; TR2</td>
</tr>
<tr>
<td>6, 3</td>
<td>collector TR1; TR2</td>
</tr>
</tbody>
</table>

Fig.1  Simplified outline SC-88 (SOT363) and symbol.

ORDERING INFORMATION

<table>
<thead>
<tr>
<th>TYPE NUMBER</th>
<th>PACKAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>PBSS2515YPN</td>
<td>SC-88 plastic surface mounted package; 6 leads</td>
</tr>
<tr>
<td></td>
<td>VERSION</td>
</tr>
<tr>
<td></td>
<td>SOT363</td>
</tr>
</tbody>
</table>
## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN.</th>
<th>MAX.</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Per transistor; for the PNP transistor with negative polarity</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{CBO}$</td>
<td>collector-base voltage</td>
<td>open emitter</td>
<td>–</td>
<td>15</td>
<td>V</td>
</tr>
<tr>
<td>$V_{CEO}$</td>
<td>collector-emitter voltage</td>
<td>open base</td>
<td>–</td>
<td>15</td>
<td>V</td>
</tr>
<tr>
<td>$V_{EBO}$</td>
<td>emitter-base voltage</td>
<td>open collector</td>
<td>–</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>$I_C$</td>
<td>collector current (DC)</td>
<td></td>
<td>–</td>
<td>500</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{CM}$</td>
<td>peak collector current</td>
<td></td>
<td>–</td>
<td>1</td>
<td>A</td>
</tr>
<tr>
<td>$I_{BM}$</td>
<td>peak base current</td>
<td></td>
<td>–</td>
<td>100</td>
<td>mA</td>
</tr>
<tr>
<td>$P_{tot}$</td>
<td>total power dissipation</td>
<td>$T_{amb} \leq 25 , ^\circ C$</td>
<td>–</td>
<td>200</td>
<td>mW</td>
</tr>
<tr>
<td>$T_{stg}$</td>
<td>storage temperature</td>
<td></td>
<td>–65</td>
<td>+150</td>
<td>°C</td>
</tr>
<tr>
<td>$T_J$</td>
<td>junction temperature</td>
<td></td>
<td>–</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>$T_{amb}$</td>
<td>operating ambient temperature</td>
<td></td>
<td>–65</td>
<td>+150</td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td>Per device</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$P_{tot}$</td>
<td>total power dissipation</td>
<td>$T_{amb} \leq 25 , ^\circ C$; note 1</td>
<td>–</td>
<td>300</td>
<td>mW</td>
</tr>
</tbody>
</table>

**Note**

1. Transistor mounted on an FR4 printed-circuit board.

## THERMAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{th(j-a)}$</td>
<td>thermal resistance from junction to ambient</td>
<td>note 1</td>
<td>416</td>
<td>K/W</td>
</tr>
</tbody>
</table>

**Note**

1. Transistor mounted on an FR4 printed-circuit board.
CHARACTERISTICS

\( T_{\text{amb}} = 25 \, ^\circ\text{C} \) unless otherwise specified.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_{\text{CBO}} )</td>
<td>collector-base cut-off current</td>
<td>( V_{\text{CB}} = 15 , \text{V} ); ( I_{\text{E}} = 0 , \text{A} )</td>
<td>–</td>
<td>–</td>
<td>100</td>
<td>nA</td>
</tr>
<tr>
<td>( I_{\text{EBO}} )</td>
<td>emitter-base cut-off current</td>
<td>( V_{\text{EB}} = 5 , \text{V} ); ( I_{\text{C}} = 0 , \text{A} )</td>
<td>–</td>
<td>–</td>
<td>100</td>
<td>nA</td>
</tr>
<tr>
<td>( h_{\text{FE}} )</td>
<td>DC current gain</td>
<td>( V_{\text{CE}} = 2 , \text{V} ); ( I_{\text{C}} = 10 , \text{mA} )</td>
<td>200</td>
<td>–</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td>( V_{\text{CEsat}} )</td>
<td>collector-emitter saturation voltage</td>
<td>( I_{\text{C}} = 10 , \text{mA} ); ( I_{\text{B}} = 0.5 , \text{mA} )</td>
<td>–</td>
<td>–</td>
<td>25</td>
<td>mV</td>
</tr>
<tr>
<td>( R_{\text{CEsat}} )</td>
<td>equivalent on-resistance</td>
<td>( I_{\text{C}} = 500 , \text{mA} ); ( I_{\text{B}} = 50 , \text{mA} ); note 1</td>
<td>–</td>
<td>300</td>
<td>&lt;500</td>
<td>mΩ</td>
</tr>
<tr>
<td>( V_{\text{BEon}} )</td>
<td>base-emitter turn-on voltage</td>
<td>( V_{\text{CE}} = 2 , \text{V} ); ( I_{\text{C}} = 100 , \text{mA} ); note 1</td>
<td>–</td>
<td>–</td>
<td>0.9</td>
<td>V</td>
</tr>
</tbody>
</table>

**NPN transistor**

\( f_T \) | transition frequency | \( I_{\text{C}} = 100 \, \text{mA} \); \( V_{\text{CE}} = 5 \, \text{V} \); \( f = 100 \, \text{MHz} \) | 250 | 420 | – | MHz |

\( C_{\text{c}} \) | collector capacitance | \( V_{\text{CB}} = 10 \, \text{V} \); \( I_{\text{E}} = I_{\text{E}} = 0 \, \text{A} \); \( f = 1 \, \text{MHz} \) | – | 4.4 | 6 | pF |

**PNP transistor**

\( f_T \) | transition frequency | \( I_{\text{C}} = -100 \, \text{mA} \); \( V_{\text{CE}} = -5 \, \text{V} \); \( f = 100 \, \text{MHz} \) | 100 | 280 | – | MHz |

\( C_{\text{c}} \) | collector capacitance | \( V_{\text{CB}} = -10 \, \text{V} \); \( I_{\text{E}} = I_{\text{E}} = 0 \, \text{A} \); \( f = 1 \, \text{MHz} \) | – | – | 10 | pF |

**Note**

1. Pulse test: \( t_p \leq 300 \, \mu\text{s} \); \( \delta \leq 0.02 \).
15 V low $V_{CE(sat)}$ NPN/PNP transistor

**Fig. 2** DC current gain as a function of collector current; typical values.

**Fig. 3** Base-emitter voltage as a function of collector current; typical values.

**Fig. 4** Collector-emitter saturation voltage as a function of collector current; typical values.

**Fig. 5** Base-emitter saturation voltage as a function of collector current; typical values.
15 V low $V_{CE(sat)}$ NPN/PNP transistor

**Fig. 6** Equivalent on-resistance as a function of collector current; typical values.

**TR1 (NPN) $I_C/I_B = 20$.**

(1) $T_{\text{amb}} = 150^\circ C$.

(2) $T_{\text{amb}} = 25^\circ C$.

(3) $T_{\text{amb}} = -55^\circ C$.

**Fig. 7** Collector current as a function of collector-emitter voltage; typical values.

**TR1 (NPN) $T_{\text{amb}} = 25^\circ C$.**

(1) $I_B = 4.6 \text{ mA}$.

(2) $I_B = 4.14 \text{ mA}$.

(3) $I_B = 3.68 \text{ mA}$.

(4) $I_B = 3.22 \text{ mA}$.

(5) $I_B = 2.76 \text{ mA}$.

(6) $I_B = 2.3 \text{ mA}$.

(7) $I_B = 1.84 \text{ mA}$.

(8) $I_B = 1.38 \text{ mA}$.

(9) $I_B = 0.92 \text{ mA}$.

(10) $I_B = 0.46 \text{ mA}$.
15 V low $V_{CE(sat)}$ NPN/PNP transistor

**Fig. 8** DC current gain as a function of collector current; typical values.

TR2 (PNP) $V_{CE} = -2$ V.
(1) $T_{amb} = 150$ °C.
(2) $T_{amb} = 25$ °C.
(3) $T_{amb} = -55$ °C.

**Fig. 9** Base-emitter voltage as a function of collector current; typical values.

TR2 (PNP) $V_{CE} = -2$ V.
(1) $T_{amb} = -55$ °C.
(2) $T_{amb} = 25$ °C.
(3) $T_{amb} = 150$ °C.

**Fig. 10** Collector-emitter saturation voltage as a function of collector current; typical values.

TR2 (PNP) $I_C/I_B = 20$.
(1) $T_{amb} = 150$ °C.
(2) $T_{amb} = 25$ °C.
(3) $T_{amb} = -55$ °C.

**Fig. 11** Base-emitter saturation voltage as a function of collector current; typical values.

TR2 (PNP) $I_C/I_B = 20$.
(1) $T_{amb} = 150$ °C.
(2) $T_{amb} = 25$ °C.
(3) $T_{amb} = -55$ °C.
15 V low $V_{CE(sat)}$ NPN/PNP transistor

**PBSS2515YPN**

---

**TR2 (PNP) $I_C/I_B = 20.$**

1. $T_{\text{amb}} = 150 \, ^\circ\text{C}.$
2. $T_{\text{amb}} = 25 \, ^\circ\text{C}.$
3. $T_{\text{amb}} = -55 \, ^\circ\text{C}.$

---

**TR2 (PNP) $T_{\text{amb}} = 25 \, ^\circ\text{C}.$**

1. $I_B = -7 \, \text{mA}.$
2. $I_B = -6.3 \, \text{mA}.$
3. $I_B = -5.6 \, \text{mA}.$
4. $I_B = -4.9 \, \text{mA}.$
5. $I_B = -4.2 \, \text{mA}.$
6. $I_B = -3.5 \, \text{mA}.$
7. $I_B = -2.8 \, \text{mA}.$
8. $I_B = -2.1 \, \text{mA}.$
9. $I_B = -1.4 \, \text{mA}.$
10. $I_B = -0.7 \, \text{mA}.$

---

**Fig. 12** Equivalent on-resistance as a function of collector current; typical values.

**Fig. 13** Collector current as a function of collector-emitter voltage; typical values.
15 V low $V_{CE(sat)}$ NPN/PNP transistor PBSS2515YPN

PACKAGE OUTLINE

Plastic surface-mounted package; 6 leads

UNIT A $A_1$ max $b_D$ c D E e $e_1$ $H_E$ $L_p$ Q v w y

<table>
<thead>
<tr>
<th>UNIT</th>
<th>A</th>
<th>$A_1$ max</th>
<th>$b_D$</th>
<th>c</th>
<th>D</th>
<th>E</th>
<th>e</th>
<th>$e_1$</th>
<th>$H_E$</th>
<th>$L_p$</th>
<th>Q</th>
<th>v</th>
<th>w</th>
<th>y</th>
</tr>
</thead>
<tbody>
<tr>
<td>mm</td>
<td>1.1</td>
<td>0.1</td>
<td>0.30</td>
<td>0.25</td>
<td>2.2</td>
<td>1.35</td>
<td>1.15</td>
<td>0.65</td>
<td>2.2</td>
<td>0.45</td>
<td>0.25</td>
<td>0.2</td>
<td>0.2</td>
<td>0.1</td>
</tr>
<tr>
<td>0.8</td>
<td></td>
<td>0.1</td>
<td>0.20</td>
<td>0.10</td>
<td>1.8</td>
<td>1.35</td>
<td>1.15</td>
<td>0.65</td>
<td>2.0</td>
<td>0.15</td>
<td>0.25</td>
<td>0.2</td>
<td>0.2</td>
<td></td>
</tr>
</tbody>
</table>

REFERENCES

IEC     JEDEC  JEITA
SOT363  SC-88

EUROPEAN PROJECTION ISSUE DATE

04-11-08
06-03-16
15 V low $V_{CE(sat)}$ NPN/PNP transistor PBSS2515YPN

DATA SHEET STATUS

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</tr>
</thead>
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<td>Objective data sheet</td>
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<td>This document contains data from the objective specification for product development.</td>
</tr>
<tr>
<td>Preliminary data sheet</td>
<td>Qualification</td>
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</tr>
<tr>
<td>Product data sheet</td>
<td>Production</td>
<td>This document contains the product specification.</td>
</tr>
</tbody>
</table>

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