



20 October 2023

Product data sheet

1. General description

PNP low V_{CEsat} transistor and NPN Resistor- Equipped Transistor (RET) in a SOT457 (SC-74) small Surface-Mounted Device (SMD) plastic package.

2. Features and benefits

- Low V_{CEsat} and resistor-equipped transistor in one package
- Low threshold voltage (<1 V) compared to MOSFET
- · Space-saving solution
- Reduction of component count
- AEC-Q101 qualified

3. Applications

- Supply line switches
- Battery charger switches
- · High-side switches for LEDs, drivers and backlights
- Portable equipment

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
TR1; PNP le	ow V _{CEsat} transistor						
V _{CEO}	collector-emitter voltage	open base		-	-	-60	V
I _C	collector current			-	-	-1.5	А
I _{CM}	peak collector current	$t_p \le 1 \text{ ms}; \text{ single pulse}$		-	-	-3	А
R _{CEsat}	collector-emitter saturation resistance	I_{C} = -1500 mA; I_{B} = -100 mA; T_{amb} = 25 °C	[1]	-	110	175	mΩ
TR2; NPN r	esistor-equipped transisto	br	l				
V _{CEO}	collector-emitter voltage	open base		-	-	50	V
lo	output current			-	-	100	mA
R1	bias resistor 1 (input)		[2]	15.4	22	28.6	kΩ
R2/R1	bias resistor ratio		[2]	0.8	1	1.2	

[1] Pulse test: $t_p \le 300 \ \mu s$; $\delta \le 0.02$

[2] See "Section 11: Test information" for resistor calculation and test conditions.

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5. Pinning information

Table 2. Pinning information						
Symbol	Description	Simplified outline	Graphic symbol			
B1	base TR1		6 5 4			
12	input (base) TR2					
O2	output (collector) TR2					
GND	GND (emitter) TR2					
C1	collector TR1					
E1	emitter TR1	TSOP6 (SOT457)				
			1 1 1 1 2 3 006aab506			
	Symbol B1 I2 O2 GND C1	SymbolDescriptionB1base TR1I2input (base) TR2O2output (collector) TR2GNDGND (emitter) TR2C1collector TR1	SymbolDescriptionSimplified outlineB1base TR1I2input (base) TR2O2output (collector) TR2GNDGND (emitter) TR2C1collector TR1			

6. Ordering information

Table 3. Ordering information					
Type number	Package				
	Name	Description	Version		
PBLS6024D	TSOP6	plastic, surface-mounted package (SC-74; TSOP6); 6 leads	<u>SOT457</u>		

7. Marking

Table 4. Marking codes	
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Type number	Marking code
PBLS6024D	КН

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

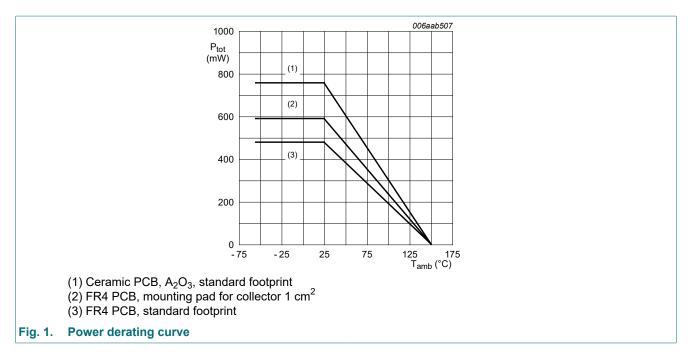
Symbol	Parameter	Conditions		Min	Max	Unit
TR1; PNP lo	w V _{CEsat} transistor					
V _{CBO}	collector-base voltage	open emitter		-	-60	V
V _{CEO}	collector-emitter voltage	open base		-	-60	V
V _{EBO}	emitter-base voltage	open collector		-	-5	V
I _C	collector current			-	-1.5	А
I _{CM}	peak collector current	$t_p \le 1 \text{ ms}; \text{ single pulse}$		-	-3	А
I _B	base current			-	-300	mA
I _{BM}	peak base current	single pulse; t _p ≤ 1 ms		-	-1000	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	370	mW
			[2]	-	480	mW
			[3]	-	630	mW
TR2; NPN re	sistor-equipped transistor	1	I			
V _{CBO}	collector-base voltage	open emitter		-	50	V
V _{CEO}	collector-emitter voltage	open base		-	50	V
V _{EBO}	emitter-base voltage	open collector		-	10	V
VI	input voltage	positive		-	40	V
		negative		-	-10	V
lo	output current			-	100	mA
I _{CM}	peak collector current	t _p ≤ 1 ms; single pulse		-	100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1] [2] [3]	-	200	mW
Per device						
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	480	mW
			[2]	-	590	mW
			[3]	-	760	mW
Tj	junction temperature			-	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided, 35 µm copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm².

[3] Device mounted on a ceramic PCB, Al₂O₃, standard footprint.

60 V, 1.5 A PNP loadswitch



9. Thermal characteristics

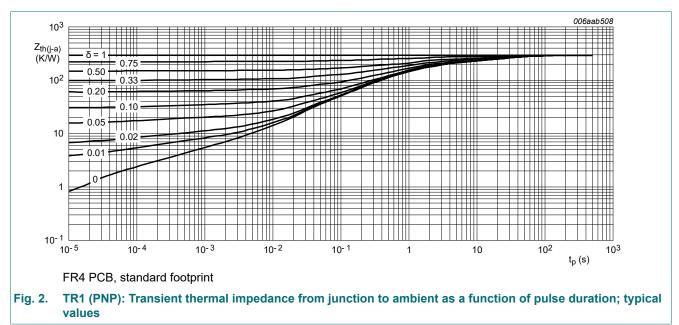
Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Тур	Мах	Unit
Per device			·		·		
R _{th(j-a)} thermal resistance from junction to ambient	in free air [1]	[1]	-	-	260	K/W	
	junction to ambient		[2]	-	-	211	K/W
		[3]	-	-	165	K/W	
R _{th(j-sp)}	thermal resistance from junction to solder point			-	-	100	K/W

[1] Device mounted on an FR4 PCB, single-sided, 35 µm copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm².

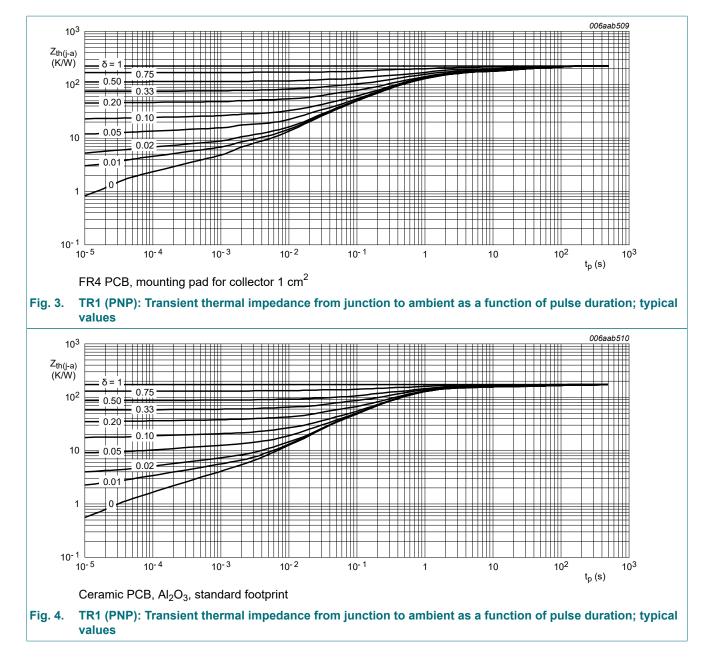
[3] Device mounted on a ceramic PCB, Al₂O₃, standard footprint.



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10. Characteristics

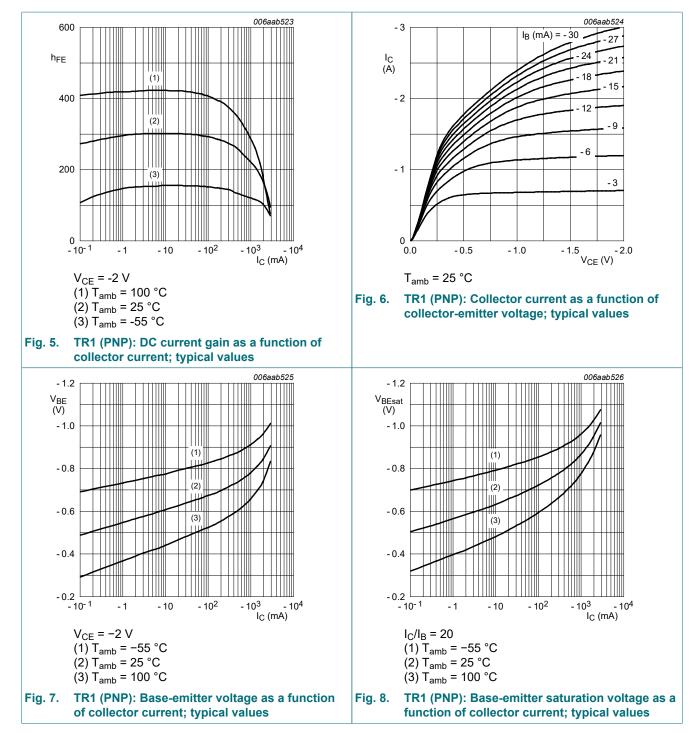
Symbol	Parameter	Conditions		Min	Тур	Max	Unit
TR1; PNP lo	w V _{CEsat} transistor	1					
I _{CBO}	collector-base cut-off	V _{CB} = -60 V; I _E = 0 A; T _{amb} = 25 °C		-	-	-100	nA
	current	V _{CB} = -60 V; I _E = 0 A; T _i = 150 °C		-	-	-50	μA
I _{CES}	collector-emitter cut-off current	$V_{CE} = -48 \text{ V}; \text{ T}_{amb} = 25 \text{ °C}; \text{ V}_{BE} = 0 \text{ A}$		-	-	-100	nA
I _{EBO}	emitter-base cut-off current	V _{EB} = -5 V; I _C = 0 A; T _{amb} = 25 °C		-	-	-100	nA
h _{FE}	DC current gain	V _{CE} = -2 V; I _C = -100 mA; T _{amb} = 25 °C		180	285	-	
		V _{CE} = -2 V; I _C = -500 mA; T _{amb} = 25 °C	[1]	150	255	-	
		V _{CE} = -2 V; I _C = -1 A; T _{amb} = 25 °C	[1]	140	210	-	
		V _{CE} = -2 V; I _C = -1.5 A; T _{amb} = 25 °C	[1]	120	185	-	
V _{CEsat}	collector-emitter	$I_B = -50 \text{ mA}; T_{amb} = 25 \text{ °C}; I_C = -0.5 \text{ A}$	[1]	-	-65	-100	mV
	saturation voltage	I _B = -50 mA; T _{amb} = 25 °C; I _C = -1 A	[1]	-	-130	-200	mV
		$I_B = -100 \text{ mA}; T_{amb} = 25 \text{ °C}; I_C = -1 \text{ A}$	[1]	-	-110	-170	mV
		$I_B = -100 \text{ mA}; T_{amb} = 25 \text{ °C}; I_C = -1.5 \text{ A}$	[1]	-	-165	-260	mV
R _{CEsat}	CEsat collector-emitter saturation resistance	$I_{C} = -1000 \text{ mA}; I_{B} = -100 \text{ mA}; T_{amb} = 25 \text{ °C}$	[1]	-	110	170	mΩ
		I _C = -1500 mA; I _B = -100 mA; T _{amb} = 25 °C	[1]	-	110	175	mΩ
V _{BEsat}	base-emitter saturation	I _C = -500 mA; I _B = -50 mA; T _{amb} = 25 °C	[1]	-	-0.85	-1	V
	voltage	I _C = -1500 mA; I _B = -100 mA; T _{amb} = 25 °C	[1]	-	-0.93	-1.1	V
V _{BEon}	base-emitter turn-on voltage	V _{CE} = -10 V; I _C = -1000 mA; T _{amb} = 25 °C	[1]	-	-0.75	-1.1	V
d	delay time	V _{CC} = -10 V; I _C = -1 A; I _{Bon} = -50 mA;		-	17	-	ns
r	rise time	I _{Boff} = 50 mA; T _{amb} = 25 °C		-	38	-	ns
on	turn-on time			-	55	-	ns
s	storage time			-	350	-	ns
f	fall time			-	65	-	ns
off	turn-off time	-		-	415	-	ns
C _c	collector capacitance	V _{CB} = -10 V; I _E = 0 A; i _e = 0 A; f = 1 MHz; T _{amb} = 25 °C		-	30	-	pF
fT	transition frequency	V_{CE} = -10 V; I _C = -50 mA; f = 100 MHz; T _{amb} = 25 °C		-	150	-	MHz
TR2; NPN re	sistor-equipped transistor						
СВО	collector-base cut-off current	$V_{CB} = 50 \text{ V}; \text{ I}_{\text{E}} = 0 \text{ A}; \text{ T}_{\text{amb}} = 25 ^{\circ}\text{C}$		-	-	100	nA
CEO	collector-emitter cut-off	V _{CE} = 30 V; I _B = 0 A; T _{amb} = 25 °C		-	-	1	μA
	current	V _{CE} = 30 V; I _B = 0 A; T _j = 150 °C		-	-	50	μA
EBO	emitter-base cut-off current	$V_{EB} = 5 \text{ V}; I_C = 0 \text{ A}; T_{amb} = 25 \text{ °C}$		-	-	180	μA
٦ _{FE}	DC current gain	V _{CE} = 5 V; I _C = 5 mA; T _{amb} = 25 °C		60	-	-	
V _{CEsat}	collector-emitter saturation voltage	$I_{\rm C}$ = 10 mA; $I_{\rm B}$ = 0.5 mA; $T_{\rm amb}$ = 25 °C		-	-	150	mV

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Symbol	Parameter	Conditions		Min	Тур	Мах	Unit
V _{I(off)}	off-state input voltage	V_{CE} = 5 V; I _C = 100 µA; T _{amb} = 25 °C		-	1.1	0.8	V
V _{I(on)}	on-state input voltage	V_{CE} = 0.3 V; I _C = 5 mA; T _{amb} = 25 °C		2.5	1.7	-	V
R1	bias resistor 1 (input)		[2]	15.4	22	28.6	kΩ
R2/R1	bias resistor ratio		[2]	0.8	1	1.2	
C _c	collector capacitance	V_{CB} = 10 V; I _E = 0 A; i _e = 0 A; f = 1 MHz; T _{amb} = 25 °C		-	-	2.5	pF

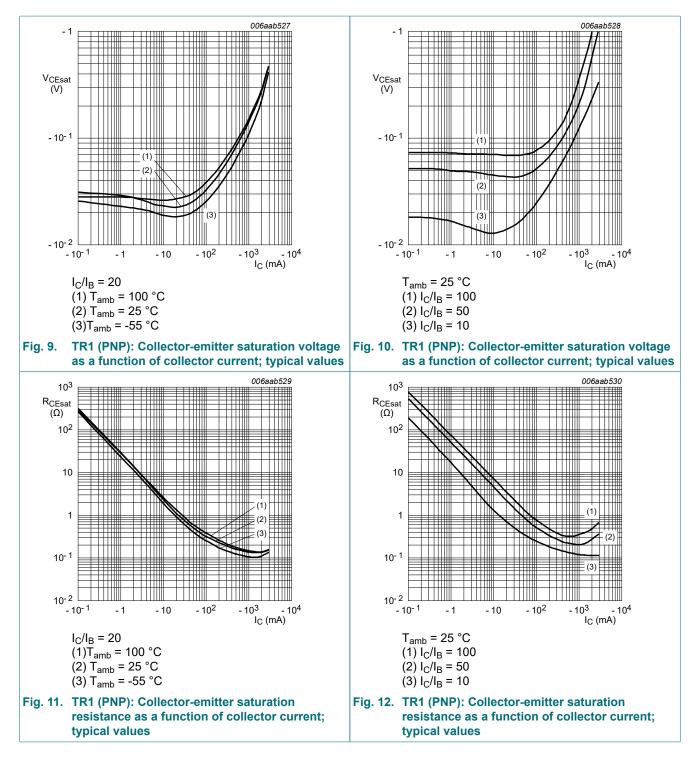
[1] Pulse test: $t_p \le 300 \ \mu s$; $\delta \le 0.02$

[2] See "Section 11: Test information" for resistor calculation and test conditions.

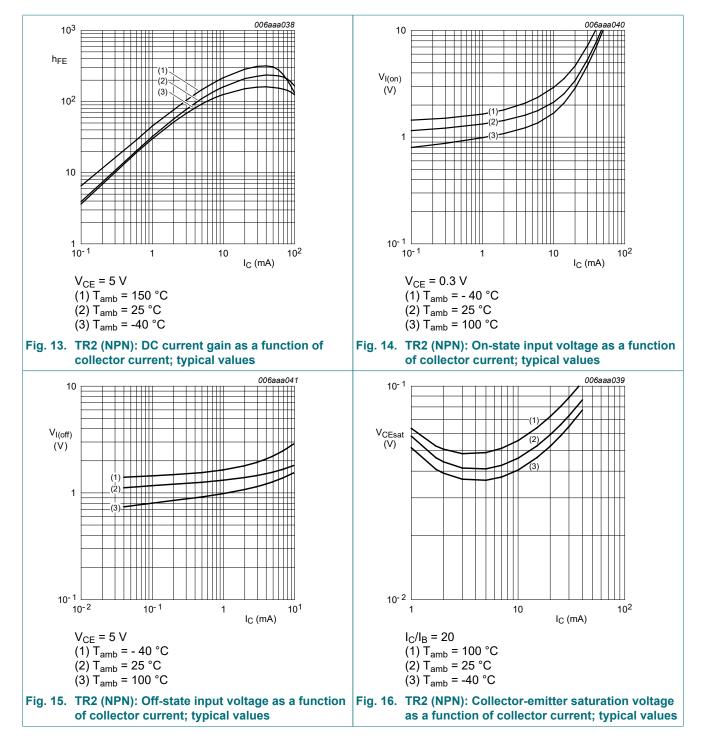


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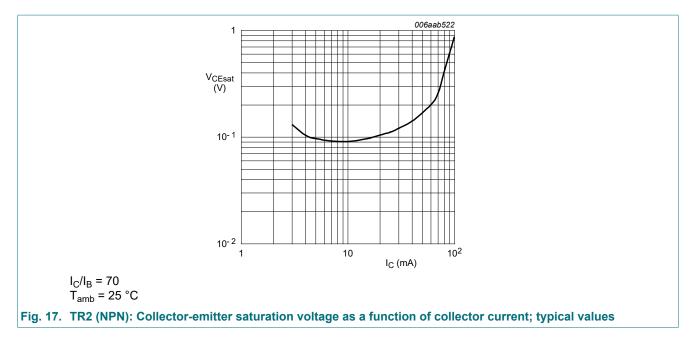
60 V, 1.5 A PNP loadswitch



60 V, 1.5 A PNP loadswitch

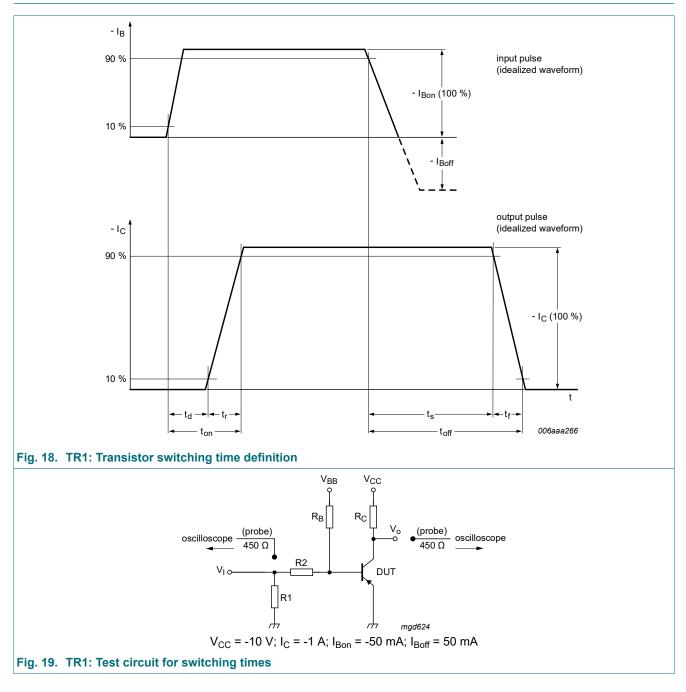


60 V, 1.5 A PNP loadswitch



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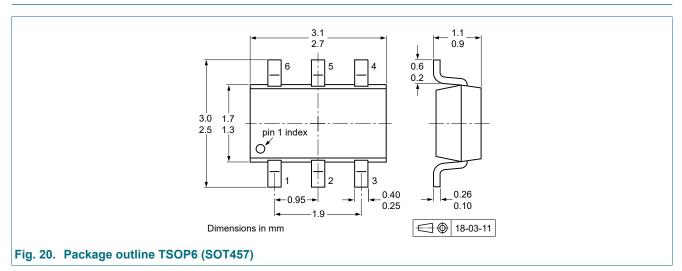
11. Test information



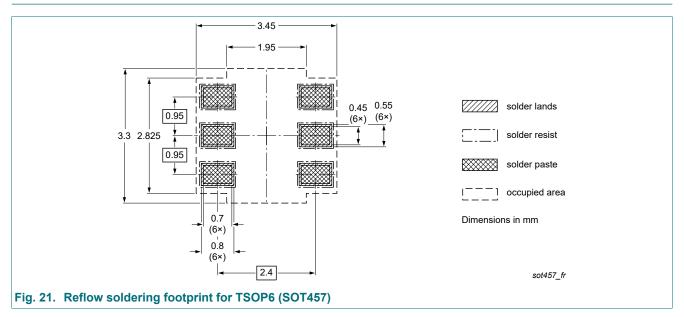
Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101* - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

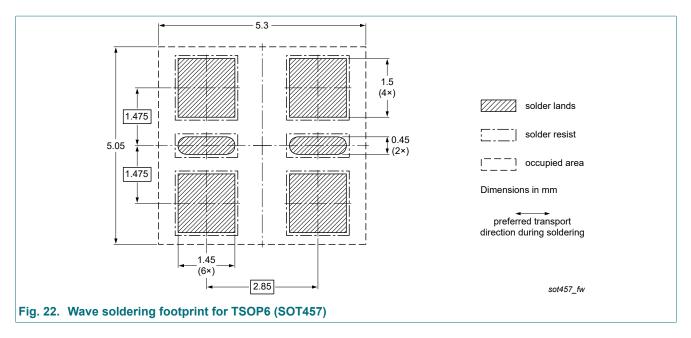


13. Soldering



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14. Revision history

Table 8. Revision history							
Data sheet ID	Release date	Data sheet status	Change notice	Supersedes			
PBLS6024D v.2	20231020	Product data sheet	-	PBLS6024D_1			
Modifications:	Nexperia. • Legal texts have b	The format of this data sheet has been redesigned to comply with the identity guidelines of					
PBLS6024D_1	20090814	Product data sheet	-	-			

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15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

 Please consult the most recently issued document before initiating or completing a design.

- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <u>https://www.nexperia.com</u>.

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