



PBL4003Y-Q

40 V 500 mA PNP/NPN loadswitch double transistor

1 June 2023

Product data sheet

1. General description

PNP low V_{CEsat} transistor and NPN Resistor- Equipped Transistor (RET) in a very small SOT363 (SC-88) Surface-Mounted Device (SMD) plastic package.

2. Features and benefits

- Low V_{CEsat} and resistor-equipped transistor in one package
- Low threshold voltage (<1 V) compared to MOSFET
- Low drive power required
- Space-saving solution
- Reduction of component count
- Qualified according to AEC-Q101 and recommended for use in automotive applications

3. Applications

- Supply line switches
- Battery charger switches
- High-side switches for LEDs, drivers and backlights
- Portable equipment

4. Quick reference data

Table 1. Quick reference data

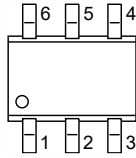
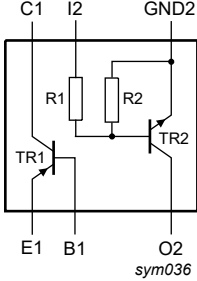
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TR1; PNP low V_{CEsat} transistor						
V_{CEO}	collector-emitter voltage	open base	-	-	-40	V
I_C	collector current		-	-	-500	mA
R_{CEsat}	collector-emitter saturation resistance	$I_C = -500$ mA; $I_B = -50$ mA; $T_{amb} = 25$ °C [1]	-	440	700	m Ω
TR2; NPN resistor-equipped transistor						
V_{CEO}	collector-emitter voltage	open base	-	-	50	V
I_O	output current		-	-	100	mA
R1	bias resistor 1 (input)	[2]	7	10	13	k Ω
R2/R1	bias resistor ratio	[2]	0.8	1	1.2	

[1] Pulse test: $t_p \leq 300$ μ s; $\delta \leq 0.02$

[2] See "Section 11: Test information" for resistor calculation and test conditions.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	E1	emitter TR1	 <p>TSSOP6 (SOT363)</p>	
2	B1	base TR1		
3	O2	output (collector) TR2		
4	GND2	GND (emitter) TR2		
5	I2	input (base) TR2		
6	C1	collector TR1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PBL54003Y-Q	TSSOP6	plastic, surface-mounted package; 6 leads; 0.65 mm pitch; 2.1 mm x 1.25 mm x 0.95 mm body	SOT363

7. Marking

Table 4. Marking codes

Type number	Marking code ^[1]
PBL54003Y-Q	S3%

[1] % = placeholder for manufacturing site code

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
TR1; PNP low V_{CEsat} transistor					
V_{CBO}	collector-base voltage	open emitter	-	-40	V
V_{CEO}	collector-emitter voltage	open base	-	-40	V
V_{EBO}	emitter-base voltage	open collector	-	-6	V
I_C	collector current		-	-500	mA
I_{CM}	peak collector current	$t_p \leq 1$ ms; single pulse	-	-1	A
I_B	base current		-	-50	mA
I_{BM}	peak base current	single pulse; $t_p \leq 1$ ms	-	-100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	200	mW
TR2; NPN resistor-equipped transistor					
V_{CBO}	collector-base voltage	open emitter	-	50	V
V_{CEO}	collector-emitter voltage	open base	-	50	V
V_{EBO}	emitter-base voltage	open collector	-	10	V
V_i	input voltage	positive	-	40	V
		negative	-	-10	V
I_O	output current		-	100	mA
I_{CM}	peak collector current	$t_p \leq 1$ ms; single pulse	-	100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	200	mW
Per device					
P_{tot}	total power dissipation		-	300	mW
T_j	junction temperature		-	150	°C
T_{amb}	ambient temperature		-65	150	°C
T_{stg}	storage temperature		-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided, 35 μ m copper, tin-plated and standard footprint.

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per device						
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	416	K/W

[1] Device mounted on an FR4 PCB, single-sided, 35 μ m copper, tin-plated and standard footprint.

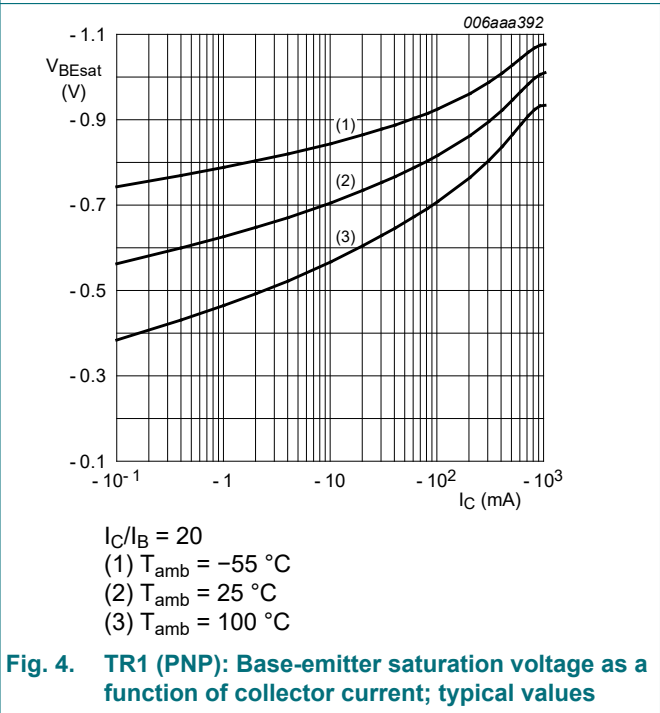
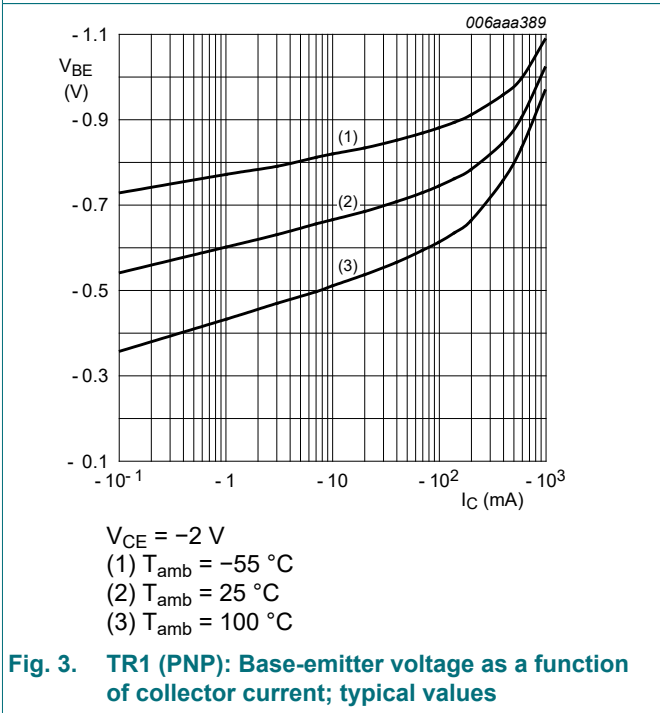
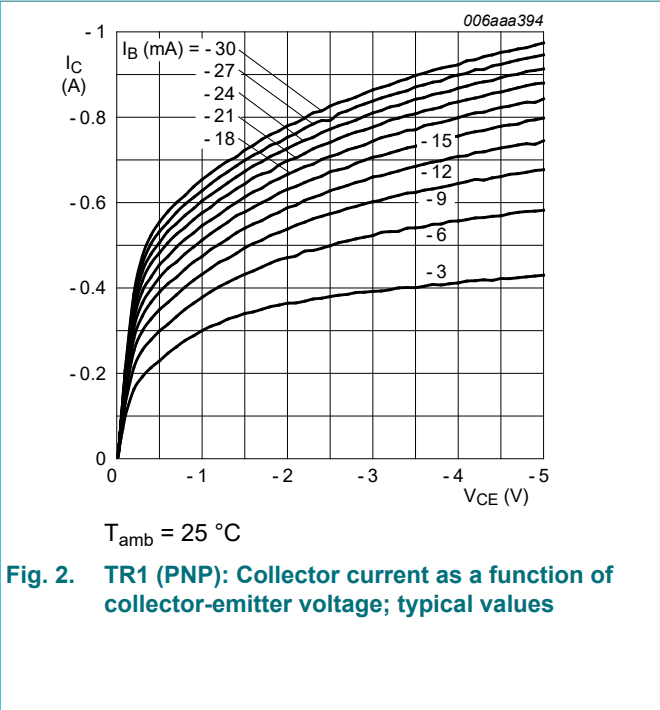
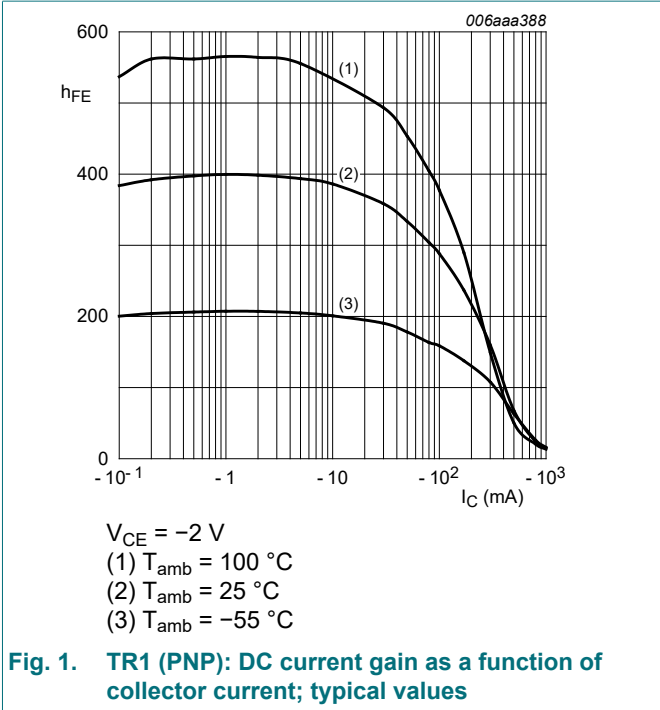
10. Characteristics

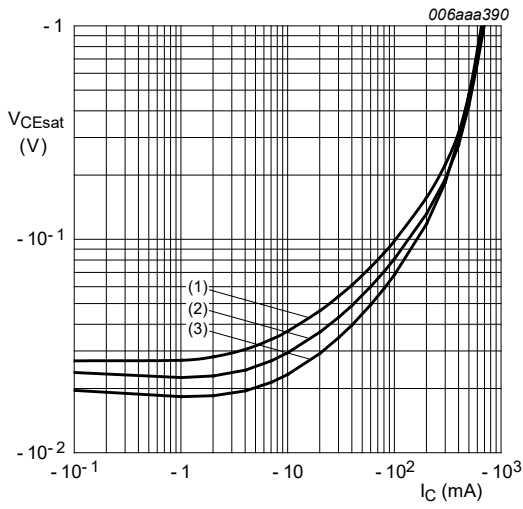
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
TR1; PNP low V_{CEsat} transistor							
I_{CBO}	collector-base cut-off current	$V_{CB} = -40\text{ V}; I_E = 0\text{ A}; T_{amb} = 25\text{ }^\circ\text{C}$	-	-	-100	nA	
		$V_{CB} = -40\text{ V}; I_E = 0\text{ A}; T_j = 150\text{ }^\circ\text{C}$	-	-	-50	μA	
I_{EBO}	emitter-base cut-off current	$V_{EB} = -5\text{ V}; I_C = 0\text{ A}; T_{amb} = 25\text{ }^\circ\text{C}$	-	-	-100	nA	
h_{FE}	DC current gain	$V_{CE} = -2\text{ V}; I_C = -10\text{ mA}; T_{amb} = 25\text{ }^\circ\text{C}$	200	-	-		
		$V_{CE} = -2\text{ V}; I_C = -100\text{ mA}; T_{amb} = 25\text{ }^\circ\text{C}$ [1]	150	-	-		
		$V_{CE} = -2\text{ V}; I_C = -500\text{ mA}; T_{amb} = 25\text{ }^\circ\text{C}$ [1]	40	-	-		
V_{CEsat}	collector-emitter saturation voltage	$I_C = -10\text{ mA}; I_B = -0.5\text{ mA}; T_{amb} = 25\text{ }^\circ\text{C}$	-	-	-50	mV	
		$I_C = -100\text{ mA}; I_B = -5\text{ mA}; T_{amb} = 25\text{ }^\circ\text{C}$	-	-	-130	mV	
		$I_C = -200\text{ mA}; I_B = -10\text{ mA}; T_{amb} = 25\text{ }^\circ\text{C}$	-	-	-200	mV	
		$I_C = -500\text{ mA}; I_B = -50\text{ mA}; T_{amb} = 25\text{ }^\circ\text{C}$ [1]	-	-	-350	mV	
R_{CEsat}	collector-emitter saturation resistance		[1]	440	700	m Ω	
V_{BEsat}	base-emitter saturation voltage		[1]	-	-1.2	V	
V_{BEon}	base-emitter turn-on voltage	$V_{CE} = -2\text{ V}; I_C = -100\text{ mA}; T_{amb} = 25\text{ }^\circ\text{C}$ [1]	-	-	-1.1	V	
C_c	collector capacitance	$V_{CB} = -10\text{ V}; I_E = 0\text{ A}; i_e = 0\text{ A}; f = 1\text{ MHz}; T_{amb} = 25\text{ }^\circ\text{C}$	-	-	10	pF	
f_T	transition frequency	$V_{CE} = -5\text{ V}; I_C = -100\text{ mA}; f = 100\text{ MHz}; T_{amb} = 25\text{ }^\circ\text{C}$	100	300	-	MHz	
TR2; NPN resistor-equipped transistor							
I_{CBO}	collector-base cut-off current	$V_{CB} = 50\text{ V}; I_E = 0\text{ A}; T_{amb} = 25\text{ }^\circ\text{C}$	-	-	100	nA	
I_{CEO}	collector-emitter cut-off current	$V_{CE} = 30\text{ V}; I_B = 0\text{ A}; T_{amb} = 25\text{ }^\circ\text{C}$	-	-	1	μA	
		$V_{CE} = 30\text{ V}; I_B = 0\text{ A}; T_j = 150\text{ }^\circ\text{C}$	-	-	50	μA	
I_{EBO}	emitter-base cut-off current	$V_{EB} = 5\text{ V}; I_C = 0\text{ A}; T_{amb} = 25\text{ }^\circ\text{C}$	-	-	400	μA	
h_{FE}	DC current gain	$V_{CE} = 5\text{ V}; I_C = 5\text{ mA}; T_{amb} = 25\text{ }^\circ\text{C}$	30	-	-		
V_{CEsat}	collector-emitter saturation voltage	$I_C = 10\text{ mA}; I_B = 0.5\text{ mA}; T_{amb} = 25\text{ }^\circ\text{C}$	-	-	150	mV	
$V_{I(off)}$	off-state input voltage	$V_{CE} = 5\text{ V}; I_C = 100\text{ }\mu\text{A}; T_{amb} = 25\text{ }^\circ\text{C}$	-	1.1	0.8	V	
$V_{I(on)}$	on-state input voltage	$V_{CE} = 0.3\text{ V}; I_C = 10\text{ mA}; T_{amb} = 25\text{ }^\circ\text{C}$	2.5	1.8	-	V	
R1	bias resistor 1 (input)		[2]	7	10	13	k Ω
R2/R1	bias resistor ratio		[2]	0.8	1	1.2	
C_c	collector capacitance	$V_{CB} = 10\text{ V}; I_E = 0\text{ A}; i_e = 0\text{ A}; f = 1\text{ MHz}; T_{amb} = 25\text{ }^\circ\text{C}$	-	-	2.5	pF	

[1] Pulse test: $t_p \leq 300\text{ }\mu\text{s}$; $\delta \leq 0.02$

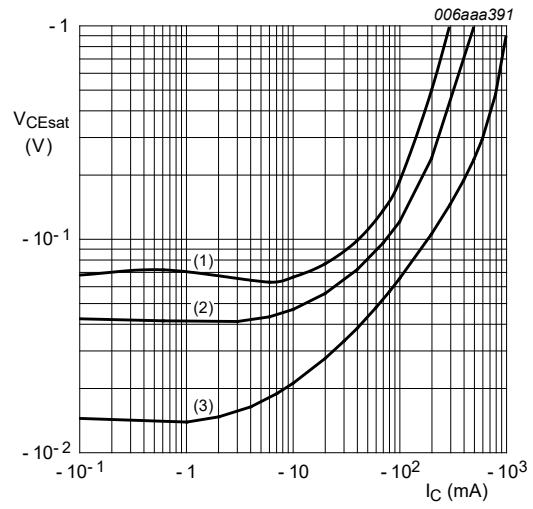
[2] See "Section 11: Test information" for resistor calculation and test conditions.





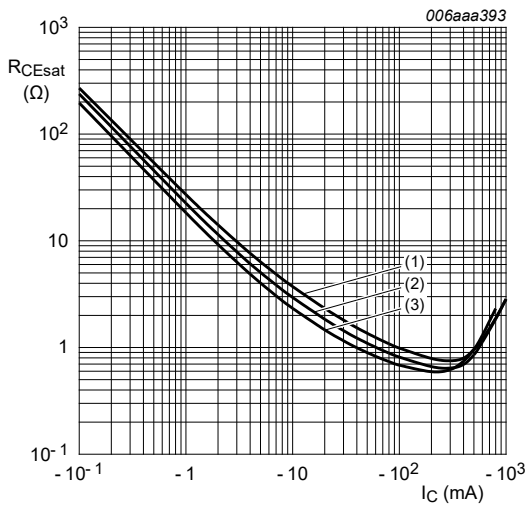
$I_C/I_B = 20$
 (1) $T_{amb} = 100\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = -55\text{ °C}$

Fig. 5. TR1 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values



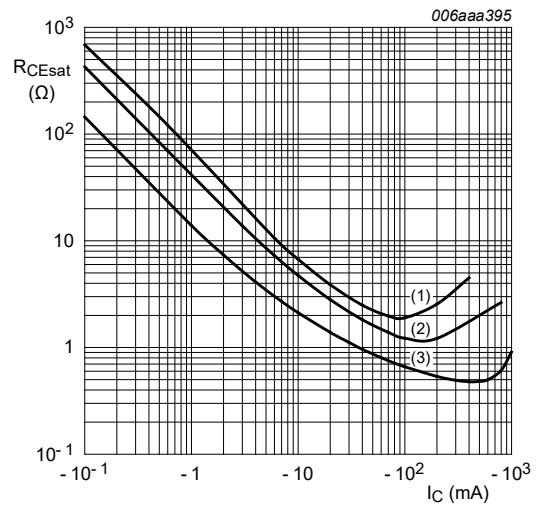
$T_{amb} = 25\text{ °C}$
 (1) $I_C/I_B = 100$
 (2) $I_C/I_B = 50$
 (3) $I_C/I_B = 10$

Fig. 6. TR1 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values



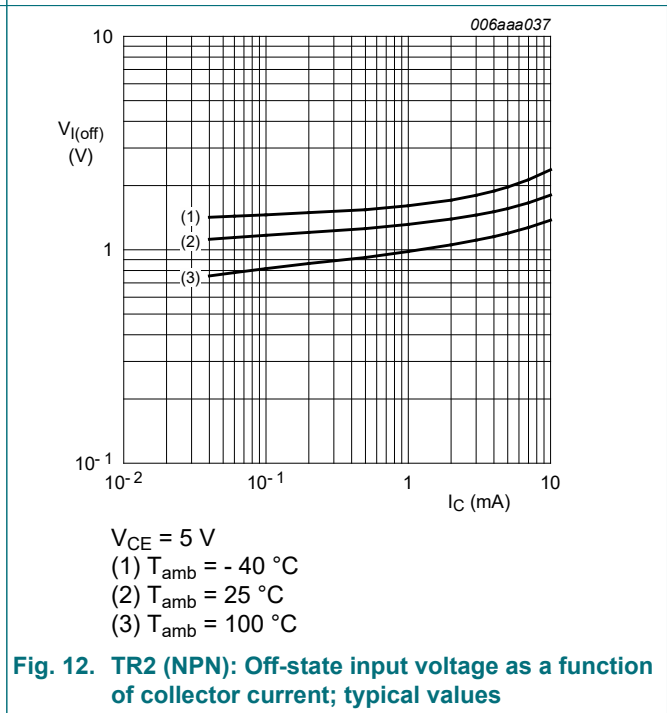
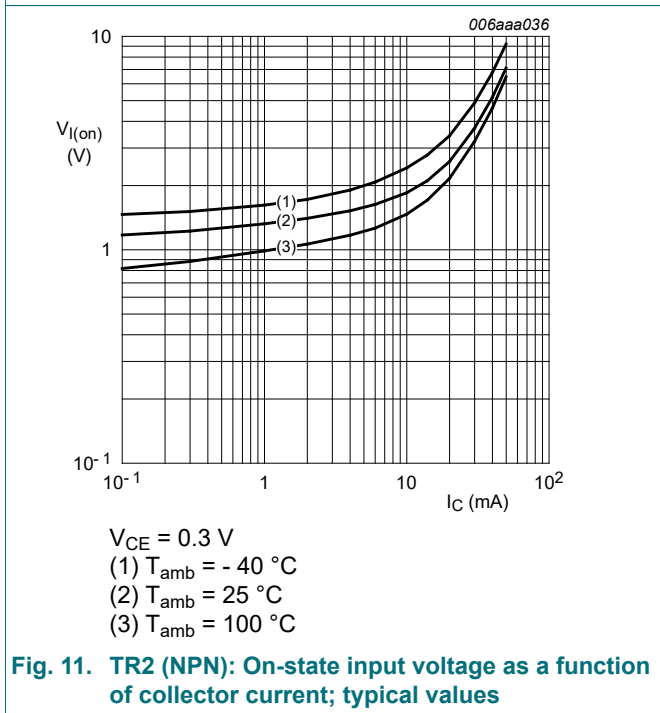
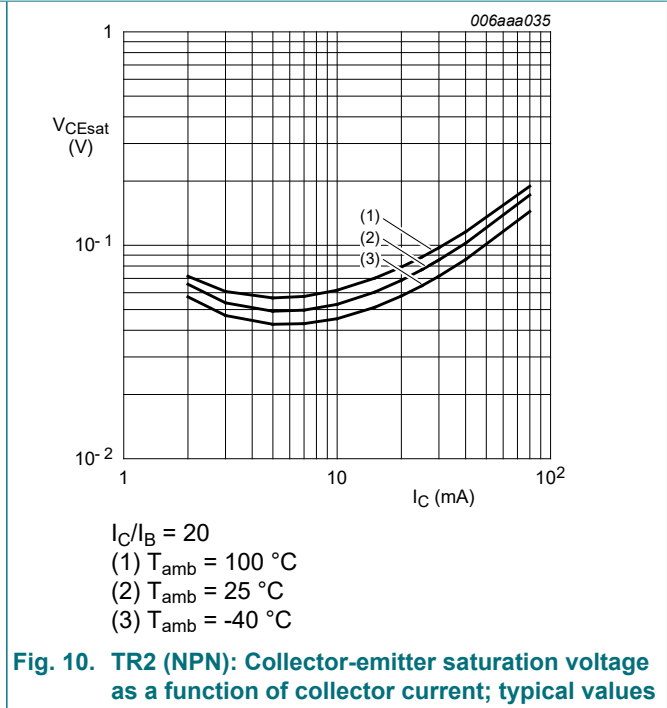
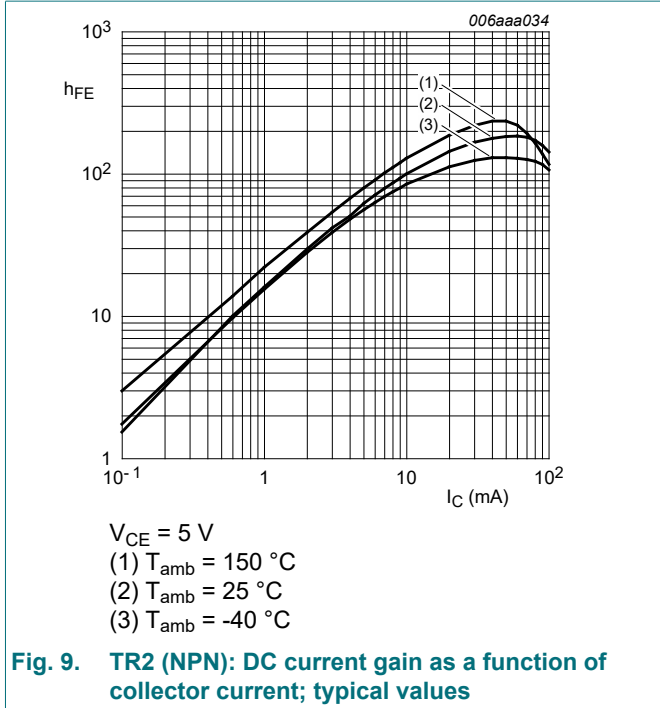
$I_C/I_B = 20$
 (1) $T_{amb} = 100\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = -55\text{ °C}$

Fig. 7. TR1 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values



$T_{amb} = 25\text{ °C}$
 (1) $I_C/I_B = 100$
 (2) $I_C/I_B = 50$
 (3) $I_C/I_B = 10$

Fig. 8. TR1 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values



11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

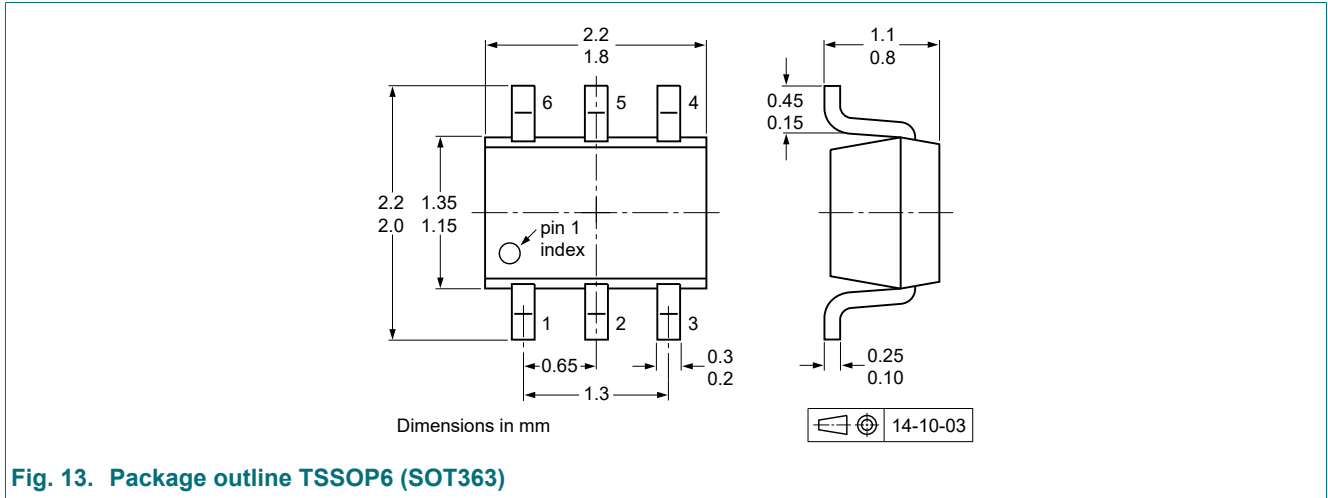


Fig. 13. Package outline TSSOP6 (SOT363)

13. Soldering

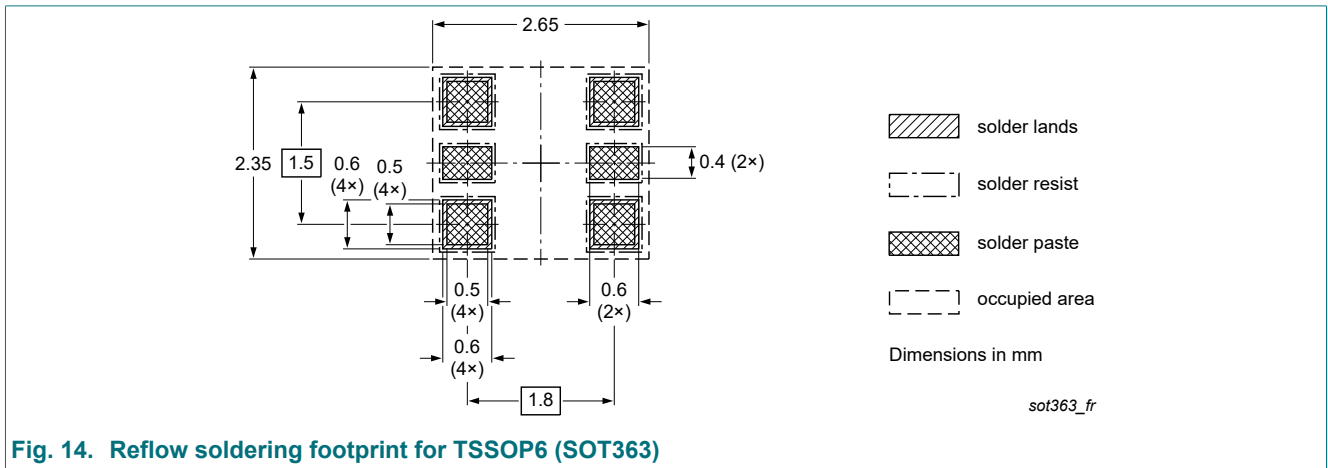


Fig. 14. Reflow soldering footprint for TSSOP6 (SOT363)

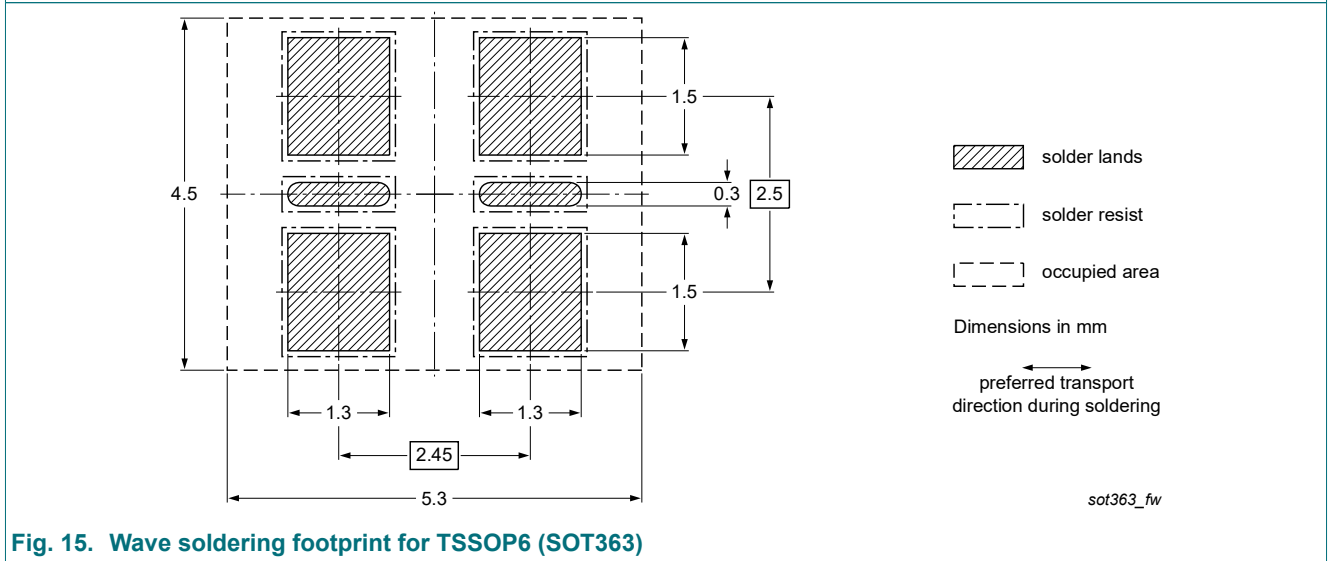


Fig. 15. Wave soldering footprint for TSSOP6 (SOT363)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PBLS4003Y-Q v.1	20230601	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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