

NSF060120T2A0

1200 V, 60 mΩ, N-channel SiC MOSFET

20 May 2026

Product data sheet

1. General description

The NSF060120T2A0 is a Silicon Carbide based 1200 V power MOSFET in a 7-pin X.PAK plastic package for surface mounted, topside-cooled technology. Its excellent R_{DSon} temperature stability, combined with fast switching speed, makes it a product of choice in high power and high voltage industrial applications, such as E-vehicle charging infrastructure, photovoltaic inverters and motor drives.

2. Features and benefits

- Excellent R_{DSon} temperature stability
- Very low switching losses
- Fast reverse recovery
- Fast switching speed
- Temperature independent turn-off switching losses
- Very fast and robust intrinsic body diode
- Faster commutation and improved switching due to the additional Kelvin source pin

3. Applications

- E-vehicle charging infrastructure
- Photovoltaic inverters
- Switch mode power supply
- Uninterruptable power supply
- Motor drives

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
V_{DS}	drain-source voltage		-	-	1200	V	
V_{GS}	gate-source voltage		[1]	-10	-	22	V
I_D	drain current	$T_c = 25\text{ °C}$	[2]	-	-	36	A
		$T_c = 100\text{ °C}$	[2]	-	-	26	A
I_{DM}	peak drain current	pulsed; t_p limited by T_j (max)	[3]	-	-	80	A
Static characteristics							
R_{DSon}	drain-source on-state resistance	$V_{GS} = 18\text{ V}$; $I_D = 20\text{ A}$; $T_j = 25\text{ °C}$	-	60	90	mΩ	

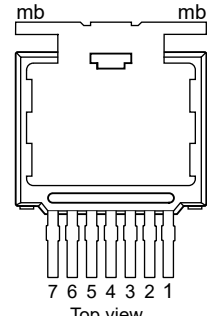
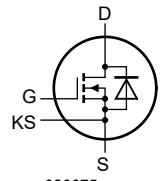
[1] Recommended turn off gate voltage is -5 V to 0 V. Recommended turn on gate voltage is 15 V to 18 V. Do not use with $V_{GSon} < 13\text{ V}$.

[2] Limited by the maximum values of T_j , $R_{th(j-c)}$ and $R_{DSon}(T_j)$.

[3] Designed value (not tested).

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>Top view X.PAK (SOT8107-2)</p>	 <p>aaa-036675</p>
2	KS	Kelvin source		
3 to 7	S	source		
mb	D	connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
NSF060120T2A0	X.PAK	Plastic, surface-mounted Top Side Cooling (TSC) Package; 1.27 mm pitch; 14.0 mm x 11.8 mm x 3.5 mm body	SOT8107-2

7. Marking

Table 4. Marking codes

Type number	Marking code
NSF060120T2A0	NSF060120T2A0

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage			-	1200	V
V_{GS}	gate-source voltage		[1]	-10	22	V
I_D	drain current	$T_c = 25\text{ °C}$	[2]	-	36	A
		$T_c = 100\text{ °C}$	[2]	-	26	A
I_{DM}	peak drain current	pulsed; t_p limited by T_j (max)	[3]	-	80	A
P_{tot}	total power dissipation	$T_c = 25\text{ °C}$	[2]	-	167	W
T_j	junction temperature			-55	175	°C
T_{stg}	storage temperature			-55	150	°C
Source-drain diode						
I_S	source current	$T_c = 25\text{ °C}$	[2]	-	38	A
I_{SM}	peak source current	pulsed; limited by T_j (max)	[3]	-	60	A

[1] Recommended turn off gate voltage is -5 V to 0 V. Recommended turn on gate voltage is 15 V to 18 V. Do not use with $V_{GSon} < 13\text{ V}$.

[2] Limited by the maximum values of T_j , $R_{th(j-c)}$ and $R_{DSon}(T_j)$.

[3] Designed value (not tested).

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-c)}$	thermal resistance from junction to case			-	0.7	0.9	K/W

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 1 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	1200	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 2 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C}$	[1]	2.3	2.9	V
		$I_D = 10 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C}$	[1]	2.77	-	V
I_{DSS}	drain leakage current	$V_{DS} = 1200 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	100	μA
I_{GSS}	gate leakage current	$V_{GS} = 22 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
		$V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 18 \text{ V}; I_D = 20 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	60	90	mΩ
		$V_{GS} = 18 \text{ V}; I_D = 20 \text{ A}; T_j = 175 \text{ }^\circ\text{C}$	-	98	-	mΩ
		$V_{GS} = 15 \text{ V}; I_D = 20 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	80	-	mΩ
		$V_{GS} = 15 \text{ V}; I_D = 20 \text{ A}; T_j = 175 \text{ }^\circ\text{C}$	-	110	-	mΩ
g_{fs}	forward transconductance	$V_{DS} = 10 \text{ V}; I_D = 20 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	9	-	S
$R_{G(int)}$	internal gate resistance	$f = 0.5 \text{ MHz}; T_j = 25 \text{ }^\circ\text{C}$	-	2	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$V_{DD} = 800 \text{ V}; I_D = 20 \text{ A}; V_{GS} = -5/+18 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	57	-	nC
Q_{GS}	gate-source charge		-	25	-	nC
Q_{GD}	gate-drain charge		-	15	-	nC
C_{iss}	input capacitance	$V_{DD} = 800 \text{ V}; f = 0.5 \text{ MHz}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	1335	-	pF
C_{oss}	output capacitance		-	74	-	pF
C_{rss}	reverse transfer capacitance		-	4	-	pF
$t_{d(on)}$	turn-on delay time		$V_{DD} = 800 \text{ V}; I_D = 20 \text{ A}; R_{G(ext)} = 2.2 \text{ }^\circ\Omega; L_L = 82 \text{ }^\circ\mu\text{H}; V_{GS} = -5/+18 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	13	-
t_r	rise time	-		8	-	ns
$t_{d(off)}$	turn-off delay time	-		14	-	ns
t_f	fall time	-		8	-	ns
E_{on}	turn-on switching loss	-		276	-	μJ
E_{off}	turn-off switching loss	-		30	-	μJ
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 20 \text{ A}; V_{GS} = -5 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	4.4	-	V
t_{rr}	reverse recovery time	$V_{DD} = 800 \text{ V}; I_S = 20 \text{ A}; V_{GS} = -5 \text{ V}; dI_S/dt = 7283 \text{ A}/\mu\text{s}; T_j = 25 \text{ }^\circ\text{C}$	-	8	-	ns
Q_r	recovered charge		-	160	-	nC

[1] Measured according to JEP183.

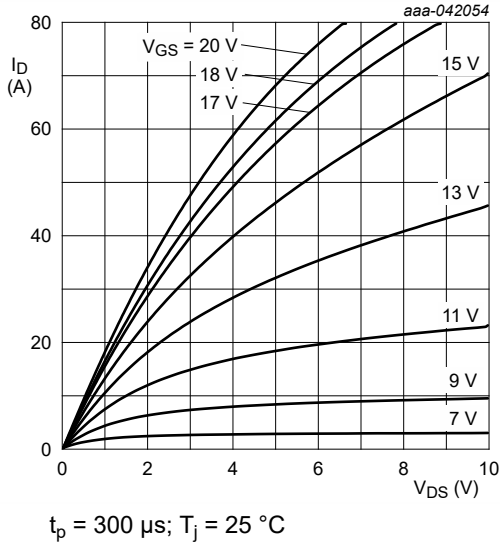


Fig. 1. Output characteristics: drain current as a function of drain-source voltage; typical values

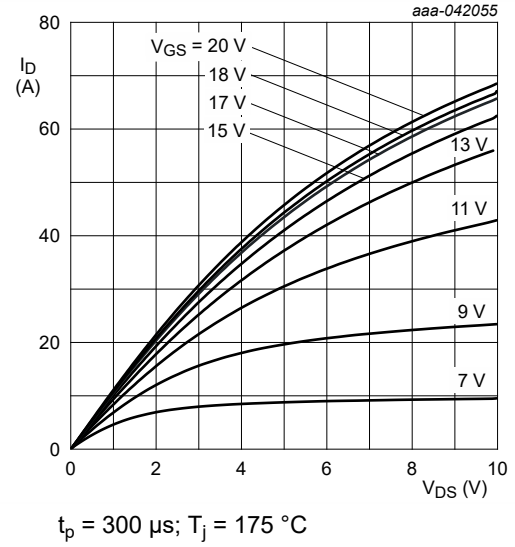


Fig. 2. Output characteristics: drain current as a function of drain-source voltage; typical values

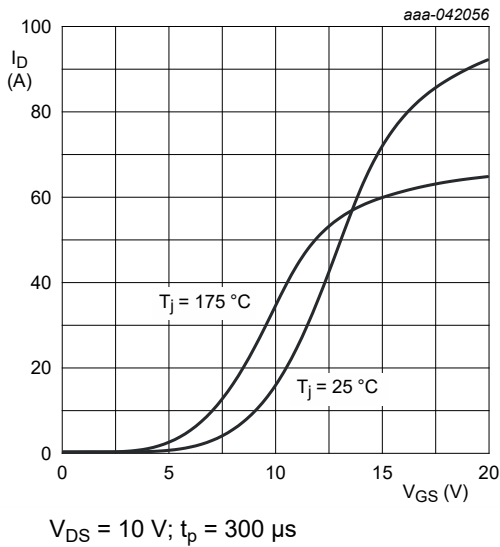


Fig. 3. Transfer characteristics: drain current as a function of gate-source voltage; typical values

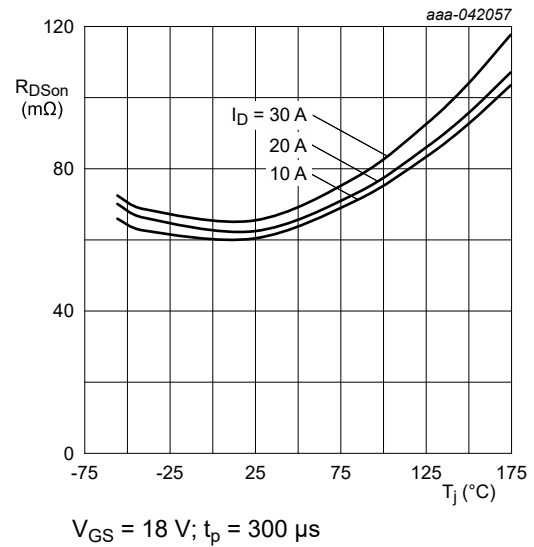


Fig. 4. Drain-source on-state resistance as a function of junction temperature; typical values

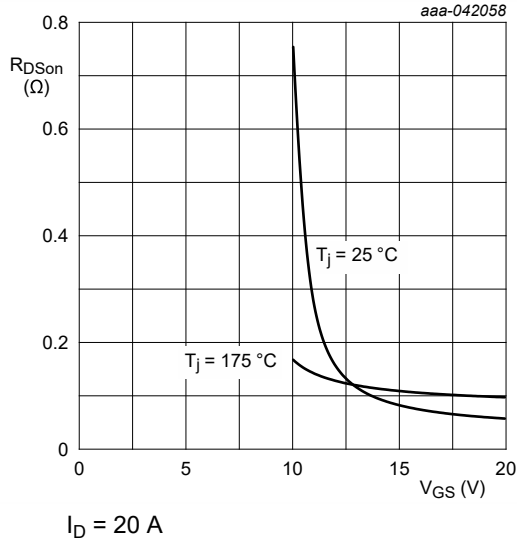


Fig. 5. Drain-source on-state resistance as a function of gate-source voltage

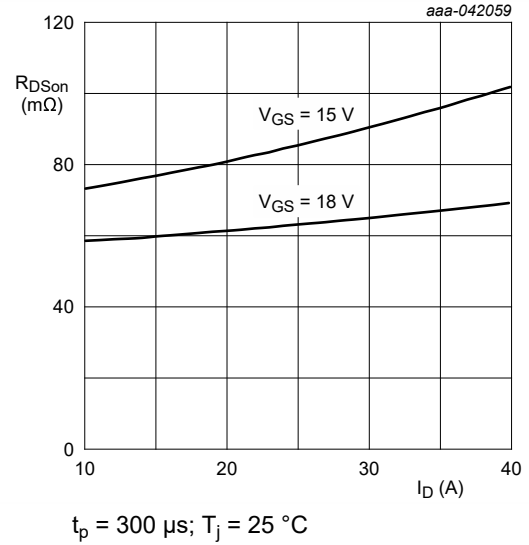


Fig. 6. Drain-source on-state resistance as a function of drain current; typical values

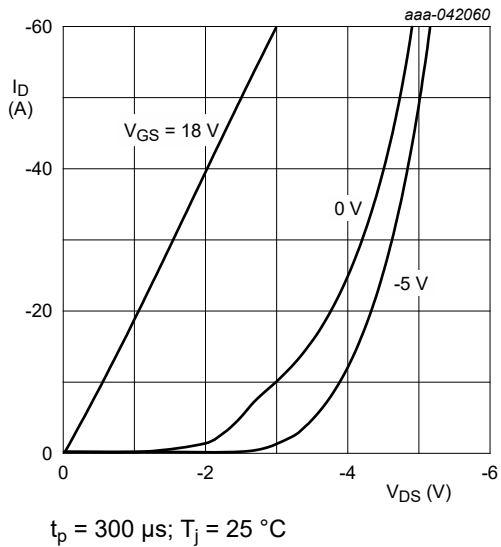


Fig. 7. Drain current as a function of drain-source voltage; typical values (third quadrant characteristics).

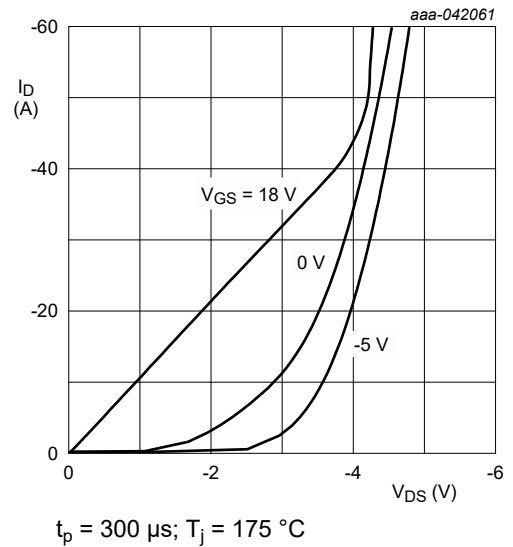


Fig. 8. Drain current as a function of drain-source voltage; typical values (third quadrant characteristics).

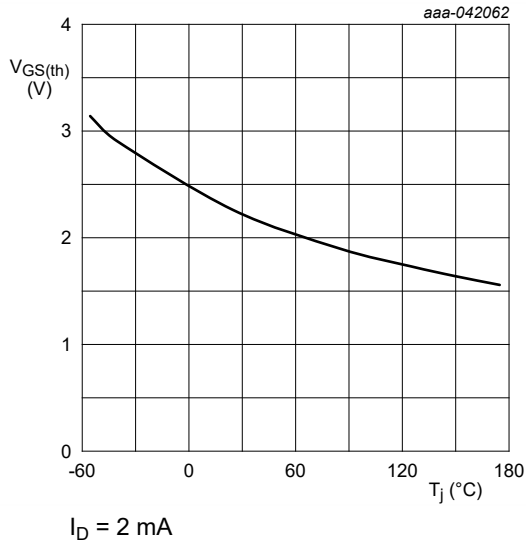


Fig. 9. Gate-source threshold voltage as a function of junction temperature; typical values

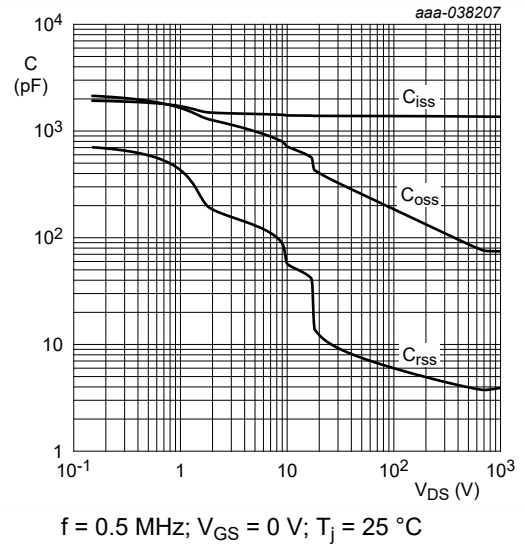


Fig. 10. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

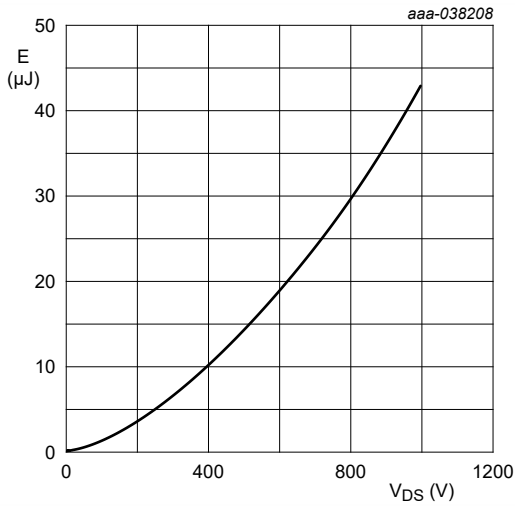


Fig. 11. C_{oss} stored energy as a function of drain-source voltage; typical values

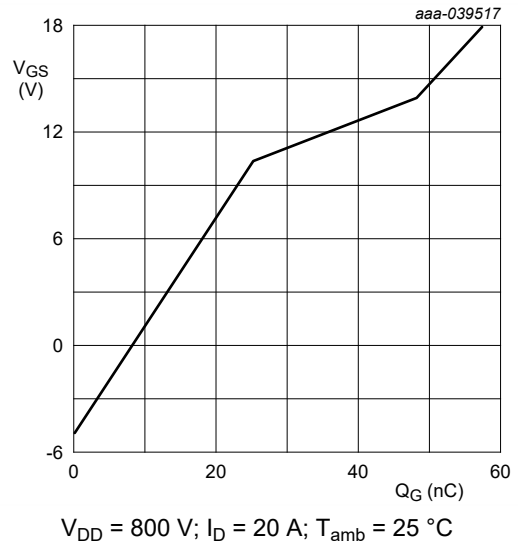


Fig. 12. Gate-source voltage as a function of gate charge; typical values

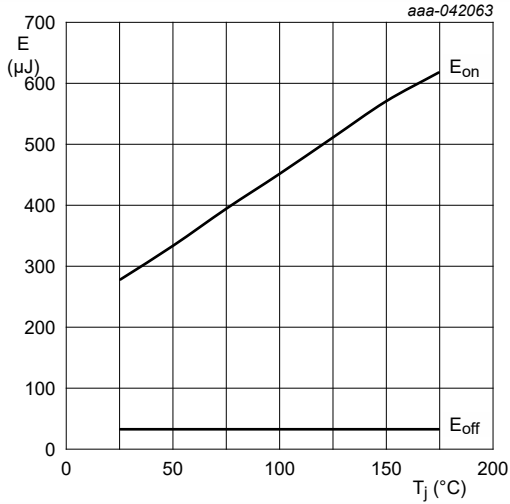


Fig. 13. Switching loss as a function of junction temperature; typical values

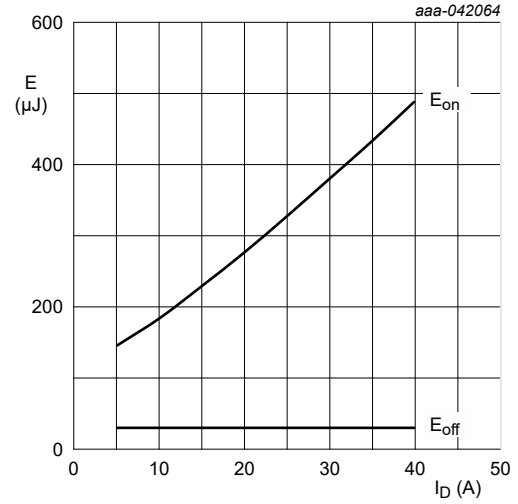


Fig. 14. Switching loss as a function of drain current; typical values

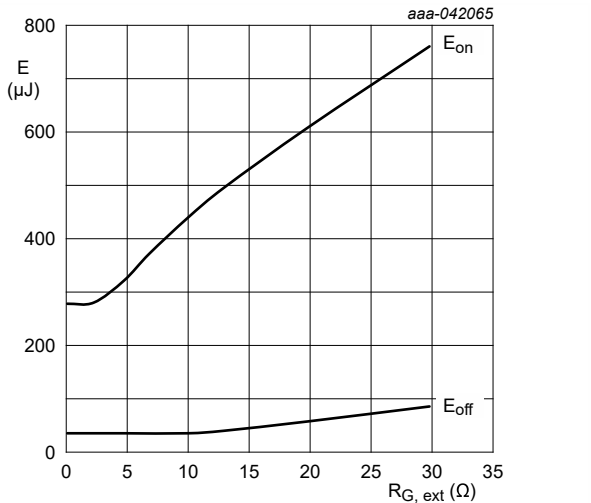


Fig. 15. Switching loss as a function of external gate resistance; typical values

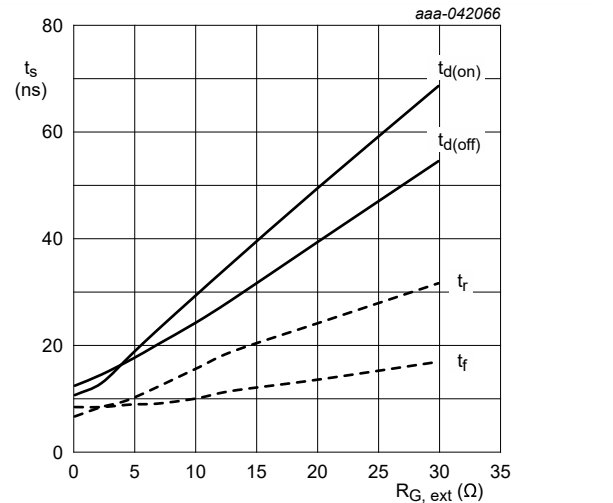


Fig. 16. Switching times as a function of external gate resistance; typical values

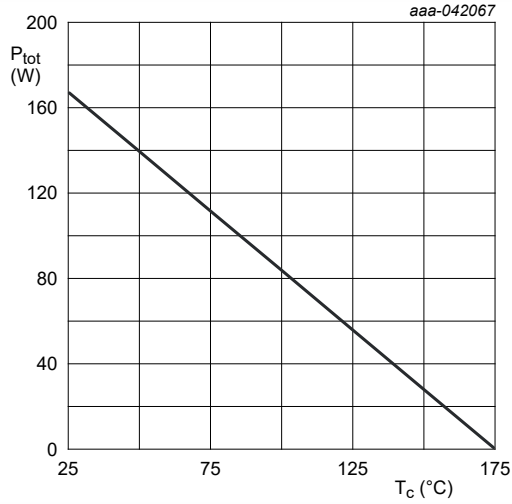


Fig. 17. Power dissipation derating as a function of case temperature; maximum values

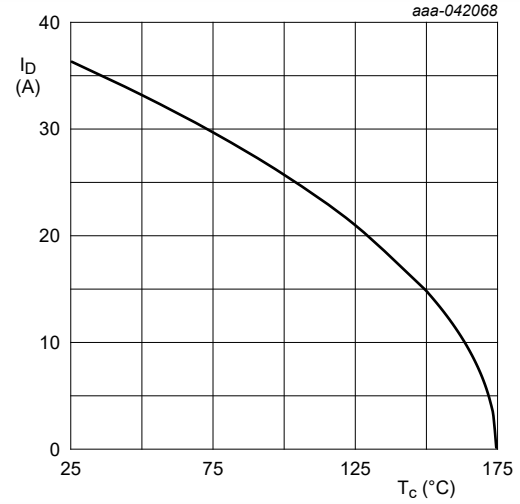
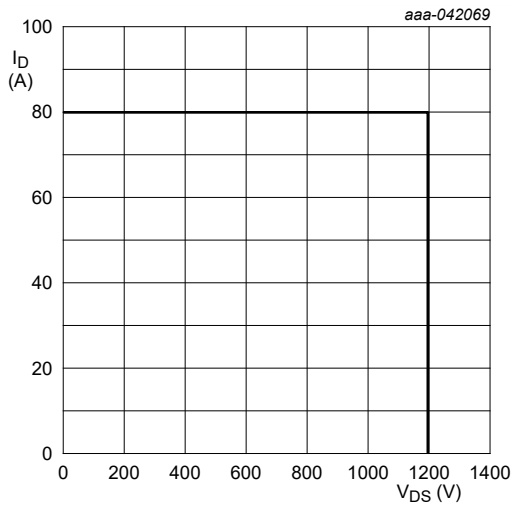


Fig. 18. Continuous drain current as a function of case temperature; maximum values



$V_{GS} = -5/+18$ V; $T_c = 25$ $^{\circ}C$; $T_j \leq 175$ $^{\circ}C$; not for linear use

Fig. 19. Reverse bias safe operating area (RBSOA)

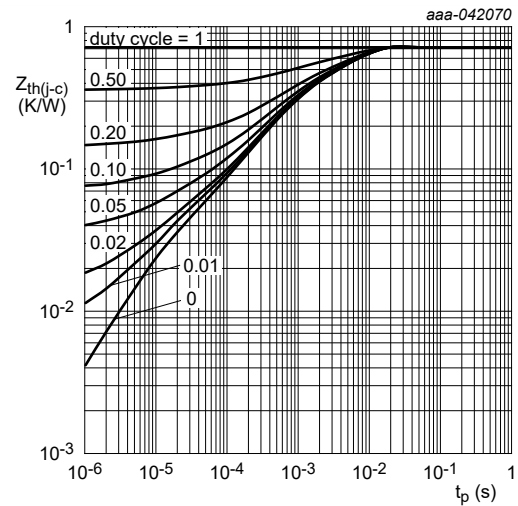


Fig. 20. Transient thermal impedance from junction to case as a function of pulse duration; typical values

11. Test information

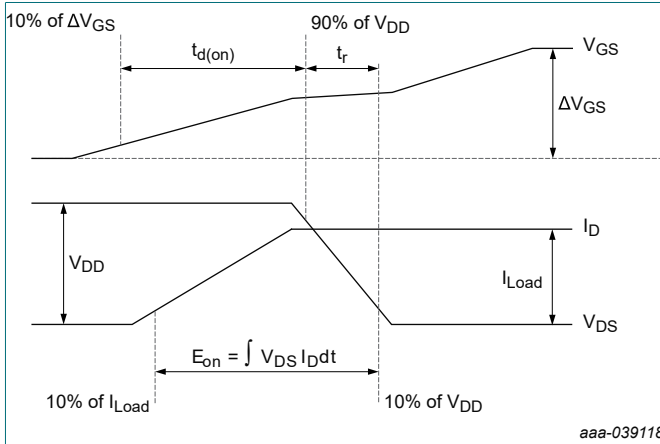


Fig. 21. Definition of switching times and losses during channel turn-on

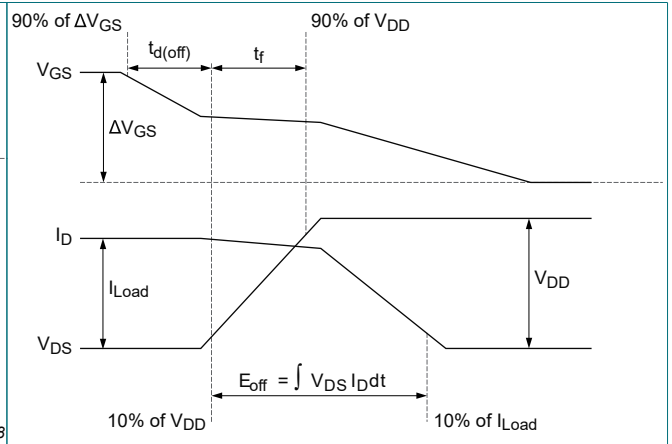


Fig. 22. Definition of switching times and losses during channel turn-off

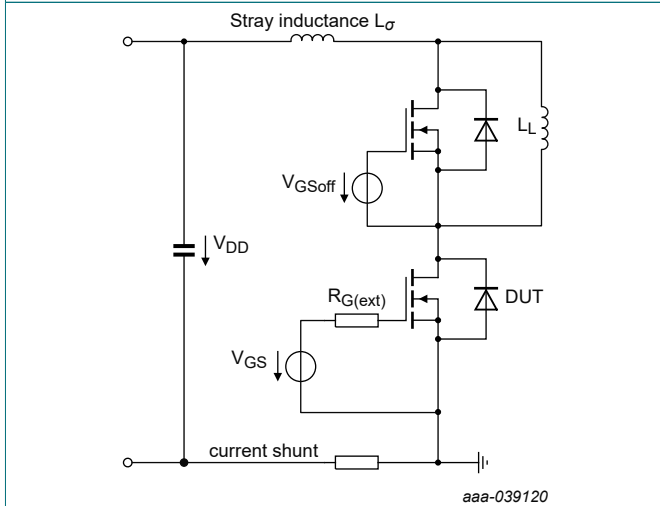


Fig. 23. Test circuit for dynamic characterization of channel and gate charge characteristics

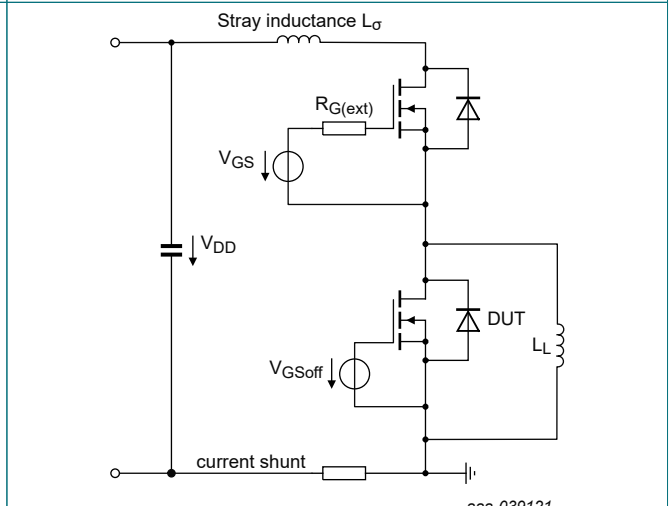


Fig. 24. Test circuit for dynamic characterization of body diode

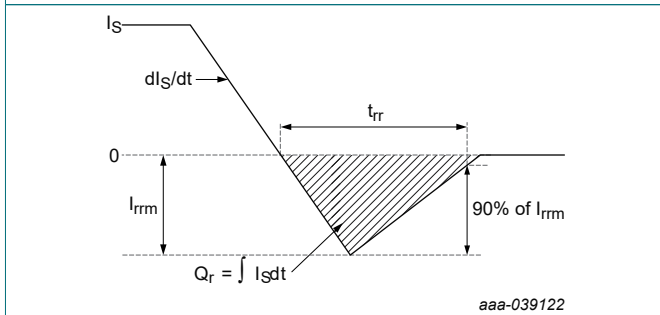


Fig. 25. Definition of dynamic characteristics of body diode

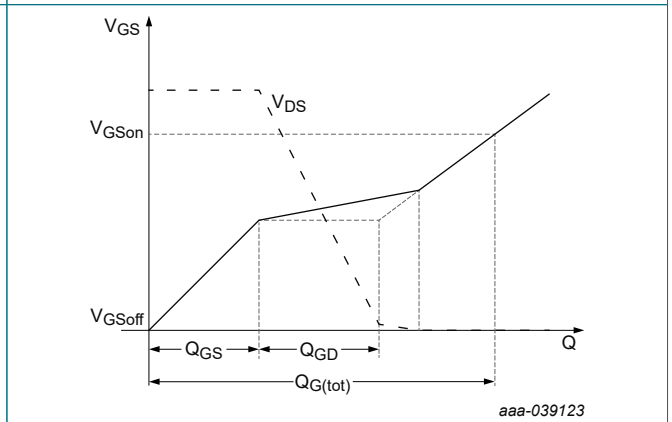
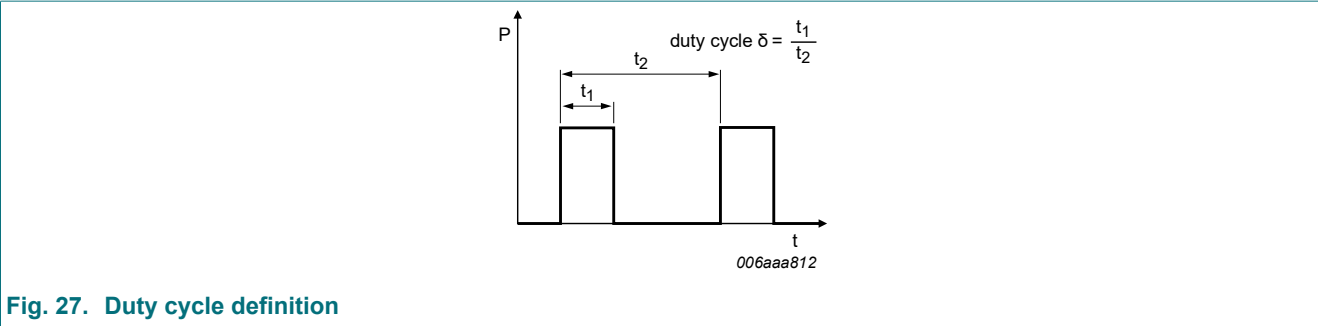


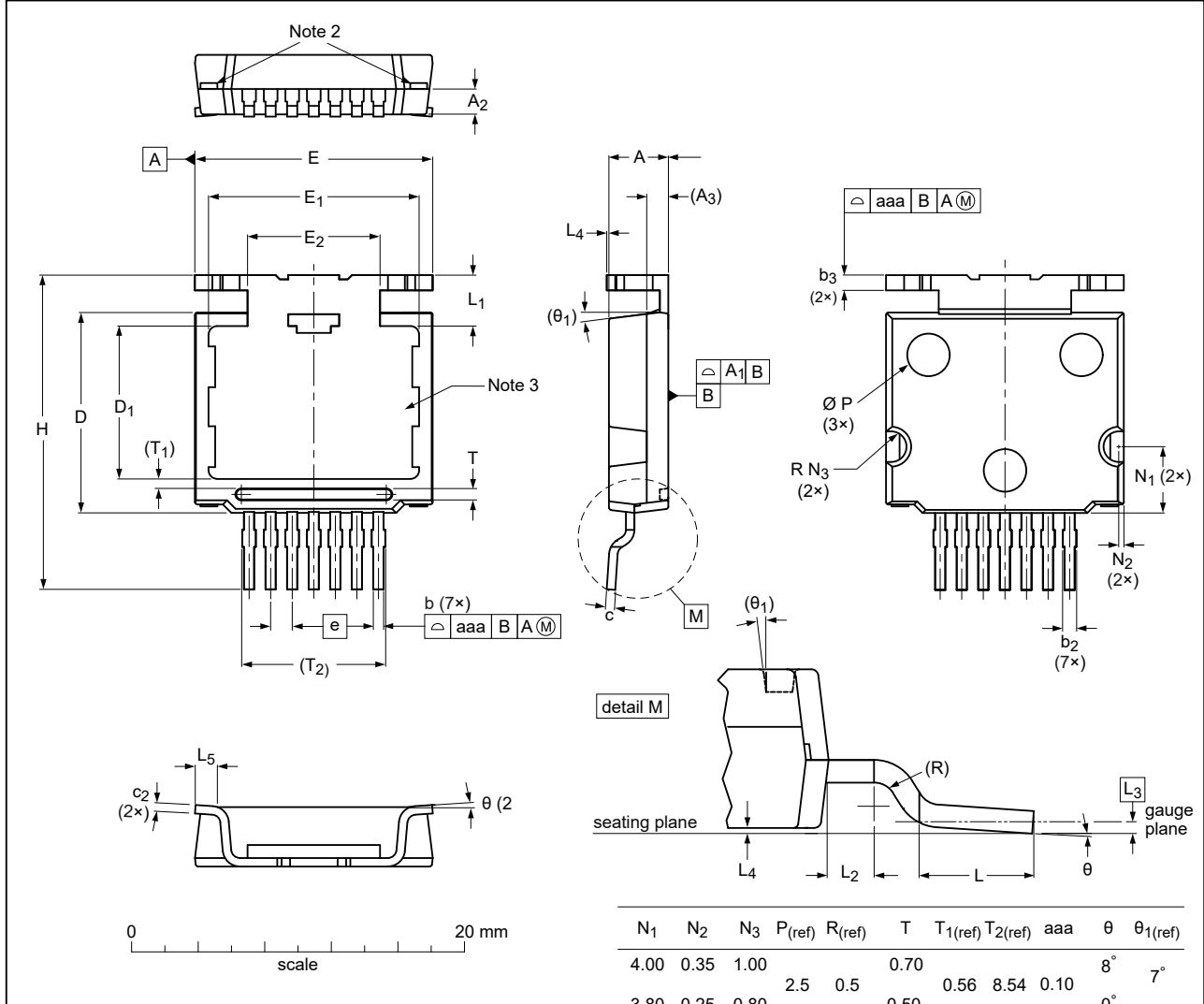
Fig. 26. Definition of gate charge characteristics



12. Package outline

X.PAK : Plastic, surface-mounted Top Side Cooling (TSC) Package;
1.27 mm pitch; 14.0 mm x 11.8 mm x 3.5 mm body

SOT8107-2



Dimensions (mm are the original dimensions)

Unit ⁽¹⁾	A	A ₁	A ₂	A _{3(ref)}	b	b ₂	b ₃	c	c ₂	D	D ₁	E	E ₁	E ₂	e	H	L	L ₁	L ₂	L ₃	L ₄	L ₅
max	3.60		1.60		0.70	1.00	1.00	0.60	0.60	11.90	9.10	14.10	12.50	7.85	1.27	19.00	2.60	3.20	1.10		0.18	2.30
nom		0.05		1.27											BSC					0.26		
min	3.40		1.40		0.50	0.50	0.80	0.40	0.40	11.70	8.90	13.90	12.30	7.75		18.00	2.40	3.00	0.90		0.07	1.42

Note

1. Max mold gate mark protrusion 0.3 mm.
2. Mold gate location shall be chosen at one of the two indicated locations.
3. Maximum allowed flash encroachment over heat sink area is 0.05 mm.

sot8107-2_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT8107-2					–24-08-07– 25-03-14

Fig. 28. Package outline X.PAK (SOT8107-2)

13. Soldering

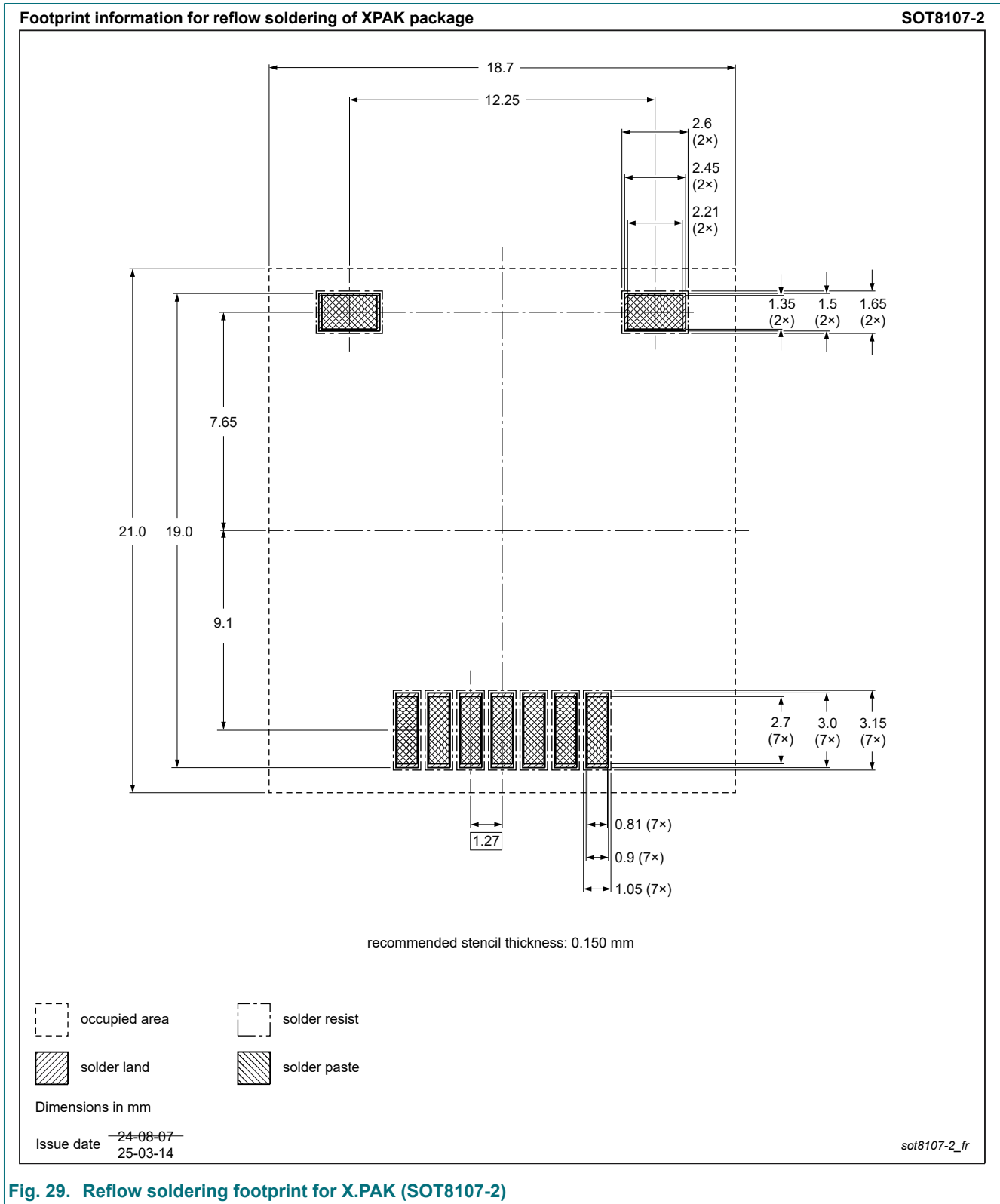


Fig. 29. Reflow soldering footprint for X.PAK (SOT8107-2)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
NSF060120T2A0 v.3	20260520	Product data sheet	-	NSF060120T2A0 v.2
Modifications:	• Characteristics: Fig. 7 and 8 labels corrected at y-axis and typo corrected in the title of Fig. 11			
NSF060120T2A0 v.2	20250324	Product data sheet	-	NSF060120T2A0 v.1
NSF060120T2A0 v.1	20250314	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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