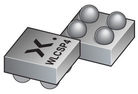


NID1101

1.5 V to 5.5 V, 1.5 A, WLCSP ideal diode with forward voltage blocking

Rev. 1 — 21 October 2025 **Product data sheet**

1. General description

The NID1101 is a compact, high-efficiency ideal diode that replaces traditional Schottky diodes in low-voltage power systems. It provides a low froward voltage drop alternative to traditional Schottky diodes while integrating both forward and true reverse current blocking.

The NID1101 operates across a 1.5 V to 5.5 V input range, and supports up to 1.5 A of continuous current. It is well suited for applications that require minimal power loss and precise current control, such as power OR-ing, redundant supply switchover, and reverse current protection. In dual-supply configurations, it enables seamless transition between sources without the need for additional control logic.

An active-high enable (EN) pin governs device operation.

- When EN is low, the NID1101 remains off, blocking current flow in both directions.
- When EN is asserted and the input voltage (IN) exceeds the output voltage (OUT), the device activates with controlled turn-on, managing inrush current during startup.

Once enabled, the device starts up in a controlled manner limiting the amount of inrush current. Once startup is completed, the device regulates the voltage between the IN and OUT pins that is approximately an order of magnitude lower than similarly rated Schottky diodes.

To ensure robust system performance, the NID1101 integrates short-circuit current limiting and thermal shutdown protection. If the output voltage rises above the input, the device automatically enters a high-impedance state with minimal reverse leakage current, effectively preventing reverse conduction.

A variety of power OR-ing configurations are supported for system flexibility:

- Two, or more, NID1101 devices
- NID1101s and conventional Schottky diodes

The NID1101 is available in a compact WLCSP4 (SOT8113) package and is characterized for operation over an ambient temperature range of –40 °C to 125 °C.

2. Features and benefits

- Input voltage range: 1.5 V to 5.5 V
- Low forward drop voltage: V_{FWD} = 29 mV (typ. at 3.6 V input and 100 mA load current)
- Reverse voltage blocking always
  - Low leakage current when $V_{OUT} > V_{IN}$
- Forward voltage blocking when disabled
- Low quiescent current
- Enhanced load transient response
- Controlled slew rate at start-up
- Over temperature protection
- Short-circuit protection
- SOT8113, 4-pin, wafer level chip scale package
- Specified over T_a= -40 °C to +125 °C

3. Applications

- Smart wearables
- OR-ing applications
- Diode replacement
- Battery backup systems
- USB powered devices

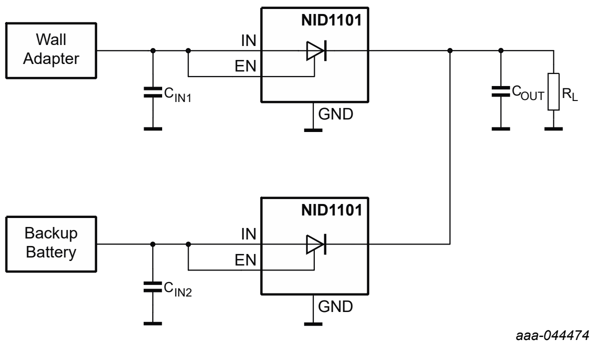


Fig. 1. Simplified application

nexperia

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NID1101UP	-40 °C to +125 °C	WLCSP4	plastic surface-mounted package; 4-pin	SOT8113

5. Marking

Table 2. Marking code

Type number	Marking code
NID1101UP	u4

6. Functional diagram

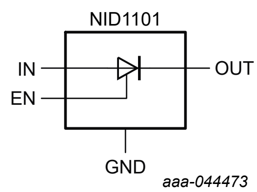


Fig. 2. Logic symbol

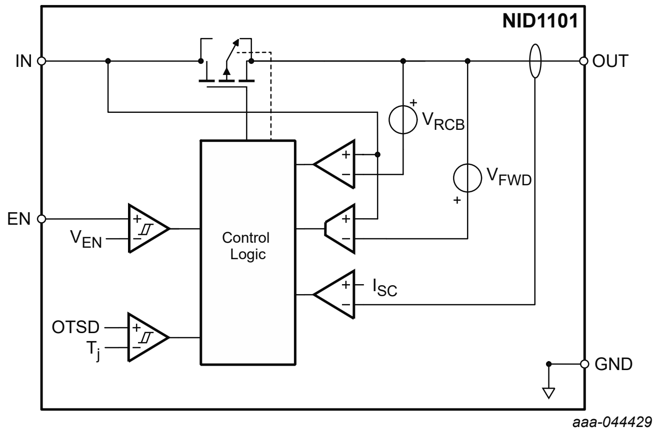


Fig. 3. Functional diagram

7. Pin configuration and description

7.1. Pin configuration

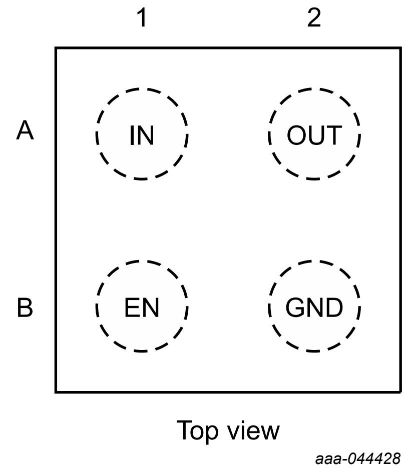


Fig. 4. Pin configuration SOT8113 (WLCSP4)

7.2. Pin description

Table 3. Pin description

Symbol	Pin	I/O	Description
IN	A1	I	“Anode” connection of the ideal diode. Connect to a power supply. Bypass with a low ESR capacitance of at least 0.1 µF.
OUT	A2	O	“Cathode” connection of the ideal diode. Connect to the load. Bypass with a low ESR capacitance of at least 0.33 µF.
EN	B1	I	Active high enable input to the IC. Connect to IN to permanently enable the device. Connect to GND to disable. Connect to an I/O to control it. Do not leave this pin floating.
GND	B2	GND	Ground (0 V)

8. Specifications

8.1. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IN}	input voltage		-0.3	6	V
V_{OUT}	output voltage		-0.3	6	V
V_{EN}	EN pin voltage		-0.3	6	V
I_{OUT}	continuous load current		internally limited		A
T_j	junction temperature		-40	150	°C
T_{stg}	storage temperature		-60	150	°C

8.2. ESD ratings

Table 5. ESD ratings

Symbol	Parameter	Conditions	Value	Unit
V_{ESD}	electrostatic discharge	HBM: ANSI/ESDA/JEDEC JS-001 class 2	±2000	V
		CDM: ANSI/ESDA/JEDEC JS-002 class C2a	±500	V

8.3. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IN}	input voltage		1.5	5.5	V
V_{OUT}	output Voltage		0	5.5	V
I_{OUT}	maximum continuous output current	> 2.0 V input	-	1.5	A
		1.6 V to 1.9 V		0.5	A
		1.5 V		50	mA
$I_{OUT,SW}$	maximum pulsed switch current	≤120 ms, 2% duty-cycle, V_{IN} = 3.3 V/5.0 V	-	2	A
V_{EN}	EN pin voltage		0	5.5	V

8.4. Recommended components

Table 7. Recommended components

Nominal component values, derating factors not included.

Symbol	Parameter	Min	Nom	Max	Unit
C_{IN}	capacitance on IN [1]	0.1	1	-	µF
C_{OUT}	capacitance on OUT [2][3]	0.33	0.47	-	µF

[1] An input capacitor is required for proper operation.
[2] An output capacitor is required for proper operation.
[3] See Section 10.4 for the detailed guidance on appropriately sizing the output capacitor.

8.5. Thermal information

Table 8. Thermal information

Thermal resistance according to JEDEC51-5 and -7

Symbol	Parameter	SOT8113	Unit
$R_{\Theta JA}$	junction-to-ambient thermal resistance	173	°C/W
Ψ_{JT}	junction-to-top characterization parameter	5	°C/W

8.6. Electrical characteristics

Table 9. Static characteristics

V_{IN} = 3.6 V, V_{EN} = 3.6 V, C_{OUT} = 0.33 µF unless otherwise specified.

Symbol	Parameter	Conditions		T_a = -40 °C to +125 °C		Unit
			Min	Typ[1]	Max	
Input						
$I_{IN,Q}$	input quiescent current	V_{EN} = V_{IN}	-	600	1100	nA
$I_{IN,SD}$	input shutdown current	EN = LO	-	120	430	nA
Pass FET						
V_{FWD}	forward voltage drop	V_{IN} = 1.5 V; I_O= 50 mA	-	21	50	mV
		V_{IN} = 3.6 V; I_O= 100 mA	-	29	52	mV
		V_{IN} = 3.6 V; I_O= 500 mA [2]	-	55	72	mV
		V_{IN} = 3.6 V; I_O= 1000 mA [2]	-	110	155	mV
		V_{IN} = 5.5 V; I_O= 100 mA	-	31	50	mV
Reverse current blocking						
V_{RCBA}	RCB activation voltage	V_{OUT} - V_{IN}	-	31	-	mV
V_{RCBD}	RCB deactivation voltage	V_{IN} - V_{OUT}	-	41	-	mV
$I_{IN,LKGE}$	leakage current into IN, enabled	V_{OUT} = 4 V [2]	-220	331	615	nA
		V_{OUT} = 5 V	-220	332	615	nA
$I_{OUT,LKGE}$	leakage current into OUT, enabled	V_{OUT} = 4 V [2]	-200	372	1200	nA
		V_{OUT} = 5 V	-200	449	1200	nA
$I_{IN,LKGD}$	leakage current into IN, disabled	V_{OUT} = 4 V; EN = LO [2]	-500	-	500	nA
		V_{OUT} = 5 V; EN = LO	-500	-	500	nA
Enable input						
$V_{EN,HI}$	enable high threshold		1.2	-	-	V
$V_{EN,LO}$	enable low threshold		-	-	0.4	V
$V_{EN,HYS}$	enable hysteresis		-	45	-	mV
$I_{EN,HI}$	enable input current	V_{EN} = 3.6 V	-	-	50	nA
Short Circuit Protection						
I_{LIM}	over current limit	R_L = 100 mΩ	-	2.2	-	A
Over temperature shutdown						
T_{OTSD}	overtemperature shut down	T_j rising [2]	170	175	-	°C
T_{OTHYS}	over temperature hysteresis	T_j falling [2]	-	35	-	°C

[1] All typical values are measured at T_{amb} = 25 °C.
[2] *Not tested in production. Obtained by characterization.*

8.7. Dynamic characteristics

Table 10. Dynamic characteristics

V_{IN} = 3.6 V, C_{OUT}= 1 µF, R_L = open unless otherwise specified.

Symbol	Parameter	Conditions		T_a = 25 °C			Unit
				Min	Typ	Max	
$t_{ON,DLY}$	turn-On delay time	V_{EN} = LO to HI step to V_{OUT} = 10 %		-	660	-	µs
t_{RISE}	rise time	V_{OUT} = 10 % to V_{OUT} = 90%		-	100	-	µs
t_{RCB}	reverse current blocking time	V_{OUT} = V_{IN}-100 mV to V_{IN} +100mV step to I_{IN} < 1 mA	[1]	-	20	-	µs
t_{LIM}	current limit response time	OUT shorted with 100 mΩ to I_{OUT} within 10% of I_{LIM}	[1]	-	35	-	µs

[1] *Not tested in production. Obtained by characterization.*

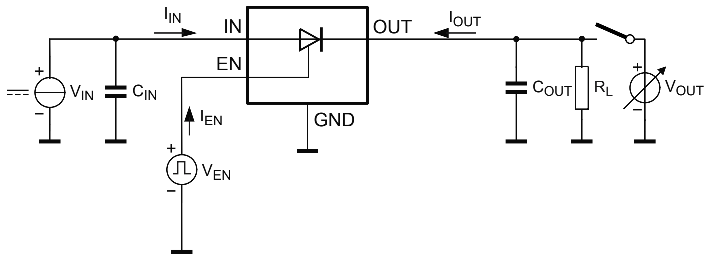


Fig. 5. Test circuit

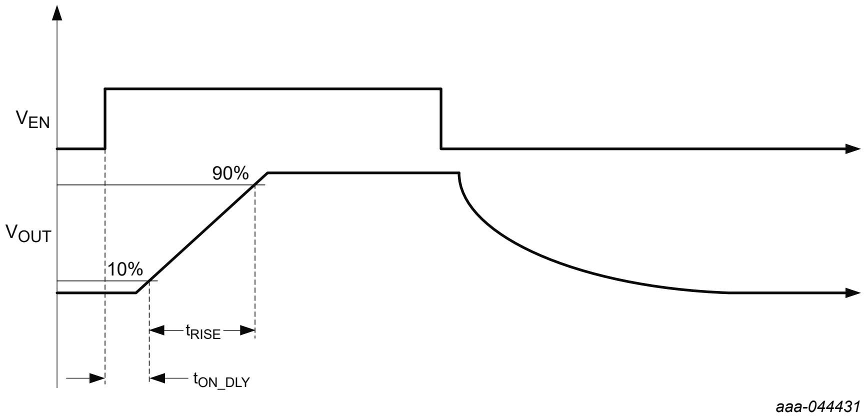
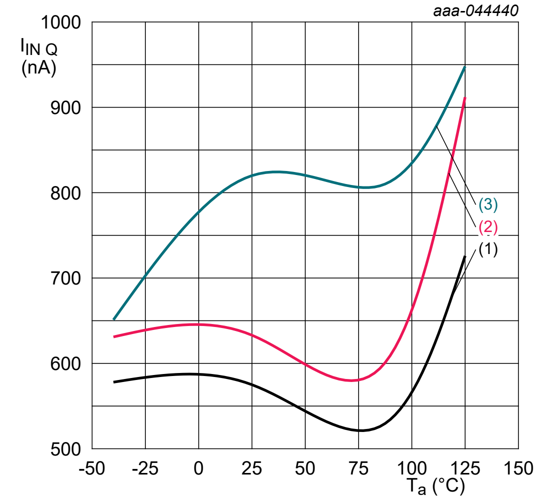


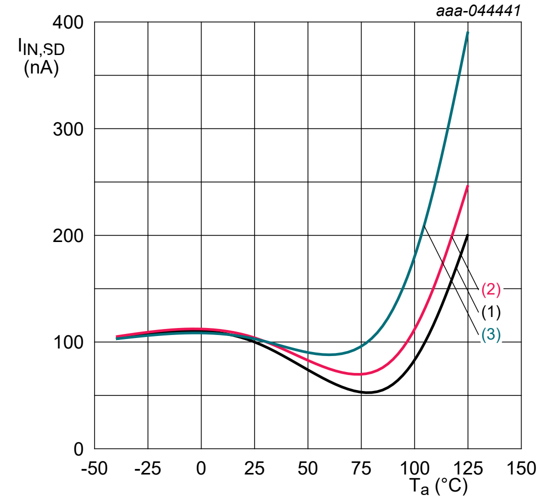
Fig. 6. Timing diagrams

8.8. Typical characteristics graphs



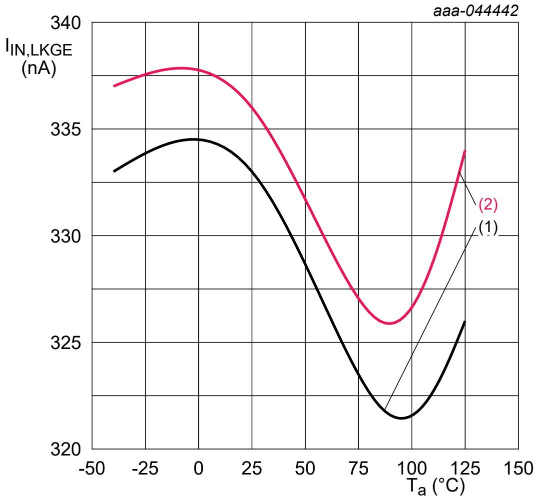
1) V_{IN} = 1.5 V
2) V_{IN} = 3.6 V
3) V_{IN} = 5.5 V

Fig. 7. Input quiescent current ($I_{IN,Q}$) versus ambient temperature



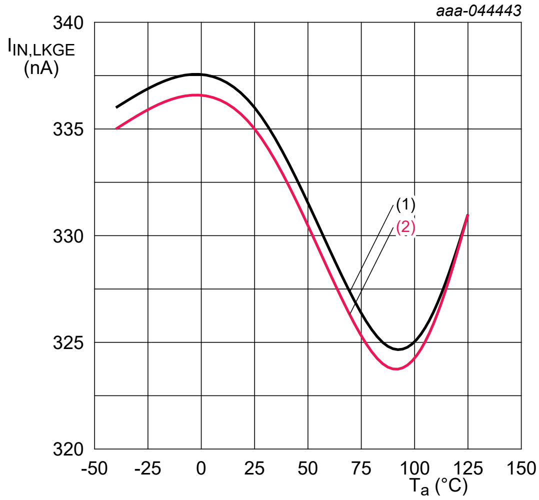
1) V_{IN} = 1.5 V
2) V_{IN} = 3.6 V
3) V_{IN} = 5.5 V

Fig. 8. Input shutdown current ($I_{IN,SD}$) versus ambient temperature



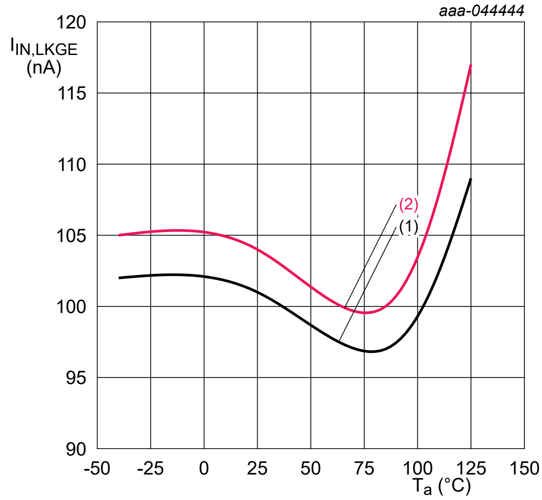
1) V_{IN} = 1.5 V
2) V_{IN} = 3.6 V

Fig. 9. Input leakage current, enabled, ($I_{IN,LKGE}$) ambient temperature at V_{OUT} = 4 V



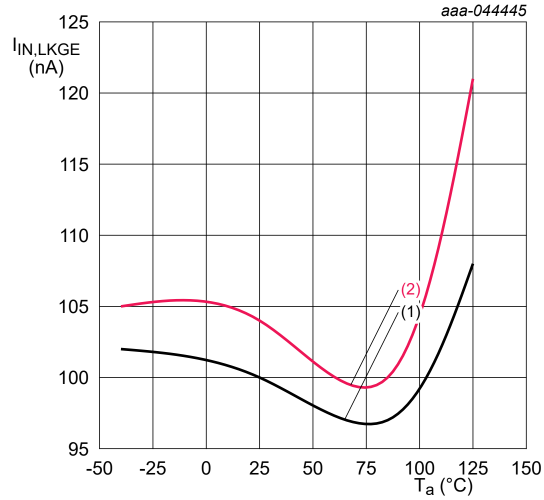
1) V_{IN} = 1.5 V
2) V_{IN} = 3.6 V

Fig. 10. Input leakage current, enabled, ($I_{IN,LKGE}$) versus ambient temperature at V_{OUT} = 5 V



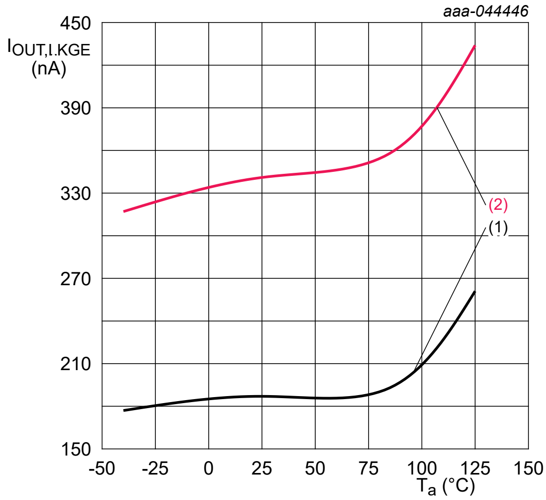
1) V_{IN} = 1.5 V
2) V_{IN} = 3.6 V

Fig. 11. Input leakage current, disabled, ($I_{IN,LKGD}$) versus ambient temperature at V_{OUT} = 4 V



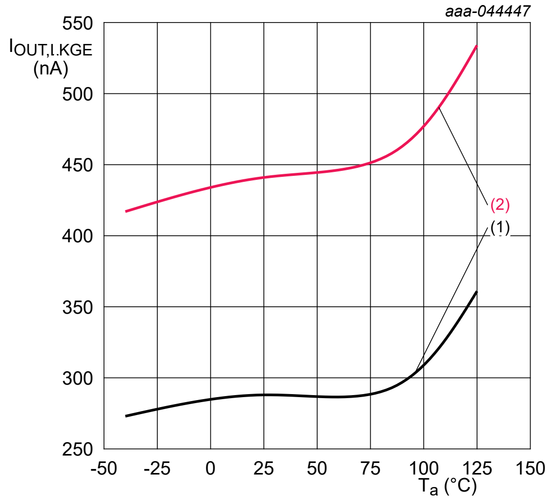
1) V_{IN} = 1.5 V
2) V_{IN} = 3.6 V

Fig. 12. Input leakage current, disabled, ($I_{IN,LKGD}$) versus ambient temperature at V_{OUT} = 5 V



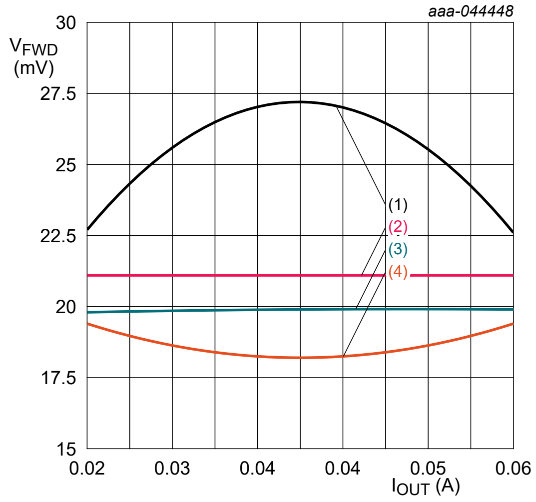
1) V_{IN} = 1.5 V
2) V_{IN} = 3.6 V

Fig. 13. Output leakage current, enabled, ($I_{OUT,LKGE}$) versus ambient temperature at V_{OUT} = 4 V



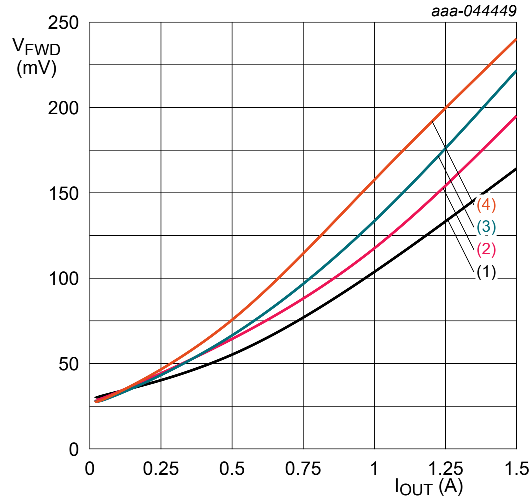
1) V_{IN} = 1.5 V
2) V_{IN} = 3.6 V

Fig. 14. Output leakage current, enabled, ($I_{OUT,LKGE}$) versus ambient temperature at V_{OUT} = 5 V



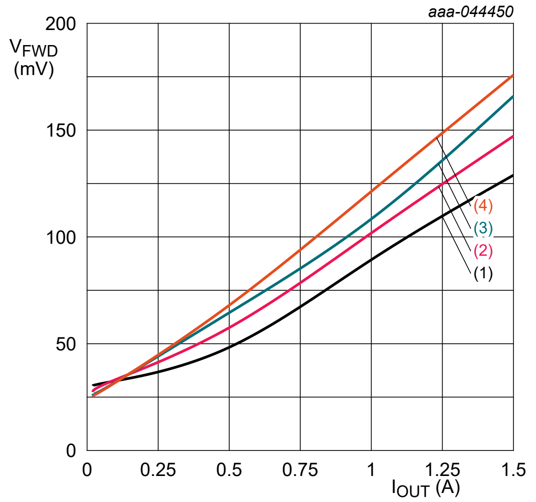
1) T_a = -40 °C
2) T_a = 25 °C
3) T_a = 85 °C
4) T_a = 125 °C

Fig. 15. Forward voltage drop versus load current at V_{IN} = 1.5 V



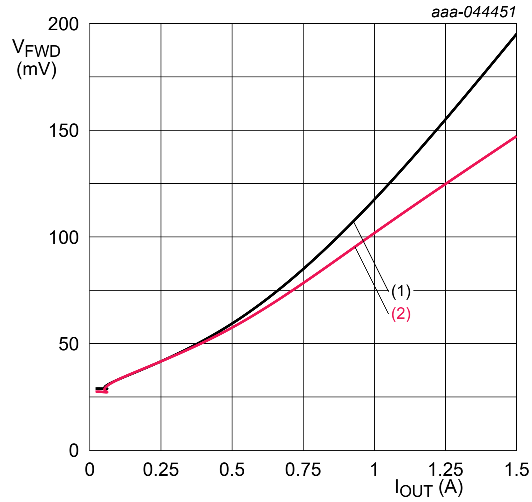
1) T_a = -40 °C
2) T_a = 25 °C
3) T_a = 85 °C
4) T_a = 125 °C

Fig. 16. Forward voltage drop versus load current at V_{IN} = 3.6 V



1) T_a = -40 °C
2) T_a = 25 °C
3) T_a = 85 °C
4) T_a = 125 °C

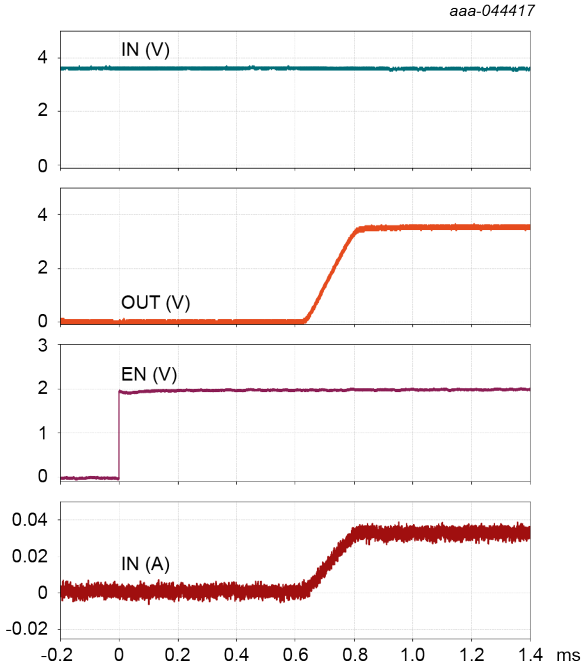
Fig. 17. Forward voltage drop versus load current at V_{IN} = 5 V



1) V_{IN} = 3.6 V
2) V_{IN} = 5.5 V

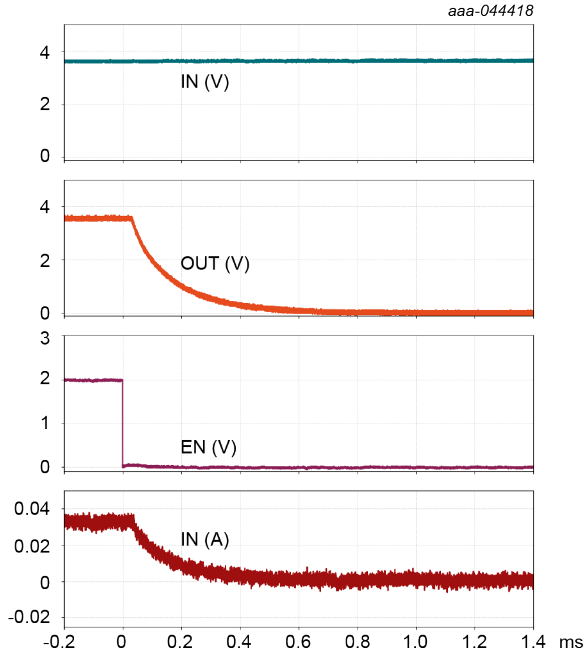
Fig. 18. Forward voltage drop versus load current at T_a = 25 °C

8.9. Typical characteristics graphs



- R_L = 120 Ω
- V_{IN} = 3.6 V

Fig. 19. Start-up with enable



- R_L = 120 Ω
- V_{IN} = 3.6 V

Fig. 20. Shutdown with enable

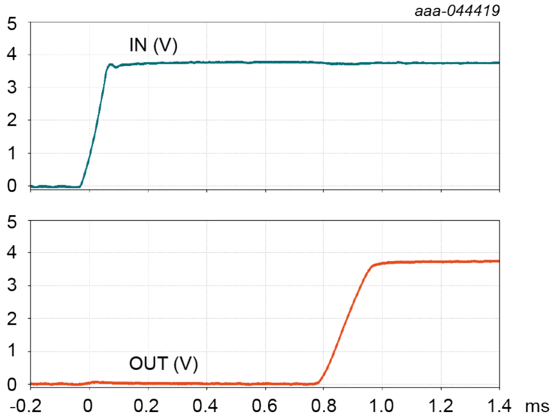


Fig. 21. Start-up with V_{IN} (V_{IN} ramp from 0 V to 3.6 V in 100 µs, EN tied to V_{IN}, R_L = 120 Ω)

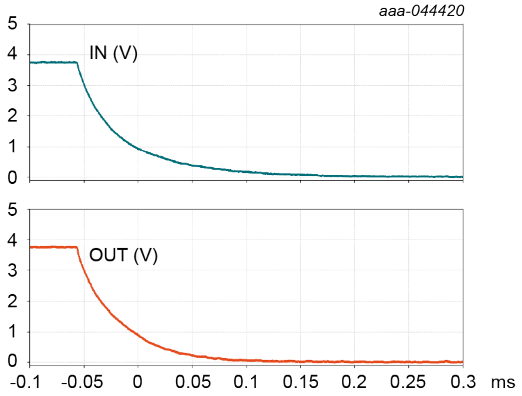
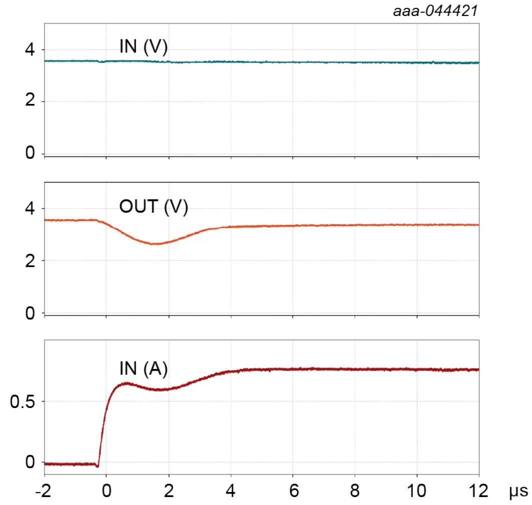
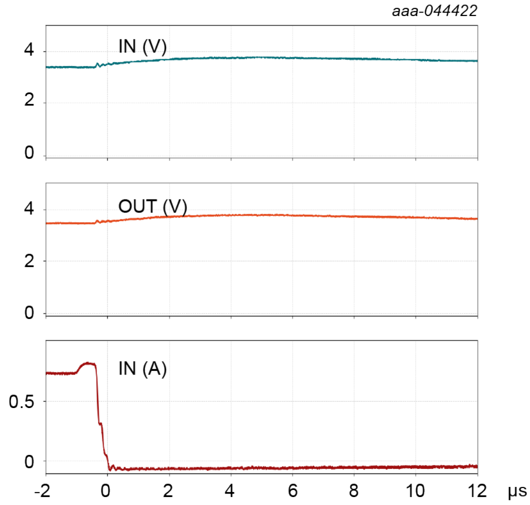


Fig. 22. Shutdown with V_{IN} (V_{IN} ramp from 3.6 V to 0 V in 100 µs, EN tied to V_{IN}, R_L = 120 Ω)



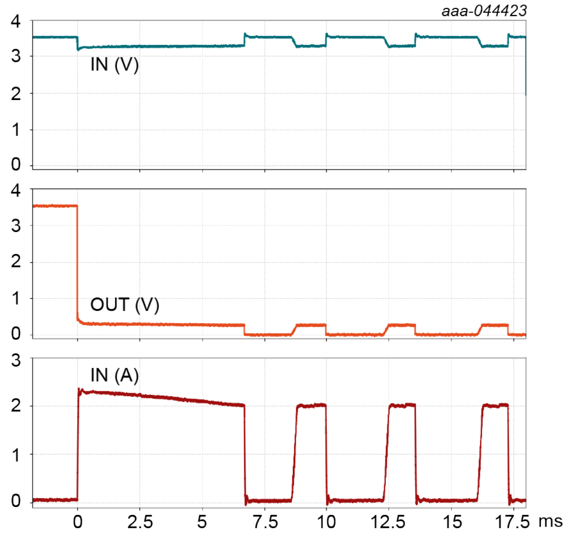
- V_{IN} = 3.6 V

Fig. 23. Load step response (I_{OUT} step from 0 A to 0.75 A)



- V_{IN} = 3.6 V

Fig. 24. Load step response (I_{OUT} step from 0.75 A to 0 A)



- V_{IN} = 3.6 V
- C_{IN} = 100 µF
- Output shorted with 0.1 Ω resistor

Fig. 25. Short circuit response

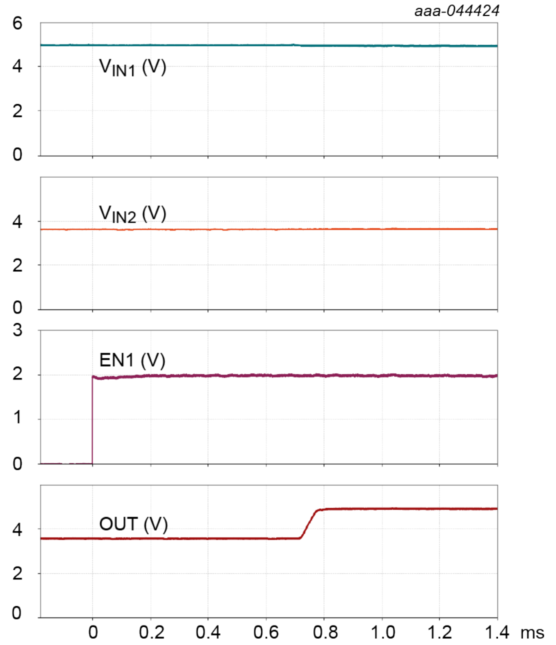


Fig. 26. OR-ing with enable (V_{IN1} = 5 V, V_{IN2} = 3.6 V; EN1 Low to High transition, EN2 tied to V_{IN2})

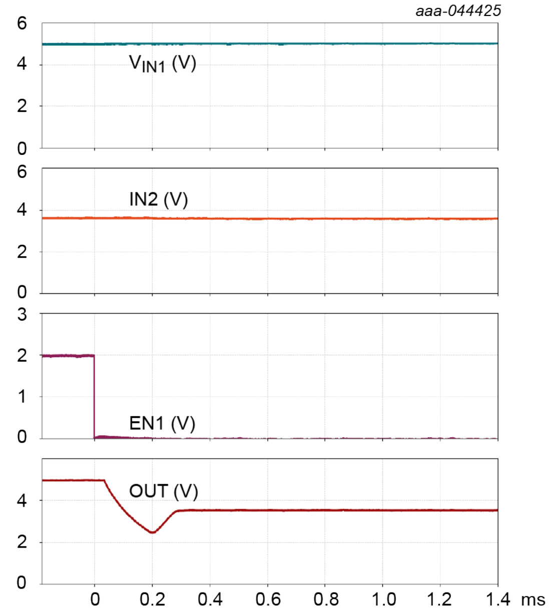


Fig. 27. OR-ing with enable (V_{IN1} = 5 V, V_{IN2} = 3.6 V; EN1 High to Low transition, EN2 tied to V_{IN2})

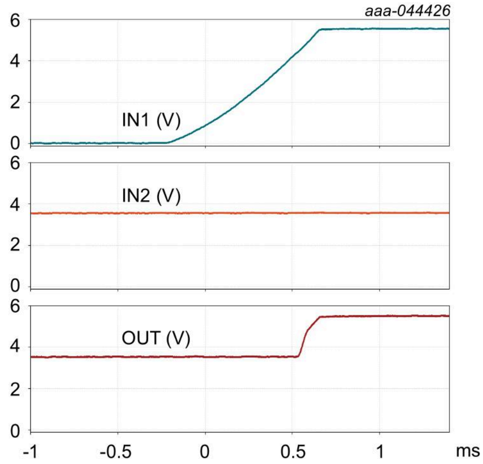


Fig. 28. OR-ing with V_{IN} (V_{IN1} = 0 V to 5 V in 1 ms, V_{IN2} = 3.6 V; EN1 tied to V_{IN1}, EN2 tied to V_{IN2})

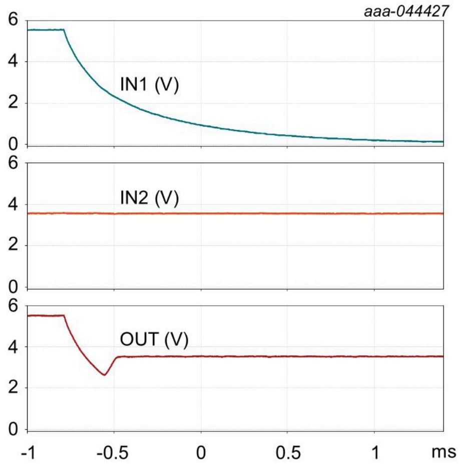


Fig. 29. OR-ing with V_{IN} (V_{IN1} = 5 V to 0 V in 1 ms, V_{IN2} = 3.6 V; EN1 tied to V_{IN1}, EN2 tied to V_{IN2})

9. Functional description

9.1. Overview

The NID1101 is a single-channel ideal diode capable of handling a 1.5 A continuous current. It is offered in a small, space-saving SOT8113 (WLCSP4) package.

This device uses a regulated P-channel MOSFET to achieve a very low forward voltage drop from its input to its output. It integrates several key protection features, including inrush current limiting, reverse voltage blocking, and over-temperature protection.

During shutdown, the NID1101 has a very low leakage current, which minimizes power consumption and prevents unnecessary leakage to downstream modules during standby.

9.2. Startup

The device starts when the voltage at either IN or OUT pins reach 1.5 V. Until then, there is insufficient voltage to power up the internal circuitry.

When V_{IN} exceeds 1.5 V, $V_{OUT} < V_{IN}$, and EN is low, the device enters Power-On-Reset (POR). In this situation, the switch is held OFF and the body diode is oriented such that the anode is at OUT and cathode is at IN. If EN pin goes high, the IC starts charging the output capacitor with an internally controlled slew rate. Once the capacitor is fully charged, the internal FET's gate is controlled by a transconductance amplifier to maintain a constant difference between V_{IN} and V_{OUT} to emulate a diode. If EN is pulled low at any time, the FET is turned OFF.

9.3. Functional modes

Table 11 summaries the various functional modes of the NID1101 and the status of the diode in each mode.

Table 11. Device functional modes ($V_{IN} \geq 1.5$ V)

V_{IN}	Functional mode	EN pin	Power device state
$V_{IN} \geq 1.5$ V	OFF	LOW	OFF: forward blocking
	ON	HIGH	ON: forward conduction regulated V_{FWD}
	Reverse current blocking $V_{OUT} > V_{IN}$	X	OFF: reverse blocking
	Output short	HIGH	ON: forward conduction regulated I_{OUT}
	Thermal fault	HIGH	OFF: reverse blocking
$V_{IN} = 0$ V	OFF	X	OFF: forward voltage blocking

The forward drop of the NID1101 depends on the input voltage and load current. Fig. 30 shows the internal block diagram of the NID1101 in forward regulation mode. Based on this figure, the drop seen between the IN and OUT pins (V_{FWD}) is given by the equation

$$V_{FWD} = I_{OUT} \times \left(R_{BP1} + R_{BP2}\right) + V_{FET}$$

where I_{OUT} is the load current, R_{BP1} and R_{BP2} are the bond pad impedances and V_{FET} is the voltage drop across the FET.

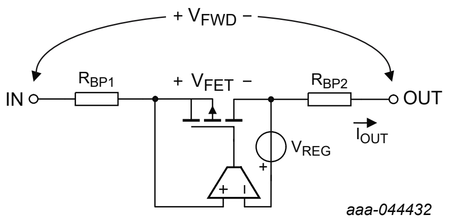


Fig. 30. NID1101 regulation scheme

The voltage drop across the FET is regulated to V_{REG} until the load current increases to a point where

$$I_{OUT} = \frac{V_{REG}}{R_{ON}}$$

where R_{ON} is the resistance of the FET.

The overall variation of the forward voltage incorporating all these effects is shown in Fig. 31.

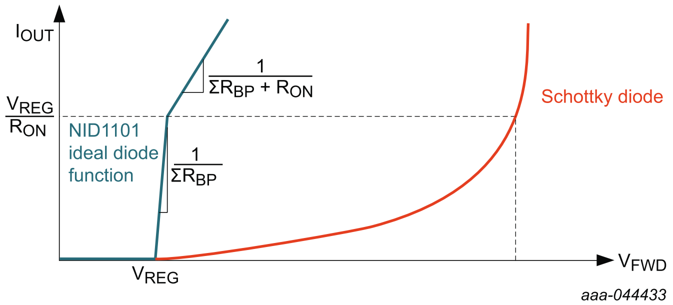


Fig. 31. NID1101 I-V curve

9.4. Reverse current blocking

Reverse Current Blocking (RCB) protection is always active, regardless of the state of EN. This protects the power supply from having to sink currents.

Two scenarios can activate the reverse current blocking functional mode.

- Output voltage starts rising and exceeds the input voltage (eg: OR-ing with two different voltage levels)
- Input voltage starts falling and goes below the output voltage (eg: loss of input power)

In either case, the NID1101 tries to maintain the forward drop between V_{IN} and V_{OUT}. As the V_{IN}-V_{OUT} differential starts reducing, the transconductance amplifier modulates the gate of the FET to increase its resistance to maintain the $V_{IN} – V_{OUT}$ differential. Once $V_{IN} \leq V_{OUT}$, the transconductance amplifier turns off the pass transistor and prevents reverse currents. An internal comparator detects when $V_{IN} \leq V_{OUT} - V_{RCBA}$ and flips the body diode polarity to ensure that the diode remains reverse biased.

When V_{IN} starts rising (or V_{OUT} starts falling) and V_{IN} exceeds $V_{OUT} + V_{RCBD}$, the body diode polarity is flipped such that the anode is at IN and the pass FET starts conducting.

In case of an extremely fast transition from forward conduction to reverse bias, the comparator also acts to turn off the pass transistor before the transconductance amplifier has a chance to react.

9.5. Output overload and temperature protection

Unlike conventional diodes and other ideal diodes, the NID1101 is also protected from output short circuit and over temperature conditions. This is due to its unique feature of being able to block voltages in either direction.

When the output current exceeds I_{LIM}, the NID1101 limits the current through the device to I_{LIM}. It will stay in this current regulation mode until the output overload condition disappears or the junction temperature of the part exceeds T_{OTSD}.

Once an over temperature condition is detected, the NID1101 turns off the pass transistor. Once the NID1101 cools down such that $T_j < T_{OTSD} – T_{HYS}$, the part attempts restart in an inrush controlled manner.

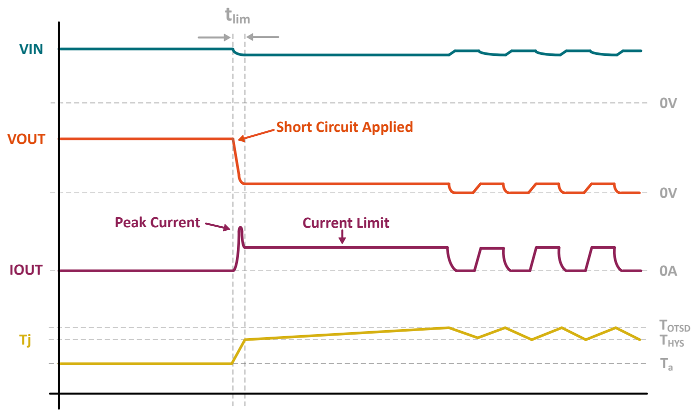


Fig. 32. NID1101 Current limiting and over temperature shut down

10. Application information

The NID1101 ideal diode is a versatile device suitable for high side power switching, protecting against reverse current conditions, OR-ing and simple power multiplexing. The following sections provide application examples to aid the design of products using NID1101.

Note:

Application implementation information in the following sections is not part of the Nexperia component specification. Nexperia's device users are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1. Startup

10.1.1. n+1 OR-ing using ideal diodes

There is no specific limitation to the number of NID1101 ideal diodes used for power OR-ing. The example below illustrates a common two power supply scenario with smooth transitions between supplies.

Some devices operate from a fixed power supply such as a standard 5 V USB port output in normal conditions but must quickly transition to a 1.5 V battery backup when the power supply is disabled or unplugged. Using two NID1101 devices in a power OR-ing configuration, the downstream load remains uninterrupted when either the DC supply or the backup battery is disconnected.

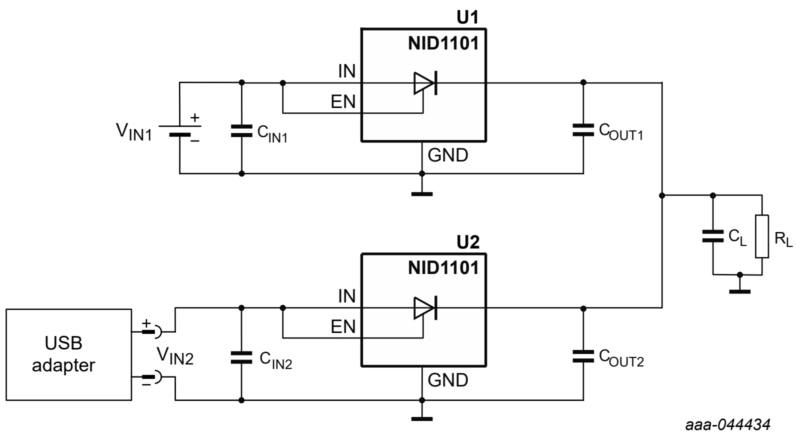


Fig. 33. OR-ing power supply and battery

The scope capture shows the output voltage (V_{OUT}) being initially powered by V_{IN2} at 5 V. When V_{IN2} is removed, V_{IN1} at 1.5 V powers V_{OUT}. When V_{IN1} is reconnected, V_{OUT} is once again powered by V_{IN2}.

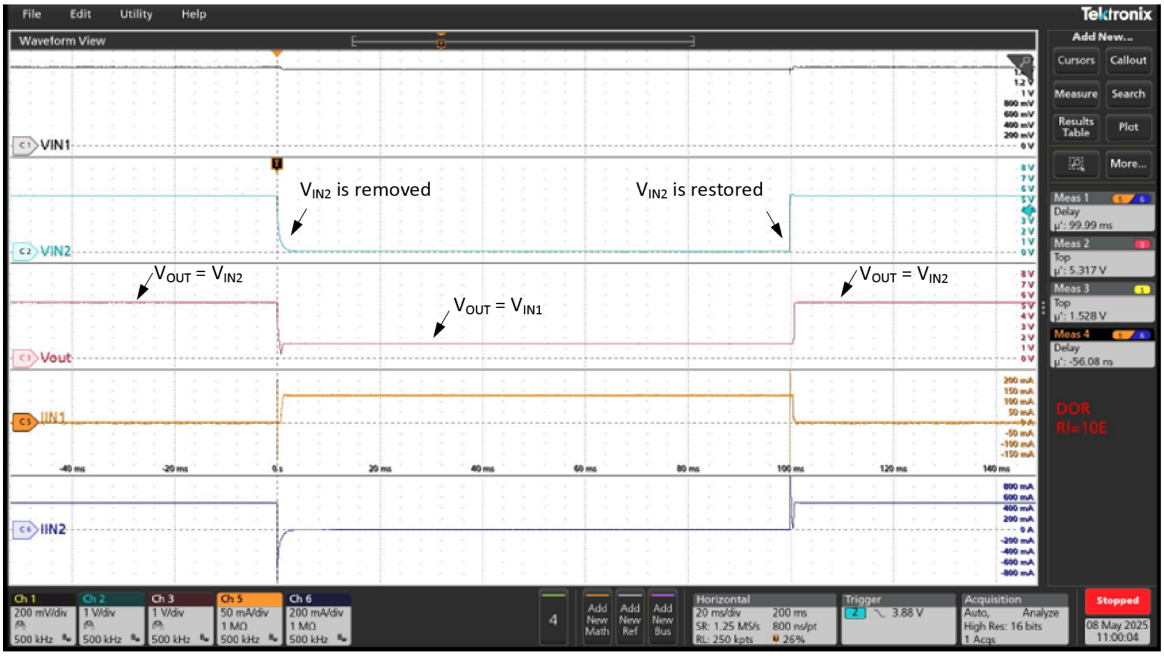


Fig. 34. Waveforms showing OR-ing behavior

10.1.2. OR-ing similar supply voltages

Some applications may require the OR-ing of supplies with similar voltages (for example, Fig. 35 and Fig. 36). In these examples, the primary DC supply is 3.3 V with a 3 V battery backup. Consider the scenario where V_{IN1}, which is initially supplying the load, is removed and subsequently restored.

In case of the OR-ing scenario with Schottky diodes, as the two supplies differ by only 300 mV, when V_{IN1} is restored, there may not be enough forward voltage, V_F, across the diode in the V_{IN1} path to forward bias it. Thus, V_{IN2} will continue to deliver power to the load until the battery voltage depletes sufficiently wasting energy in the backup source.

In case of the OR-ing scenario with NID1101s, when V_{IN1} is restored, the reverse current blocking deactivation threshold, V_{RCBD}, is easily exceeded allowing the 3.3 V supply to carry the full load. As the OUT is approximately 300 mV above V_{IN2}, the 3 V supplied NID1101 becomes reverse biased and the battery drain is minimized.

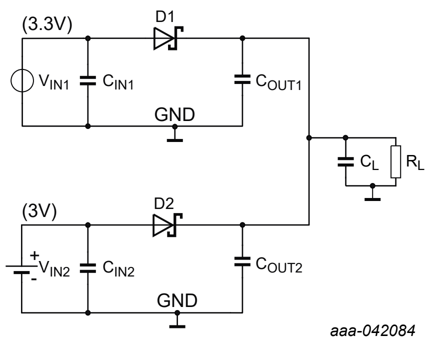


Fig. 35. OR-ing with Schottky diodes

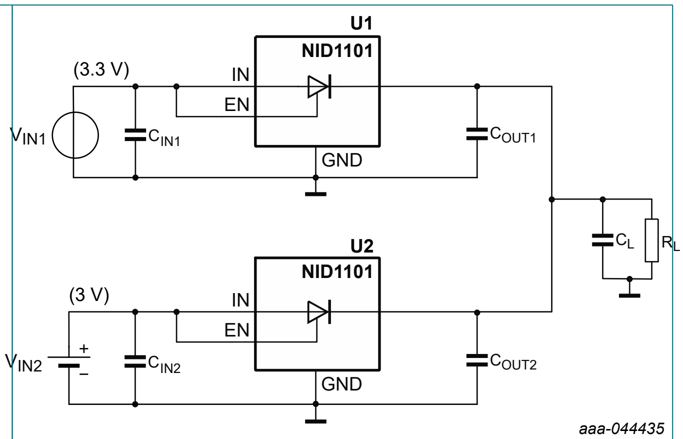


Fig. 36. OR-ing with NID1101

10.1.3. n+1 OR-ing using ideal and conventional diodes

When voltage drops and electrical losses of one of two power sources is not of concern, a combination of ideal diodes and conventional diodes can be implemented as shown in Fig. 37. In this example the AC-DC adapter is the primary power source supplying 5 V to the system with three alkaline cells providing a 4.5 V backup. As stated in Section 8.6, consideration

should be given to the V_F rating of the Schottky diode as well as worst case tolerances of the supply voltages to ensure seamless transitions.

A resistor, R_{PD}, connected to ground in the Schottky diode path is recommended to prevent diode reverse leakage during blocking conditions from charging C_{IN1} and raising V_{IN1}.

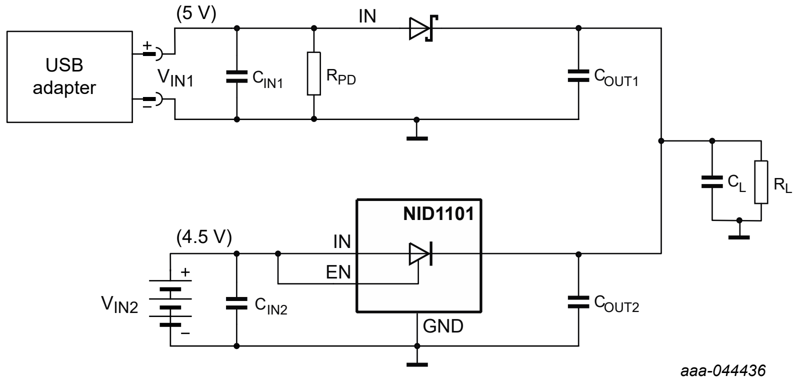


Fig. 37. OR-ing behavior with a combination of ideal and Schottky diodes

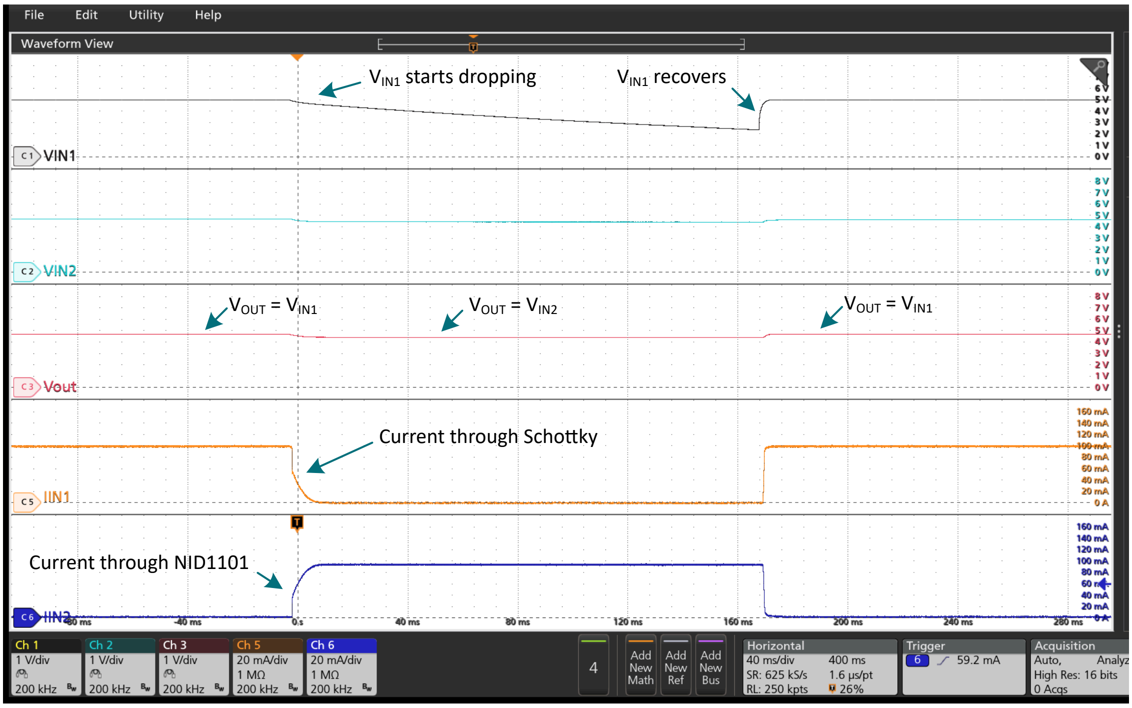


Fig. 38. Waveforms showing OR-ing behavior with a combination of ideal and Schottky diode (PMEG4010)

10.1.4. Paralleling NID1101 for thermal and sustained high current considerations

As with using any power semiconductor component, thermal ratings must be observed to maintain device reliability. Refer to the Section 8.5 table. System thermal analysis should be performed to ensure the device junction temperature, T_J, remains below 125 °C under all operating conditions. If analysis shows that using a single NID1101 would cause a thermal violation, two NID1101s can be paralleled to share the load current and lower internal power dissipation as shown in Fig. 39. Fig. 40 shows two NID1101's supporting a combined 3 A load current with 1.5 A current flowing in each NID1101.

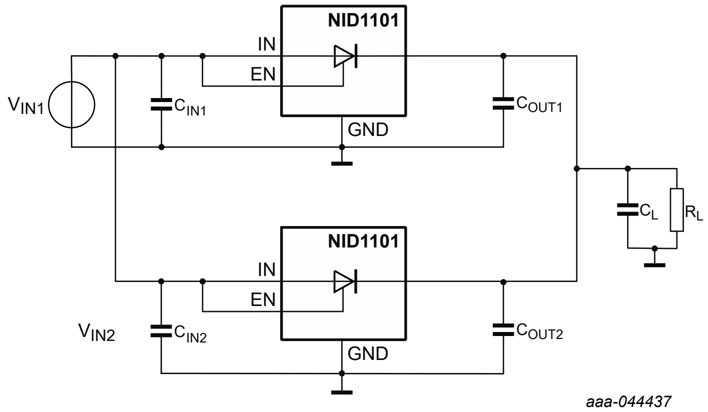


Fig. 39. Paralleling two NID1101 ideal diodes for high current

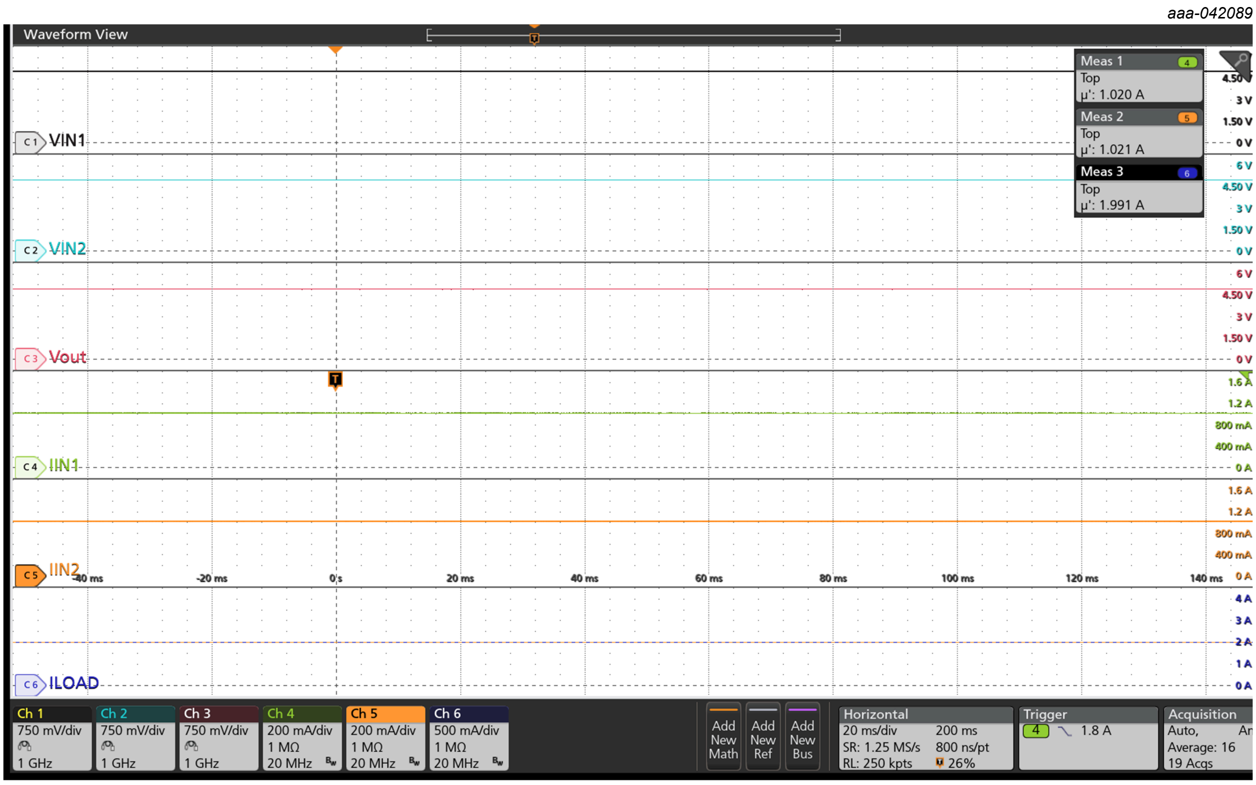


Fig. 40. Waveforms showing paralleling of two NID1101s

10.1.5. Power multiplexing and load switching

Because the NID1101 has forward voltage blocking, it is possible to use a single device as a high side load switch with short circuit protection or multiple devices for power multiplexing. Fig. 41 depicts an application example that can be used to switch between a USB-PD source, a wall wart and a Li-ion battery.

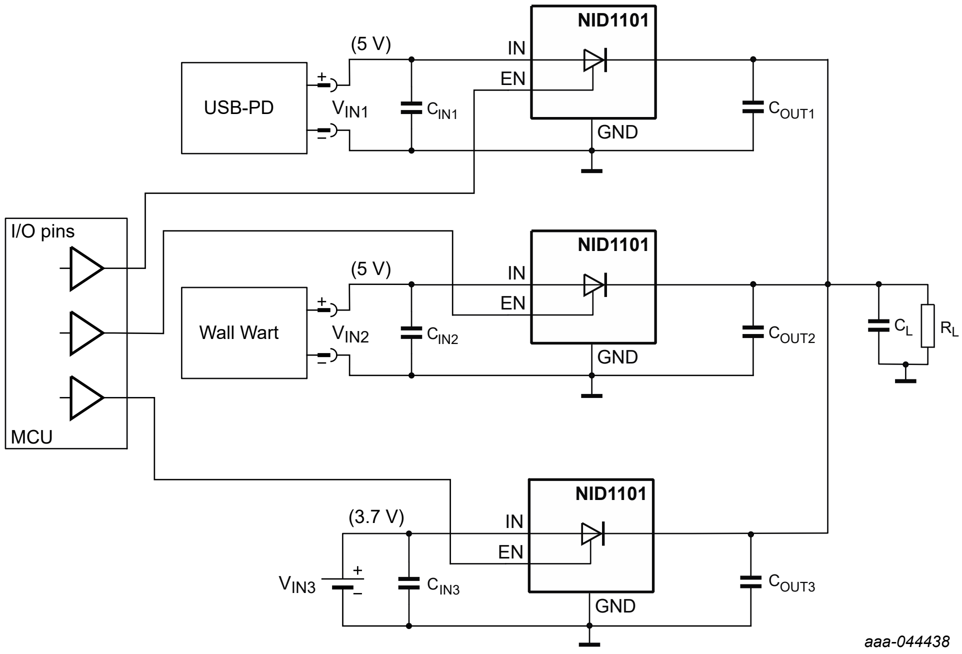


Fig. 41. Power multiplexing with NID1101

10.2. Thermal characteristics and power dissipation

The junction temperature of a semiconductor device is determined by the internal power dissipation and its capacity to dissipate heat to the surrounding environment. The electronic equivalent is shown in Fig. 42.

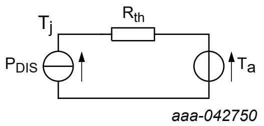


Fig. 42. Thermal diagram

From the diagram, the formula for calculating the junction temperature can be derived as follows:

$$T_j = P_{DIS} \times R_{th} + T_{amb}$$

Where T_j is the junction temperature, P_{DIS} is the power dissipation, R_{th} is the thermal resistance, and T_{amb} is the ambient temperature.

The internal power dissipation is given by:

$$P_{DIS} = I_{OUT} \times (V_{IN} - V_{OUT})$$

where I_{OUT} is the output current, V_{IN} is the input voltage, and V_{OUT} is the output voltage.

It is a characteristic of semiconductor devices that power losses increase with rising temperatures. Operating the device above the specified maximum junction temperature of 125°C can lead to thermal runaway due to these increased losses, thereby reducing the device's lifespan or triggering thermal protection.

The aforementioned equations can be used to estimate the junction temperature for a given application. To verify the actual junction temperature, the specified Ψ_{JT} value can be used in conjunction with the measured top package temperature:

$$T_j = \Psi_{JT} \times P_{DIS} + T_{TOP}$$

where T_{TOP} is the top surface temperature of the package.

10.3. Power supply recommendations

NID1101 is designed to operate with a V_{IN} range of 1.5 V to 5.5 V.

The V_{IN} power supply must be well regulated and placed as close to the device terminal as possible. The power supply must be able to withstand all transient load current steps.

In most cases, using an input capacitance (C_{IN}) of 0.1 + 1 μF is sufficient to prevent the supply voltage from drooping. In other cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance is required on the input.

An effective capacitance of no less than 0.3 μF, after applying voltage and temperature derating factors, is required on the OUT pin to ensure the stability of the control loop Gm amplifier.

10.4. Output capacitance considerations

When selecting the output capacitor (C_{OUT}) for the NID1101, consider inrush current, thermal performance, startup behavior, and system stability. Internal validation showed stable operation with output capacitance up to 1000 μF (1 mF).

Testing used hot-plug conditions at V_{IN} = 5.5 V, load current = 1.5 A, and C_{OUT} = 1 mF at an ambient temperature of 85 °C. The device completed over 1 million cycles with no degradation or abnormal behavior. This result confirms the robustness of the NID1101 under high output capacitance.

The NID1101 can support output capacitance above 1 mF. This allows flexibility for designs that require large bulk capacitance or load stabilization. However, the correct value of C_{OUT} depends on the system design and operating conditions. The designer must check inrush current, thermal limits, startup behavior, and stability before selecting a capacitor. While 1 mF is a validated safe value, higher values are acceptable at the designer's discretion.

10.5. PCB layout

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for V_{IN}, V_{OUT} and GND helps minimize the parasitic electrical events.

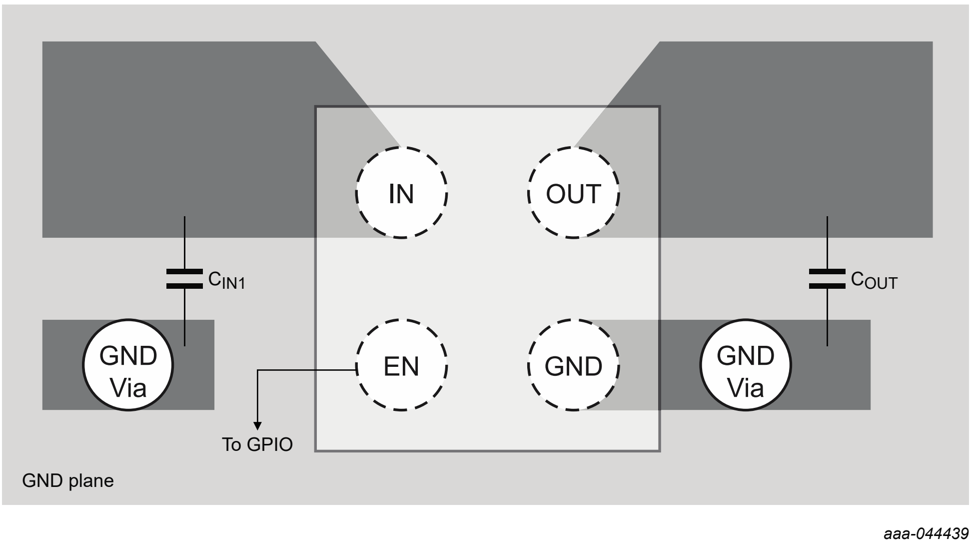
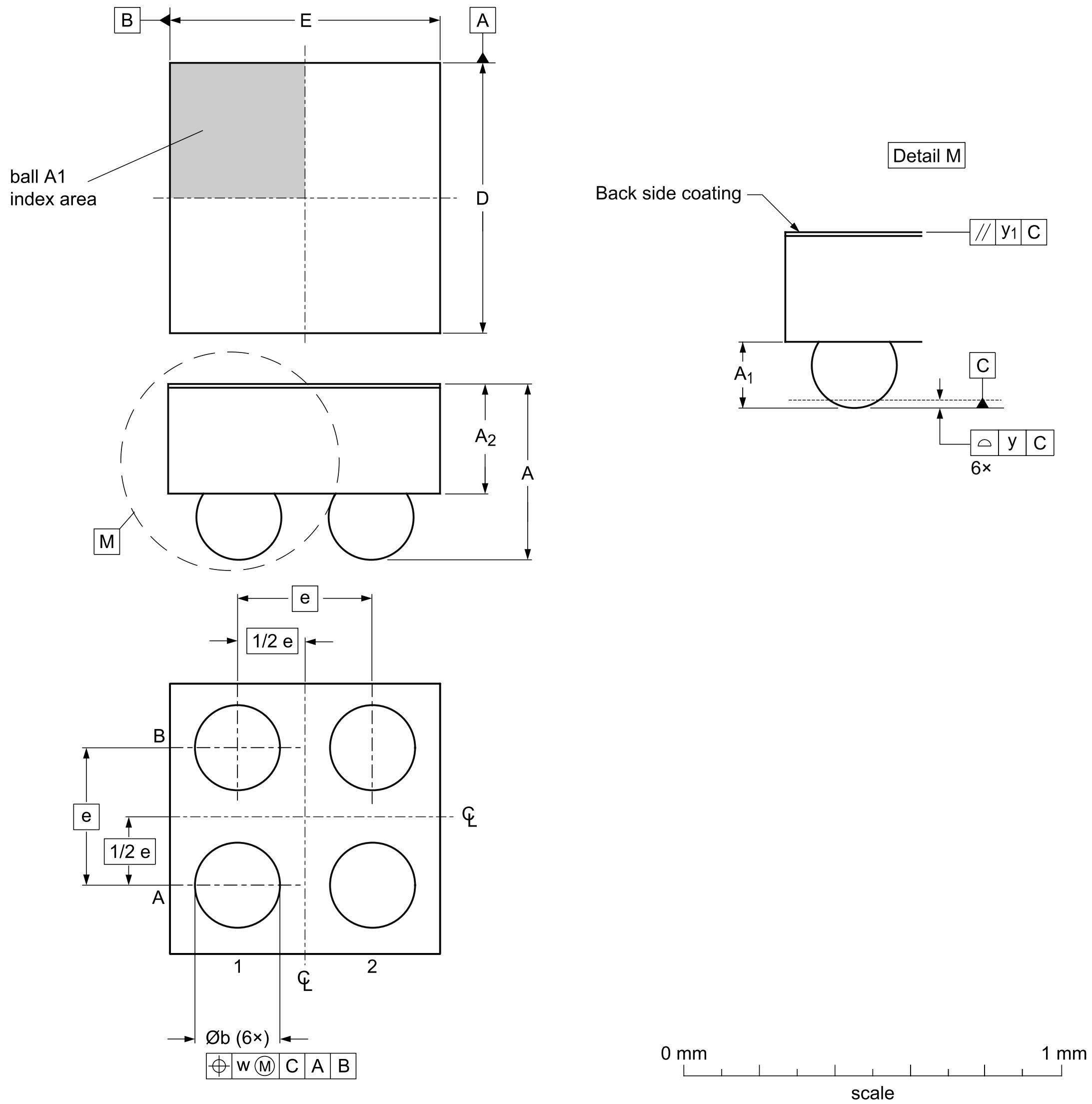


Fig. 43. PCB layout

11. Package outline

WLCSP4: wafer level chip-size package; 4 bumps **SOT8113**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	w	y	y_1
mm	max	0.465		0.290	0.245	0.745	0.745				
	nom			0.265	0.225	0.715	0.715	0.35 BSC	0.015	0.05	0.06
	min		0.145	0.240	0.205	0.685	0.685				

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8113						25-09-30

Fig. 44. Package outline SOT8113 (WLCSP4)

12. Abbreviations

Table 12. Abbreviations

Acronym	Description
AEC	Automotive Electronics Council
CDM	Charged Device Model
ESD	ElectroStatic Discharge
FET	Field-Effect Transistor
HBM	Human Body Model
IEC	International Electrotechnical Commission
JEDEC	Joint Electron Device Engineering Council
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
PCB	Printed Circuit Board
PMOS	P-channel Metal-Oxide Semiconductor

13. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NID1101 v.1	20251021	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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Date of release: 21 October 2025

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