1. General description

NPN/PNP Resistor-Equipped double Transistors (RET) family in a very small SOT363 (SC-88) Surface-Mounted Device (SMD) plastic package.

Table 1. Product overview

<table>
<thead>
<tr>
<th>Type number</th>
<th>R1</th>
<th>R2</th>
<th>Package</th>
<th>NPN/NPN complement:</th>
<th>PNP/PNP complement:</th>
</tr>
</thead>
<tbody>
<tr>
<td>NHUMD10</td>
<td>2.2</td>
<td>47</td>
<td>SOT363</td>
<td>NHUMH10</td>
<td>NHUMB10</td>
</tr>
<tr>
<td>NHUMD13</td>
<td>4.7</td>
<td>47</td>
<td>SC-88</td>
<td>NHUMH13</td>
<td>NHUMB13</td>
</tr>
<tr>
<td>NHUMD9</td>
<td>10</td>
<td>47</td>
<td></td>
<td>NHUMH9</td>
<td>NHUMB9</td>
</tr>
</tbody>
</table>

2. Features and benefits

- 100 mA output current capability
- High breakdown voltage
- Built-in resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- AEC-Q101 qualified

3. Applications

- Digital applications
- Cost saving alternative for BC846 / BC856 series in digital applications
- Controlling IC inputs
- Switching loads

4. Quick reference data

Table 2. Quick reference data

$T_{amb} = 25 \, ^{\circ}C$ unless otherwise specified.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CEO}$</td>
<td>collector-emitter voltage</td>
<td>open base</td>
<td>-</td>
<td>-</td>
<td>80</td>
<td>V</td>
</tr>
<tr>
<td>$I_O$</td>
<td>output current</td>
<td></td>
<td>-</td>
<td>-</td>
<td>100</td>
<td>mA</td>
</tr>
</tbody>
</table>
5. Pinning information

Table 3. Pinning

<table>
<thead>
<tr>
<th>Pin</th>
<th>Symbol</th>
<th>Description</th>
<th>Simplified outline</th>
<th>Graphic symbol</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>GND1</td>
<td>GND (emitter) TR1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>I1</td>
<td>input (base) TR1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>O2</td>
<td>output (collector) TR2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>GND2</td>
<td>GND (emitter) TR2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>I2</td>
<td>input (base) TR2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>O1</td>
<td>output (collector) TR1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

6. Ordering information

Table 4. Ordering information

<table>
<thead>
<tr>
<th>Type number</th>
<th>Package</th>
<th>Description</th>
<th>Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>NHUMD10</td>
<td>SC-88</td>
<td>plastic surface-mounted package; 6 leads</td>
<td>SOT363</td>
</tr>
<tr>
<td>NHUMD13</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NHUMD9</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

7. Marking

Table 5. Marking

<table>
<thead>
<tr>
<th>Type number</th>
<th>Marking code [1]</th>
</tr>
</thead>
<tbody>
<tr>
<td>NHUMD10</td>
<td>6P%</td>
</tr>
<tr>
<td>NHUMD13</td>
<td>6R%</td>
</tr>
<tr>
<td>NHUMD9</td>
<td>6N%</td>
</tr>
</tbody>
</table>

[1] % = placeholder for manufacturing site code
## 8. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

**Symbol** 
**Parameter** 
**Conditions** 
**Min** 
**Max** 
**Unit**  

### Per transistor, for the PNP transistor with negative polarity

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CBO}$</td>
<td>collector-base voltage</td>
<td>open emitter</td>
<td>-</td>
<td>80</td>
<td>V</td>
</tr>
<tr>
<td>$V_{CEO}$</td>
<td>collector-emitter voltage</td>
<td>open base</td>
<td>-</td>
<td>80</td>
<td>V</td>
</tr>
<tr>
<td>$V_{EBO}$</td>
<td>emitter-base voltage</td>
<td>open collector</td>
<td>-</td>
<td>7</td>
<td>V</td>
</tr>
</tbody>
</table>

### Input voltage

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{I}$</td>
<td>input voltage</td>
<td>NHUMD10, TR1 (NPN)</td>
<td>-7</td>
<td>+20</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>NHUMD10, TR2 (PNP)</td>
<td>-20</td>
<td>+7</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>NHUMD13, TR1 (NPN)</td>
<td>-7</td>
<td>+30</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>NHUMD13, TR2 (PNP)</td>
<td>-30</td>
<td>+7</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>NHUMD9, TR1 (NPN)</td>
<td>-7</td>
<td>+40</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>NHUMD9, TR2 (PNP)</td>
<td>-40</td>
<td>+7</td>
<td>V</td>
</tr>
</tbody>
</table>

### Output current

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{O}$</td>
<td>output current</td>
<td>-</td>
<td>100</td>
<td>mA</td>
<td></td>
</tr>
</tbody>
</table>

### Total power dissipation

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_{tot}$</td>
<td>total power dissipation</td>
<td>$T_{amb} \leq 25 \degree C$</td>
<td>[1]</td>
<td>-</td>
<td>235</td>
</tr>
</tbody>
</table>

### Per device

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_{tot}$</td>
<td>total power dissipation</td>
<td>$T_{amb} \leq 25 \degree C$</td>
<td>[1]</td>
<td>-</td>
<td>350</td>
</tr>
<tr>
<td>$T_{j}$</td>
<td>junction temperature</td>
<td>-</td>
<td>150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>$T_{amb}$</td>
<td>ambient temperature</td>
<td>-55</td>
<td>150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>$T_{stg}$</td>
<td>storage temperature</td>
<td>-65</td>
<td>150</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

[1] Device mounted on an FR4 Printed-Circuit-Board (PCB); single-sided copper; tin-plated and standard footprint.

---

### FR4 PCB, single-sided copper, standard footprint

**Fig. 1.** Per device: Power derating curves for SOT363 (SC-88)
9. Thermal characteristics

Table 7. Thermal characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Per transistor</td>
<td>$R_{th(j-a)}$</td>
<td>thermal resistance from junction to ambient</td>
<td>in free air</td>
<td>[1]</td>
<td>-</td>
<td>532</td>
</tr>
<tr>
<td>Per transistor</td>
<td>$R_{th(j-sp)}$</td>
<td>thermal resistance from junction to solder point</td>
<td>-</td>
<td>-</td>
<td>150</td>
<td>K/W</td>
</tr>
<tr>
<td>Per device</td>
<td>$R_{th(j-a)}$</td>
<td>thermal resistance from junction to ambient</td>
<td>in free air</td>
<td>[1]</td>
<td>-</td>
<td>358</td>
</tr>
</tbody>
</table>

[1] Device mounted on an FR4 Printed-Circuit-Board (PCB); single-sided copper; tin-plated and standard footprint.

![Fig. 2](attachment:fig2.png)

FR4 PCB, single-sided copper, tin-plated and standard footprint

Fig. 2. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values
## 10. Characteristics

### Table 8. Characteristics

\( T_{\text{amb}} = 25 \, ^\circ\text{C} \) unless otherwise specified.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Per transistor, for the PNP transistor with negative polarity</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{(BR)CBO} )</td>
<td>collector-base breakdown voltage</td>
<td>( I_C = 100 \mu A; , I_E = 0 , A )</td>
<td>80</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>( V_{(BR)CEO} )</td>
<td>collector-emitter breakdown voltage</td>
<td>( I_C = 2 , mA; , I_B = 0 , A )</td>
<td>80</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>( I_{CBO} )</td>
<td>collector-base cut-off current</td>
<td>( V_{CB} = 80 , V; , I_E = 0 , A )</td>
<td>-</td>
<td>-</td>
<td>100</td>
<td>nA</td>
</tr>
<tr>
<td>( I_{CEO} )</td>
<td>collector-emitter cut-off current</td>
<td>( V_{CE} = 60 , V; , I_B = 0 , A )</td>
<td>-</td>
<td>-</td>
<td>100</td>
<td>nA</td>
</tr>
<tr>
<td>( I_{EBO} )</td>
<td>emitter-base cut-off current</td>
<td>( V_{EB} = 7 , V; , I_C = 0 , A )</td>
<td>-</td>
<td>-</td>
<td>270</td>
<td>µA</td>
</tr>
<tr>
<td>NHUMD10</td>
<td></td>
<td></td>
<td>-</td>
<td>-</td>
<td>260</td>
<td>µA</td>
</tr>
<tr>
<td>NHUMD13</td>
<td></td>
<td></td>
<td>-</td>
<td>-</td>
<td>230</td>
<td>µA</td>
</tr>
<tr>
<td>( h_{FE} )</td>
<td>DC current gain</td>
<td>( V_{CE} = 5 , V; , I_C = 10 , mA )</td>
<td>100</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>( V_{CEsat} )</td>
<td>collector-emitter saturation voltage</td>
<td>( I_C = 10 , mA; , I_E = 0.5 , mA )</td>
<td>-</td>
<td>-</td>
<td>100</td>
<td>mV</td>
</tr>
<tr>
<td>( V_{I(off)} )</td>
<td>off-state input voltage</td>
<td>( V_{CE} = 5 , V; , I_C = 100 \mu A )</td>
<td>-</td>
<td>595</td>
<td>500</td>
<td>mV</td>
</tr>
<tr>
<td>NHUMD10</td>
<td></td>
<td></td>
<td>-</td>
<td>625</td>
<td>500</td>
<td>mV</td>
</tr>
<tr>
<td>NHUMD13</td>
<td></td>
<td></td>
<td>-</td>
<td>690</td>
<td>500</td>
<td>mV</td>
</tr>
<tr>
<td>( V_{I(on)} )</td>
<td>on-state input voltage</td>
<td>( V_{CE} = 0.3 , V; , I_C = 10 , mA )</td>
<td>1.2</td>
<td>0.81</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>NHUMD10</td>
<td></td>
<td></td>
<td>1.4</td>
<td>0.95</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>NHUMD13</td>
<td></td>
<td></td>
<td>1.6</td>
<td>1.22</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>NHUMD9</td>
<td></td>
<td></td>
<td>3.3</td>
<td>4.7</td>
<td>6.1</td>
<td>kΩ</td>
</tr>
<tr>
<td>R1</td>
<td>bias resistor 1 (input)</td>
<td></td>
<td>1.54</td>
<td>2.2</td>
<td>2.86</td>
<td>kΩ</td>
</tr>
<tr>
<td>NHUMD10</td>
<td></td>
<td></td>
<td>17</td>
<td>21</td>
<td>26</td>
<td></td>
</tr>
<tr>
<td>NHUMD13</td>
<td></td>
<td></td>
<td>8</td>
<td>10</td>
<td>12</td>
<td>kΩ</td>
</tr>
<tr>
<td>NHUMD9</td>
<td></td>
<td></td>
<td>3.7</td>
<td>4.7</td>
<td>5.7</td>
<td></td>
</tr>
<tr>
<td>R2/R1</td>
<td>bias resistor ratio</td>
<td></td>
<td>17</td>
<td>21</td>
<td>26</td>
<td></td>
</tr>
<tr>
<td>NHUMD10</td>
<td></td>
<td></td>
<td>1</td>
<td>3.7</td>
<td>4.7</td>
<td></td>
</tr>
<tr>
<td>NHUMD13</td>
<td></td>
<td></td>
<td>8</td>
<td>10</td>
<td>12</td>
<td></td>
</tr>
<tr>
<td>NHUMD9</td>
<td></td>
<td></td>
<td>3.7</td>
<td>4.7</td>
<td>5.7</td>
<td></td>
</tr>
<tr>
<td>( f_T )</td>
<td>transition frequency</td>
<td>( V_{CE} = 5 , V; , I_C = 10 , mA; , f = 100 , MHz )</td>
<td>-</td>
<td>170</td>
<td>-</td>
<td>MHz</td>
</tr>
<tr>
<td>TR1 (NPN)</td>
<td></td>
<td></td>
<td>-</td>
<td>150</td>
<td>-</td>
<td>MHz</td>
</tr>
<tr>
<td>( C_C )</td>
<td>collector capacitance</td>
<td>( V_{CB} = 10 , V; , I_E = I_B = 0 , A; , f = 1 , MHz )</td>
<td>-</td>
<td>-</td>
<td>2.5</td>
<td>pF</td>
</tr>
<tr>
<td>TR1 (NPN)</td>
<td></td>
<td></td>
<td>-</td>
<td>-</td>
<td>3</td>
<td>pF</td>
</tr>
<tr>
<td>TR2 (PNP)</td>
<td></td>
<td></td>
<td>-</td>
<td>-</td>
<td>2.5</td>
<td>pF</td>
</tr>
</tbody>
</table>

[1] See section "Test information" for resistor calculation and test conditions
NHUMD10/13/9 series
80 V, 100 mA NPN/PNP resistor-equipped double transistors

Fig. 3. NHUMD10, TR1 (NPN): DC current gain as a function of collector current; typical values

\[ h_{FE} = 5 \text{ V} \]

(1) \( T_{\text{amb}} = 100 \degree \text{C} \)
(2) \( T_{\text{amb}} = 25 \degree \text{C} \)
(3) \( T_{\text{amb}} = -40 \degree \text{C} \)

Fig. 4. NHUMD10, TR1 (NPN): Collector current as a function of collector-emitter voltage; typical values

\[ I_{C} \text{ (A)} \]

T_{\text{amb}} = 25 \degree \text{C}

Fig. 5. NHUMD10, TR1 (NPN): On-state input voltage as a function of collector current; typical values

\[ V_{\text{on}} (\text{V}) \]

\[ V_{\text{CE}} = 0.3 \text{ V} \]

(1) \( T_{\text{amb}} = -40 \degree \text{C} \)
(2) \( T_{\text{amb}} = 25 \degree \text{C} \)
(3) \( T_{\text{amb}} = 100 \degree \text{C} \)

Fig. 6. NHUMD10, TR1 (NPN): Off-state input voltage as a function of collector current; typical values

\[ V_{\text{off}} (\text{V}) \]

\[ V_{\text{CE}} = 5 \text{ V} \]

(1) \( T_{\text{amb}} = -40 \degree \text{C} \)
(2) \( T_{\text{amb}} = 25 \degree \text{C} \)
(3) \( T_{\text{amb}} = 100 \degree \text{C} \)
**Fig. 7.** NHUMD10, TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values

$$V_{CE} = 10$$

(1) $T_{amb} = 100$ °C
(2) $T_{amb} = 25$ °C
(3) $T_{amb} = -40$ °C

**Fig. 8.** NHUMD10, TR1 (NPN): Collector capacitance as a function of collector-base voltage; typical values

$$C_C$$ (pF)

$$f = 1 \text{ MHz}$$

$T_{amb} = 25$ °C

**Fig. 9.** NHUMD10, TR2 (PNP): DC current gain as a function of collector current; typical values

$$h_{FE}$$

$$V_{CE} = -5$$ V

(1) $T_{amb} = 100$ °C
(2) $T_{amb} = 25$ °C
(3) $T_{amb} = -40$ °C

**Fig. 10.** NHUMD10, TR2 (PNP): Collector current as a function of collector-emitter voltage; typical values

$$I_C$$ (A)

$I_B = -0.6$ mA

$T_{amb} = 25$ °C
NHUMD10/13/9 series
80 V, 100 mA NPN/PNP resistor-equipped double transistors

**Fig. 11.** NHUMD10, TR2 (PNP): On-state input voltage as a function of collector current; typical values

\[ V_{CE} = -0.3 \text{ V} \]
(1) \( T_{amb} = -40 ^\circ \text{C} \)
(2) \( T_{amb} = 25 ^\circ \text{C} \)
(3) \( T_{amb} = 100 ^\circ \text{C} \)

**Fig. 12.** NHUMD10, TR2 (PNP): Off-state input voltage as a function of collector current; typical values

\[ V_{CE} = -5 \text{ V} \]
(1) \( T_{amb} = -40 ^\circ \text{C} \)
(2) \( T_{amb} = 25 ^\circ \text{C} \)
(3) \( T_{amb} = 100 ^\circ \text{C} \)

**Fig. 13.** NHUMD10, TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values

\[ I_{C}/I_{B} = 20 \]
(1) \( T_{amb} = 100 ^\circ \text{C} \)
(2) \( T_{amb} = 25 ^\circ \text{C} \)
(3) \( T_{amb} = -40 ^\circ \text{C} \)

**Fig. 14.** NHUMD10, TR2 (PNP): Collector capacitance as a function of collector-base voltage; typical values

\[ f = 1 \text{ MHz} \]
\[ T_{amb} = 25 ^\circ \text{C} \]
80 V, 100 mA NPN/PNP resistor-equipped double transistors

Fig. 15. NHUMD13, TR1 (NPN): DC current gain as a function of collector current; typical values

$V_{CE} = 5\, V$
(1) $T_{amb} = 100\, ^{\circ}C$
(2) $T_{amb} = 25\, ^{\circ}C$
(3) $T_{amb} = -40\, ^{\circ}C$

Fig. 16. NHUMD13, TR1 (NPN): Collector current as a function of collector-emitter voltage; typical values

$T_{amb} = 25\, ^{\circ}C$

Fig. 17. NHUMD13, TR1 (NPN): On-state input voltage as a function of collector current; typical values

$V_{CE} = 0.3\, V$
(1) $T_{amb} = -40\, ^{\circ}C$
(2) $T_{amb} = 25\, ^{\circ}C$
(3) $T_{amb} = 100\, ^{\circ}C$

Fig. 18. NHUMD13, TR1 (NPN): Off-state input voltage as a function of collector current; typical values

$V_{CE} = 5\, V$
(1) $T_{amb} = -40\, ^{\circ}C$
(2) $T_{amb} = 25\, ^{\circ}C$
(3) $T_{amb} = 100\, ^{\circ}C$
80 V, 100 mA NPN/PNP resistor-equipped double transistors

Fig. 19. NHUMD13, TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values

Fig. 20. NHUMD13, TR1 (NPN): Collector capacitance as a function of collector-base voltage; typical values

Fig. 21. NHUMD13, TR2 (PNP): DC current gain as a function of collector current; typical values

Fig. 22. NHUMD13, TR2 (PNP): Collector current as a function of collector-emitter voltage; typical values
80 V, 100 mA NPN/PNP resistor-equipped double transistors

**Fig. 23.** NHUMD13, TR2 (PNP): On-state input voltage as a function of collector current; typical values

\[ V_{CE} = -0.3 \text{ V} \]

- (1) \( T_{amb} = -40 \text{ °C} \)
- (2) \( T_{amb} = 25 \text{ °C} \)
- (3) \( T_{amb} = 100 \text{ °C} \)

**Fig. 24.** NHUMD13, TR2 (PNP): Off-state input voltage as a function of collector current; typical values

\[ V_{CE} = -5 \text{ V} \]

- (1) \( T_{amb} = -40 \text{ °C} \)
- (2) \( T_{amb} = 25 \text{ °C} \)
- (3) \( T_{amb} = 100 \text{ °C} \)

**Fig. 25.** NHUMD13, TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values

\[ I_{c}/I_{b} = 20 \]

- (1) \( T_{amb} = 100 \text{ °C} \)
- (2) \( T_{amb} = 25 \text{ °C} \)
- (3) \( T_{amb} = -40 \text{ °C} \)

**Fig. 26.** NHUMD13, TR2 (PNP): Collector capacitance as a function of collector-base voltage; typical values

\( f = 1 \text{ MHz} \)

\( T_{amb} = 25 \text{ °C} \)
80 V, 100 mA NPN/PNP resistor-equipped double transistors

**Fig. 27.** NHUMD9, TR1 (NPN): DC current gain as a function of collector current; typical values

\[ V_{CE} = 5 \text{ V} \]
- (1) \( T_{\text{amb}} = 100 \text{ °C} \)
- (2) \( T_{\text{amb}} = 25 \text{ °C} \)
- (3) \( T_{\text{amb}} = -40 \text{ °C} \)

**Fig. 28.** NHUMD9, TR1 (NPN): Collector current as a function of collector-emitter voltage; typical values

**Fig. 29.** NHUMD9, TR1 (NPN): On-state input voltage as a function of collector current; typical values

\[ V_{CE} = 0.3 \text{ V} \]
- (1) \( T_{\text{amb}} = -40 \text{ °C} \)
- (2) \( T_{\text{amb}} = 25 \text{ °C} \)
- (3) \( T_{\text{amb}} = 100 \text{ °C} \)

**Fig. 30.** NHUMD9, TR1 (NPN): Off-state input voltage as a function of collector current; typical values

\[ V_{CE} = 5 \text{ V} \]
- (1) \( T_{\text{amb}} = -40 \text{ °C} \)
- (2) \( T_{\text{amb}} = 25 \text{ °C} \)
- (3) \( T_{\text{amb}} = 100 \text{ °C} \)
80 V, 100 mA NPN/PNP resistor-equipped double transistors

Fig. 31. NHUMD9, TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values

\[ V_{CE\text{sat}} (V) \]

- \( I_C/I_B = 20 \)
- (1) \( T_{\text{amb}} = 100 \, ^\circ\text{C} \)
- (2) \( T_{\text{amb}} = 25 \, ^\circ\text{C} \)
- (3) \( T_{\text{amb}} = -40 \, ^\circ\text{C} \)

Fig. 32. NHUMD9, TR1 (NPN): Collector capacitance as a function of collector-base voltage; typical values

\[ C_C (\text{pF}) \]

- \( f = 1 \, \text{MHz} \)
- \( T_{\text{amb}} = 25 \, ^\circ\text{C} \)

Fig. 33. NHUMD9, TR2 (PNP): DC current gain as a function of collector current; typical values

\[ h_{FE} \]

- \( V_{CE} = -5 \, V \)
- (1) \( T_{\text{amb}} = 100 \, ^\circ\text{C} \)
- (2) \( T_{\text{amb}} = 25 \, ^\circ\text{C} \)
- (3) \( T_{\text{amb}} = -40 \, ^\circ\text{C} \)

Fig. 34. NHUMD9, TR2 (PNP): Collector current as a function of collector-emitter voltage; typical values

\[ I_C (A) \]

- \( I_B = -0.520 \, mA \)
- \( -0.585 \, mA \)
- \( -0.650 \, mA \)
- \( -0.390 \, mA \)
- \( -0.325 \, mA \)
- \( -0.260 \, mA \)
- \( -0.195 \, mA \)
- \( -0.130 \, mA \)
- \( -0.065 \, mA \)

- \( T_{\text{amb}} = 25 \, ^\circ\text{C} \)
**NHUMD10/13/9 series**

80 V, 100 mA NPN/PNP resistor-equipped double transistors

---

Fig. 35. NHUMD9, TR2 (PNP): On-state input voltage as a function of collector current; typical values

\[ V_{CE} = -0.3 \text{ V} \]

1. \( T_{\text{amb}} = -40 ^\circ \text{C} \)
2. \( T_{\text{amb}} = 25 ^\circ \text{C} \)
3. \( T_{\text{amb}} = 100 ^\circ \text{C} \)

---

Fig. 36. NHUMD9, TR2 (PNP): Off-state input voltage as a function of collector current; typical values

\[ V_{CE} = -5 \text{ V} \]

1. \( T_{\text{amb}} = -40 ^\circ \text{C} \)
2. \( T_{\text{amb}} = 25 ^\circ \text{C} \)
3. \( T_{\text{amb}} = 100 ^\circ \text{C} \)

---

Fig. 37. NHUMD9, TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values

\[ I_c/I_B = 20 \]

1. \( T_{\text{amb}} = 100 ^\circ \text{C} \)
2. \( T_{\text{amb}} = 25 ^\circ \text{C} \)
3. \( T_{\text{amb}} = -40 ^\circ \text{C} \)

---

Fig. 38. NHUMD9, TR2 (PNP): Collector capacitance as a function of collector-base voltage; typical values

\[ f = 1 \text{ MHz} \]

\[ T_{\text{amb}} = 25 ^\circ \text{C} \]
Fig. 39. TR1 (NPN): Transition frequency as a function of collector current; typical values of built-in transistor

\[ f = 100 \text{ MHz} \]
\[ V_{CE} = 5 \text{ V} \]
\[ T_{amb} = 25 \degree C \]

Fig. 40. TR2 (PNP): Transition frequency as a function of collector current; typical values of built-in transistor

\[ f = 100 \text{ MHz} \]
\[ V_{CE} = -5 \text{ V} \]
\[ T_{amb} = 25 \degree C \]
11. Test information

Quality information
This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

Resistor calculation
• Calculation of bias resistor 1 (R1)
\[ R_1 = \frac{V(I_{I2}) - V(I_{I1})}{I_{I2} - I_{I1}} \]
• Calculation of bias resistor ratio (R2/R1)
\[ \frac{R_2}{R_1} = \frac{V(I_{I4}) - V(I_{I3})}{R_1 \cdot (I_{I4} - I_{I3})} \]

Resistor test conditions

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<th>R1 (kΩ)</th>
<th>R2 (kΩ)</th>
<th>Test conditions</th>
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<td></td>
<td>I1</td>
<td>I2</td>
<td>I3</td>
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<tr>
<td>Per transistor, for the PNP transistor with negative polarity</td>
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<td></td>
<td></td>
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<td>1.6 mA</td>
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<tr>
<td>NHUMD13</td>
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<td>NHUMD9</td>
<td>10</td>
<td>47</td>
<td>0.8 mA</td>
</tr>
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</table>

Fig. 41. TR1 (NPN): Resistor test circuit

Fig. 42. TR2 (PNP): Resistor test circuit

Table 9. Resistor test conditions
12. Package outline

Fig. 43. Package outline SOT363 (SC-88)

13. Soldering

Fig. 44. Reflow soldering footprint for SOT363 (SC-88)

Fig. 45. Wave soldering footprint for SOT363 (SC-88)
14. Revision history

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<th>Data sheet status</th>
<th>Change notice</th>
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<td>Product data sheet</td>
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15. Legal information

Data sheet status

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<td>This document contains data from the objective specification for product development.</td>
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<tr>
<td>Preliminary [short] data sheet</td>
<td>Qualification</td>
<td>This document contains data from the preliminary specification.</td>
</tr>
<tr>
<td>Product [short] data sheet</td>
<td>Production</td>
<td>This document contains the product specification.</td>
</tr>
</tbody>
</table>

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term “short data sheet” is explained in section “Definitions”.

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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