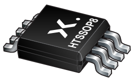


NEX90515-Q100

150 mA, 40 V ultra-low Iq (5.3 µA) low-dropout voltage regulator

Rev. 1 — 12 November 2024 **Product data sheet**

1. General description

The NEX90515-Q100 device is a low-dropout (LDO) linear regulator designed for applications with input voltages of up to 40 V. It features a typical quiescent current (I_Q) of only 5.3 µA at light load and a typical shutdown current (I_{SHUT}) of 300 nA when disabled. This makes the device ideal for powering always-on components, such as microcontrollers (MCUs) and Controller Area Network (CAN) or Local Interconnect Network (LIN) transceivers in standby or CAN-wake systems.

In battery-powered automotive applications, low I_Q and I_{SHUT} are critical for saving energy and extending battery life. Always-on systems require ultra-low I_Q across an extended temperature range to ensure sustained operation when the vehicle ignition is off. In CAN-wake systems or certain sleep modes, maintaining an ultralow I_{SHUT} is essential to minimize battery consumption even when the system is in sleep or disabled mode.

The device features integrated protections for shortcircuit, over-current, and thermal shutdown. It operates within an ambient temperature range of -40 °C to 125 °C and a junction temperature range of -40 °C to 150 °C. Additionally, this device is available in an enhanced thermal package, HTSSOP8.

Table 1. Device information

Part number	Package	Body size (nom)
NEX90515-Q100	HTSSOP8	3.0 mm x 3.0 mm

2. Features and benefits

- AEC-Q100 qualified for automotive applications
  - Temperature grade 1 (T_{amb}): -40 °C to 125 °C
  - Junction temperature (T_J): -40 °C to 150 °C
- Input voltage range: 3 V to 40 V (45 V transient)
- Output voltage range: 3.3 V and 5 V (fixed)
- Output voltage accuracy: ±2% (max)
- Maximum output current: 150 mA
- Low dropout voltage:
  - 230 mV typical at 150 mA (V_{OUT} = 5 V)
- Low quiescent current (I_Q):
  - 5.3 µA typical at light loads
  - 300 nA typical shutdown current
- Stable with a wide range of ceramic output-stability cap:
  - ESR from 0.001 Ω to 2 Ω; output cap of 1 µF to 220 µF
- Integrated various fault protections:
  - Thermal shutdown
  - Short-circuit and over-current protection
- Enhanced thermal package available:
  - HTSSOP8, $R_{\theta JA}$= 62.3 °C/W

3. Applications

- Body control modules (BCM)
- Automotive lighting
- Automotive head units & cluster
- Telematics control units
- EV/HEV power train

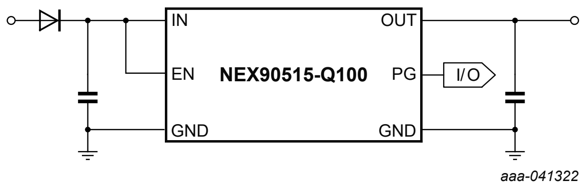


Fig. 1. Typical application

4. Ordering information

Table 2. Ordering information

Type number	Package			
	Temperature range (T_J)	Name	Description	Version
NEX90515APA-Q100	-40 °C to +150 °C	HTSSOP8	Plastic, thermal enhanced thin shrink small outline package; 8 leads,0.65 mm pitch, 3 mm × 3 mm × 1.1 mm body	SOT8062-1
NEX90515BPA-Q100	-40 °C to +150 °C	HTSSOP8	Plastic, thermal enhanced thin shrink small outline package; 8 leads,0.65 mm pitch, 3 mm × 3 mm × 1.1 mm body	SOT8062-1

5. Marking

Table 3. Marking codes

Type number	Marking code
NEX90515APA-Q100	N133P
NEX90515BPA-Q100	N150P

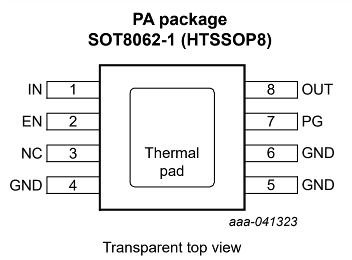
6. Device comparison

Table 4. Device comparison

Type number	Package	Output voltage	Power-good (PG)
NEX90515APA-Q100	HTSSOP8	3.3 V	Y
NEX90515BPA-Q100	HTSSOP8	5 V	Y

7. Pin configuration and description

7.1. Pin configuration



7.2. Pin description

Table 5. Pin description

Symbol	Pin	I/O	Description
IN	1	I	The input power-supply voltage pin should use the recommended value or a larger ceramic capacitor from IN to ground for optimal transient response and minimal input impedance. Place the input capacitor as close to the device's input as possible.
EN	2	I	The enable logic pin activates the device when at a high level and disables it at a low level. If this pin is connected to the IN pin or left floating (a pull-up resistor is not required), the device will be enabled.
NC	3	-	Not connected internally. This pin is not connected internally and can be tied to the ground plane to enhance thermal dissipation.
GND	4, 5, 6	G	Ground pin. Connect this pin to the thermal pad with a low-impedance connection.
PG	7	O	The power good pin (for the PG version) is an open-drain pin that should be connected to V_{OUT} or external voltage source (< 5.5 V) through an external pull-up resistor. V_{PG} is at a logic high level when V_{OUT} exceeds the power-good threshold.
OUT	8	O	The regulated output voltage pin requires a capacitor from OUT to ground for stability. For optimal transient response, use the recommended nominal value or a larger ceramic capacitor from OUT to ground. Place the output capacitor as close to the device's output as possible. If using a high ESR capacitor, decouple the output with a 100 nF ceramic capacitor.
Thermal pad	pad	-	The exposed thermal pad should be soldered to GND for improved thermal performance.

8. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).[1]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IN}	input voltage		-0.3	+45	V
V_{EN}	enable voltage		-0.3	+45	V
V_{OUT}	output voltage		-0.3	+6.6	V
V_{PG}	power good voltage		-0.3	+6.6	V
T_J	operating junction temperature		-40	+150	°C
T_{amb}	operating ambient temperature		-40	+125	°C
T_{stg}	storage temperature		-65	+165	°C

[1] Stresses beyond those conditions under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

9. ESD ratings

		Conditions	Value	Unit
V_{ESD}	electrostatic discharge voltage	Human-body model (HBM), per AEC Q100-002 [1]	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	V

[1] AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

10. Thermal Information

Table 7. Thermal information

Thermal resistance according to JEDEC51-5 and -7.

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	junction to ambient thermal resistance	62.3	°C/W
$R_{\theta JC(top)}$	junction to case(top) thermal resistance	146.8	°C/W
$R_{\theta JB}$	junction to board thermal resistance	20.0	°C/W
Ψ_{JT}	junction to top char parameter	17.3	°C/W

11. Recommended operating conditions

Table 8. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	input voltage		3	-	40	V
V_{OUT}	output voltage		1.5	-	5.5	V
I_{OUT}	output current	[1]	-	-	150	mA
V_{EN}	enable voltage		0	-	40	V
V_{PG}	power good voltage		0	-	5.5	V
C_{IN}	input capacitance		-	2.2	-	µF
C_{OUT}	output capacitance	[2]	1	-	220	µF
ESR	output capacitor ESR requirements	[3]	0.001	-	2	Ω
T_{amb}	ambient temperature		-40	-	+125	°C
T_J	junction temperature		-40	-	+150	°C

[1] Maximum output current when device is not thermal shutdown.
[2] Effective output capacitance of 1 µF minimum required for stability.
[3] Relevant ESR value at f = 10 kHz, if using a large ESR capacitor it is recommended to decouple this with a 100 nF ceramic capacitor to improve transient performance.

12. Electrical characteristics

Table 9. Electrical characteristics

At recommended operating conditions; T_{amb} = -40 °C to +125 °C, T_J = -40 °C to +150 °C, C_{OUT} = 1 µF, V_{IN} = 13.5 V; I_{OUT} = 100 µA, V_{EN} = 2 V; (unless otherwise noted) voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = -40 °C to +125 °C			Unit
			Min	Typ[1]	Max	
Power supply						
V_{IN}	input voltage range	Fixed 3.3 V output, I_{OUT} = 1 mA	4	-	40	V
		Fixed 5V output, I_{OUT} = 1 mA	5.5	-	40	V
$V_{IN(UVLO)}$	under voltage lockout threshold	V_{IN} rising	2.53	2.72	2.87	V
		V_{IN} falling	2.30	2.46	2.60	V
		Hysteresis		230		mV
I_Q	quiescent current	V_{IN} = V_{OUT} + 500 mV to 40 V, I_{OUT} = 0 µA	-	5.3	10	µA
		V_{IN} = V_{OUT} + 500 mV to 40 V, I_{OUT} = 100 µA	-	8	15	µA
I_{SHUT}	shutdown current	V_{EN} = 0 V	-	0.3	1	µA

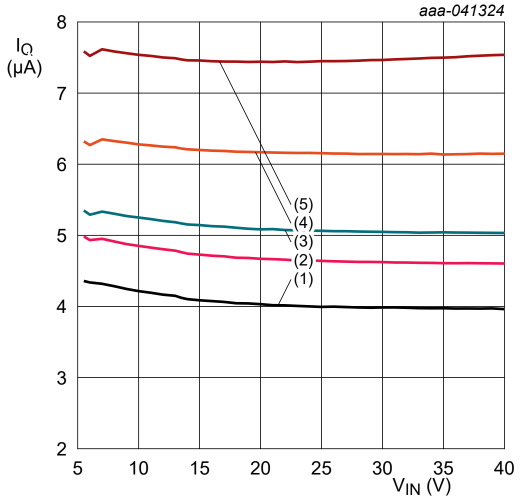
Symbol	Parameter	Conditions	T_{amb} = -40 °C to +125 °C			Unit
			Min	Typ[1]	Max	
Enable input (EN)						
V_{EN_L}	logic input low level		-	-	0.7	V
V_{EN_H}	logic input high level		2	-	-	V
I_{EN}	EN pin current	V_{EN} = V_{IN} = 13.5 V	-	-	50	nA
Output						
V_{OUT}	output accuracy	V_{IN} = 4.5 V to 40 V (V_{OUT} = 3.3 V); V_{IN} = 6 V to 40 V (V_{OUT} = 5 V); I_{OUT} = 100 µA to 150 mA	-2	-	2	%
$\Delta V_{OUT(\Delta VIN)}$	line regulation	V_{IN} = 4.5 V to 40 V (V_{OUT} = 3.3 V); V_{IN} = 6 V to 40 V (V_{OUT} = 5 V), I_{OUT} = 10 mA	-	-	10	mV
$\Delta V_{OUT(\Delta IOUT)}$	load regulation	V_{IN} = 13.5 V, I_{OUT} = 100 µA to 150 mA	-	-	40	mV
V_{DO}	dropout voltage	V_{OUT} = 3.3 V; I_{OUT} = 100 mA	-	190	300	mV
		I_{OUT} = 150 mA	-	290	450	
		V_{OUT} = 5 V; I_{OUT} = 100 mA	-	150	250	
		I_{OUT} = 150 mA	-	230	375	
I_{OUT}	output current	V_{IN} = V_{OUT} + 1 V	-	-	150	mA
I_{CL}	output current limit	V_{IN} = V_{OUT} + 1 V, output short to 90% × V_{OUT}	180	460	570	mA
PSRR	power-supply ripple rejection	V_{IN} = 13.5 V, V_{Ripple} = 0.5 V_{pp}, I_{OUT} = 10 mA, C_{OUT} = 2.2 µF, frequency = 100 Hz [2]	-	60	-	dB
Power good						
$V_{PG\_H(th)}$	power-good threshold	V_{OUT} rising	84	-	97	%V_{OUT}
		V_{OUT} falling	83	-	95	
V_{PG_HYST}	power-good hysteresis		-	2	-	%V_{OUT}
V_{PG_L}	PG pin low level output voltage	Sink 2 mA current	-	-	0.4	V
t_{DLY}	power-good delay time	PG pin from high state to low state	-	110	-	µs
Operating temperature range						
T_{SD}	junction thermal shutdown temperature	Rising junction temperature	-	175	-	°C
T_{HYST}	thermal shutdown hysteresis		-	20	-	°C

[1] All typical values are measured at T_{amb} = 25 °C.
[2] Guaranteed by bench test, not fully tested in production.

13. Typical characteristics

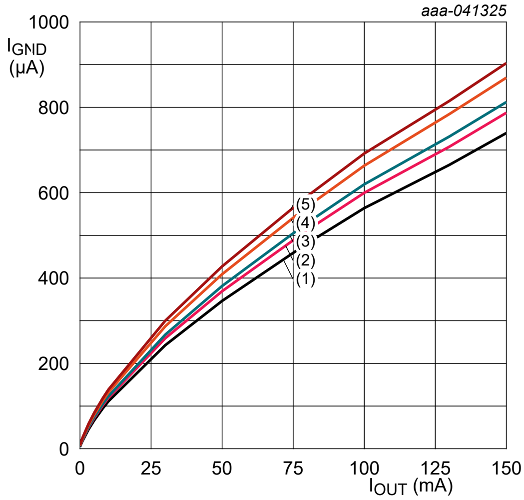
At recommended operating conditions, voltages are referenced to GND (ground = 0 V); typical values are at 25 °C (unless otherwise noted).

V_{IN} = 13.5 V, V_{EN} ≥ 2 V, C_{OUT} = 1 µF, V_{OUT} = 5 V, T_{amb} = -40 °C to 125 °C, unless otherwise specified.



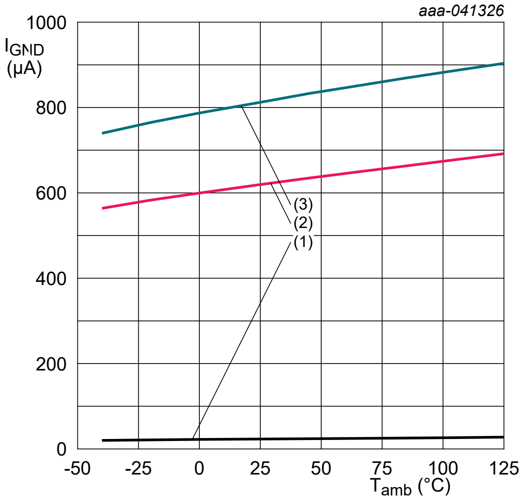
(1) T_{amb} = -40 °C
(2) T_{amb} = 0 °C
(3) T_{amb} = 25 °C
(4) T_{amb} = 85 °C
(5) T_{amb} = 125 °C

Fig. 2. Quiescent current vs input voltage



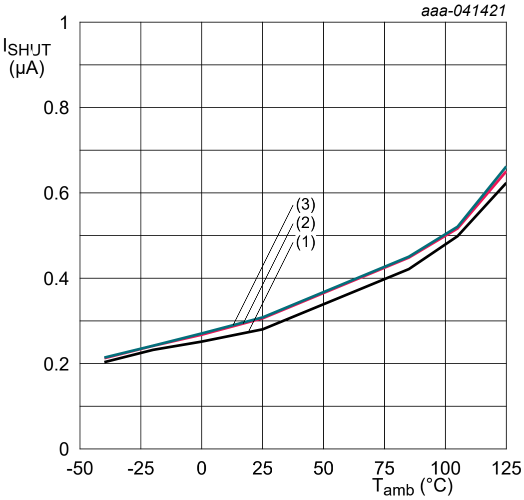
(1) T_{amb} = -40 °C
(2) T_{amb} = 0 °C
(3) T_{amb} = 25 °C
(4) T_{amb} = 85 °C
(5) T_{amb} = 125 °C

Fig. 3. Ground current vs output current



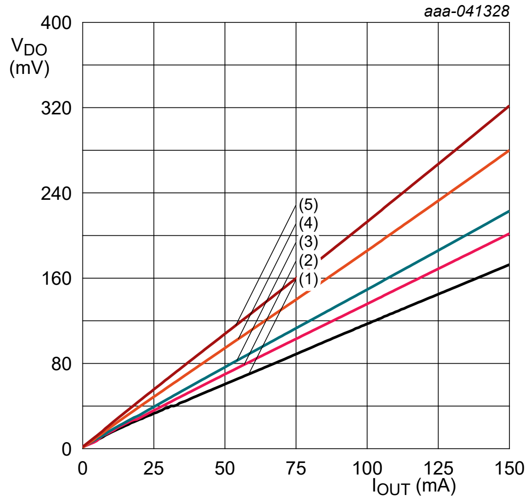
(1) I_{OUT} = 1 mA
(2) I_{OUT} = 100 mA
(3) I_{OUT} = 150 mA

Fig. 4. Ground current vs ambient temperature



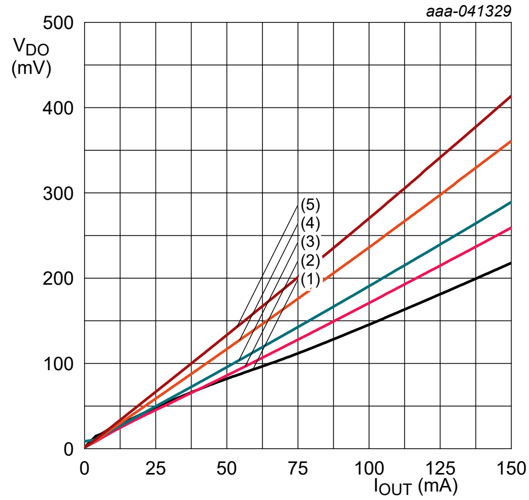
(1) V_{IN} =4 V
(2) V_{IN} = 13.5 V
(3) V_{IN} = 16 V

Fig. 5. Shutdown current vs ambient temperature



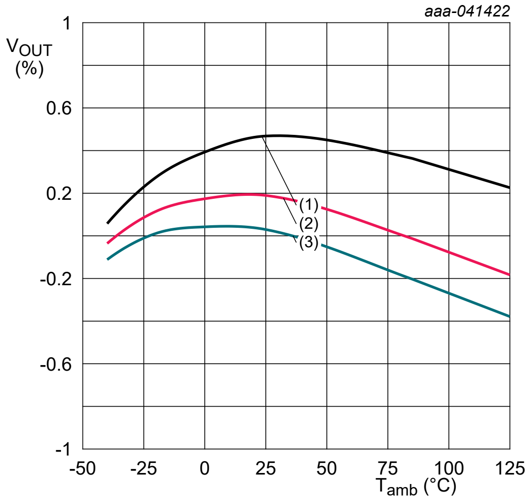
V_{OUT} = 5 V
(1) T_{amb} = -40 °C
(2) T_{amb} = 0 °C
(3) T_{amb} = 25 °C
(4) T_{amb} = 85 °C
(5) T_{amb} = 125 °C

Fig. 6. Dropout voltage vs output current



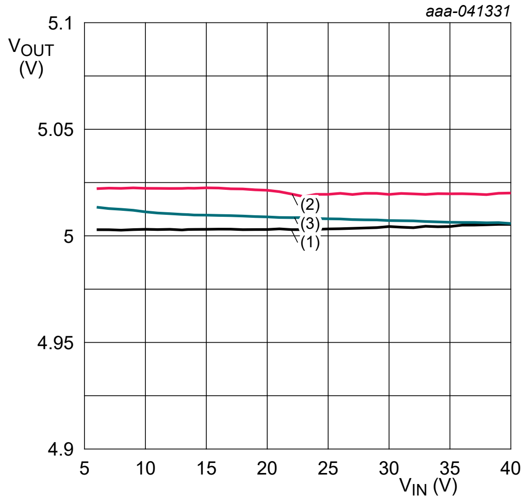
V_{OUT} = 3.3 V
(1) T_{amb} = -40 °C
(2) T_{amb} = 0 °C
(3) T_{amb} = 25 °C
(4) T_{amb} = 85 °C
(5) T_{amb} = 125 °C

Fig. 7. Dropout voltage vs output current



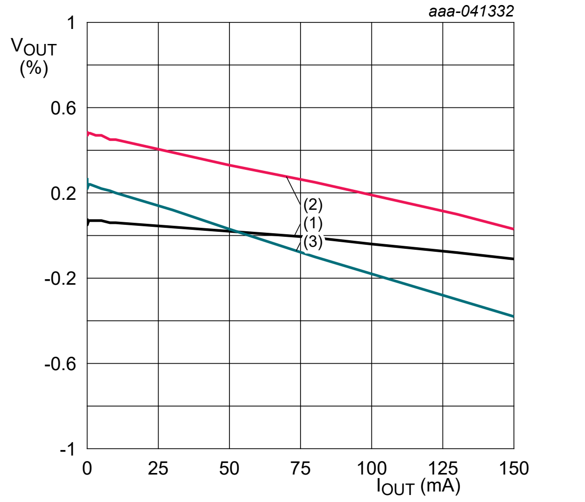
V_{OUT} = 5 V
(1) I_{OUT} = 100 µA
(2) I_{OUT} = 100 mA
(3) I_{OUT} =150 mA

Fig. 8. Output accuracy vs ambient temperature



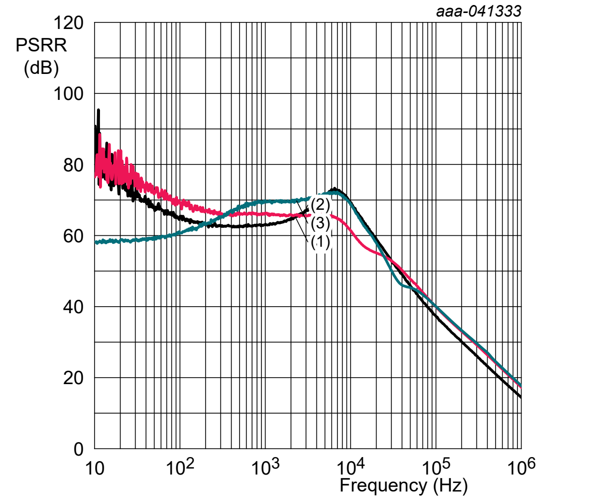
V_{OUT} = 5 V, I_{OUT} = 10 mA
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 125 °C

Fig. 9. Line regulation vs input voltage



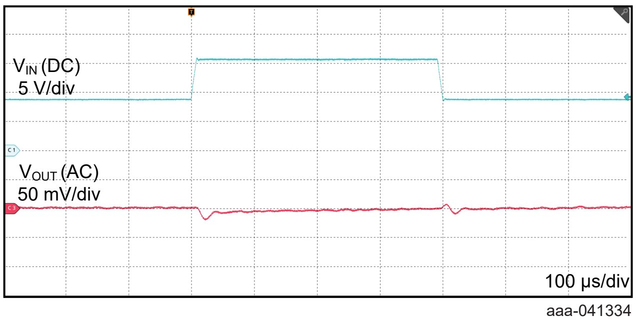
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 125 °C

Fig. 10. Load regulation (5V)



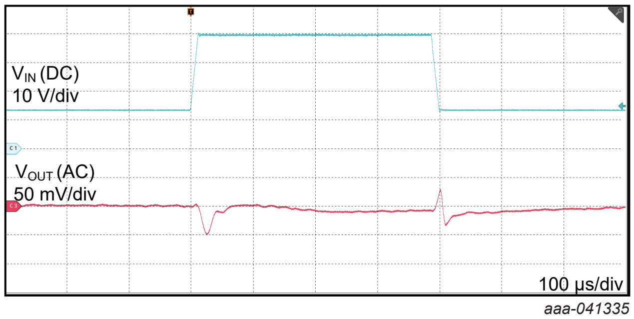
(1) I_{OUT} = 1 mA
(2) I_{OUT} = 10 mA
(3) I_{OUT} = 100 mA

Fig. 11. PSRR vs frequency



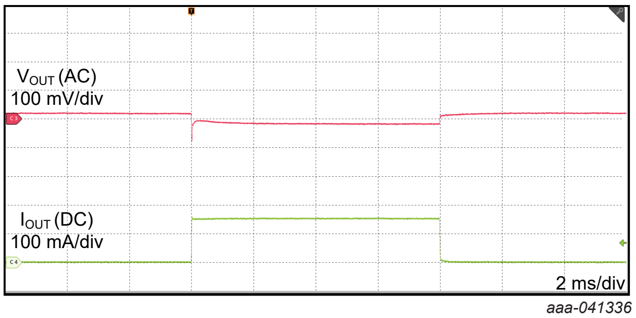
V_{IN} = 9 V to 16 V slew rate = 1 V/μs,
V_{OUT} = 5 V, I_{OUT} = 100 mA, C_{OUT} = 10 μF

Fig. 12. Line transient



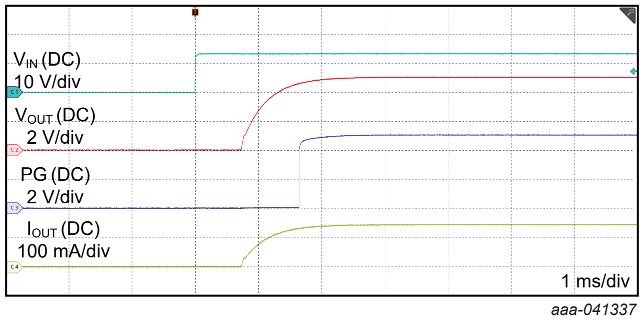
V_{IN} = 13.5 V to 40 V slew rate = 2 V/μs,
V_{OUT} = 5 V, I_{OUT} = 100 mA, C_{OUT} = 10 μF

Fig. 13. Line transient



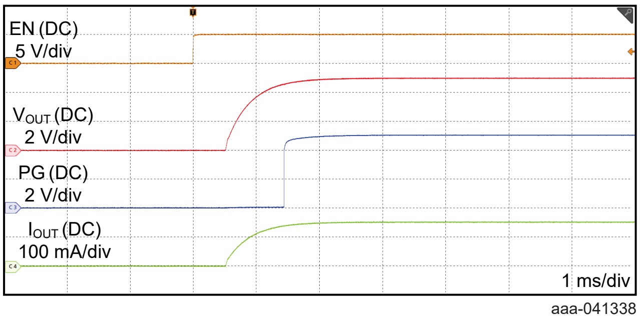
V_{IN} = 13.5 V, I_{OUT} = 0 mA to 150 mA,
slew rate = 0.2 A/μs, V_{OUT} = 5 V, C_{OUT} = 10 μF

Fig. 14. Load transient



V_{EN} = 5 V, I_{OUT} = 150 mA,
V_{OUT} = 5 V, C_{OUT} = 10 μF, V_{IN} from 0 to 13.5 V

Fig. 15. Start up by VIN



V_{IN} = 13.5 V, I_{OUT} = 150 mA,
V_{OUT} = 5 V, C_{OUT} = 10 μF, V_{EN} from 0 to 5 V

Fig. 16. Start up by EN

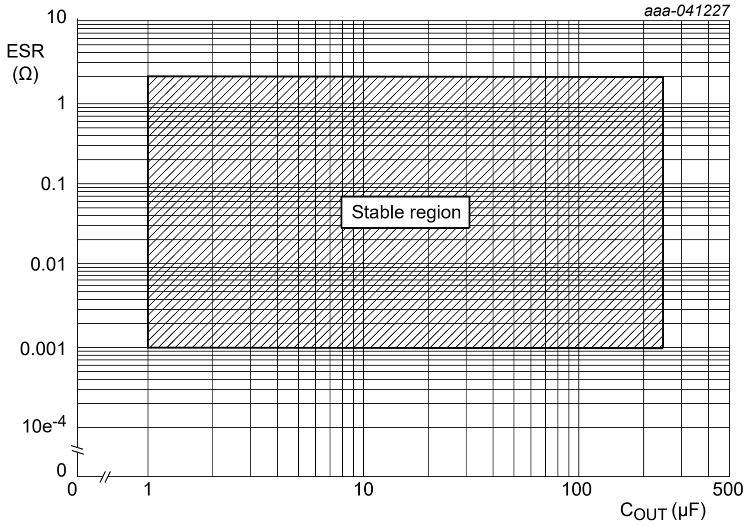


Fig. 17. Stability, ESR vs C_{OUT}

14. Detailed description

14.1. Overview

The NEX90515-Q100 is a low-dropout linear regulator (LDO) designed for direct connection to the battery in automotive applications. It has an input voltage range up to 40 V (with a maximum of 45 V), enabling it to withstand transients, such as load dumps, commonly encountered in automotive systems. With a typical quiescent current of only 5.3 μA at light loads and a shutdown current of 300 nA when disabled, this device is ideal for powering always-on components and CAN-wake systems. Additionally, it features thermal shutdown and short-circuit protection to safeguard against damage from overtemperature and over-current conditions.

14.2. Function block diagram

The NEX90515-Q100 function block diagram is shown in Fig. 18.

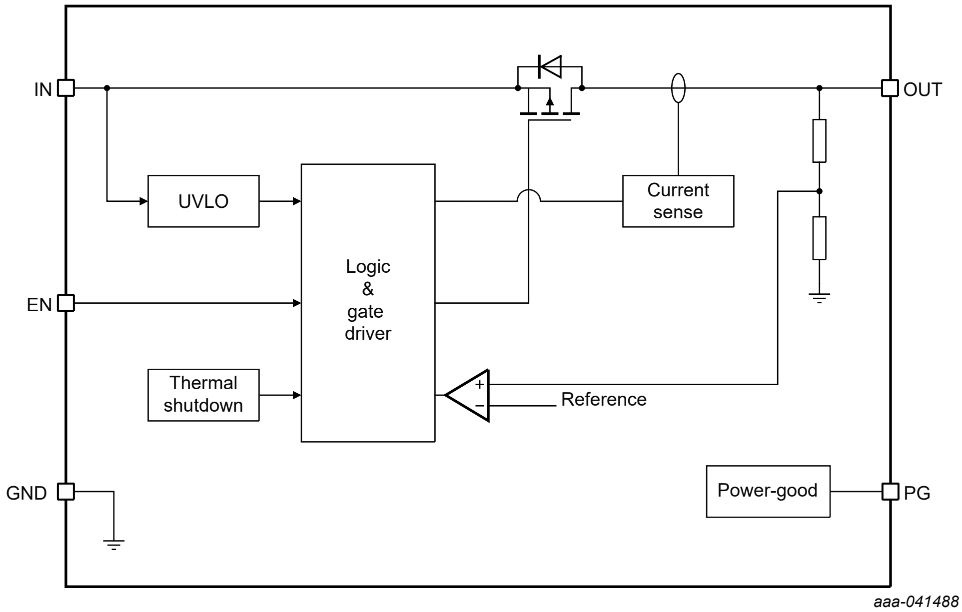


Fig. 18. Function block diagram

14.3. Feature description

14.3.1. Device Enable (EN)

The enable pin is a high-voltage-tolerant pin. A high input on EN actives the device and turns on the regulator. Connect this pin to an external microcontroller or a digital circuit to enable and disable the device or connect to the IN pin for self-bias applications. Always ensure that $V_{EN} \leq V_{IN}$.

14.3.2. Undervoltage lockout (UVLO)

An undervoltage lockout (UVLO) circuit prevents the device from operating when the input voltage falls below the typical falling threshold, $V_{IN(UVLO)}$. To avoid turning off the device during startup, the UVLO incorporates hysteresis, as specified in Table 9. If the input voltage experiences a negative transient that drops below the UVLO threshold and then recovers, the regulator will shut down and restart following the normal power-up sequence once the input voltage exceeds the required level.

14.3.3. Power good (PG)

The PG signal offers a straightforward solution for meeting demanding sequencing requirements, as it alerts when the output approaches its nominal value. An external pull-up resistor (R_{PG}) is needed for the regulated supply, as shown in Fig. 19. The PG voltage remains low until the regulated V_{OUT} exceeds approximately 90% of the set value.

The PG signal can be used to signal other devices in a system when the output voltage is near, at, or above the set output voltage. Fig. 19 illustrates the principle of PG operation. The PG signal includes an internal pull-up resistor to the nominal output voltage and is active high. The PG circuit sets the PG pin to a high-impedance state to indicate that the power is good.

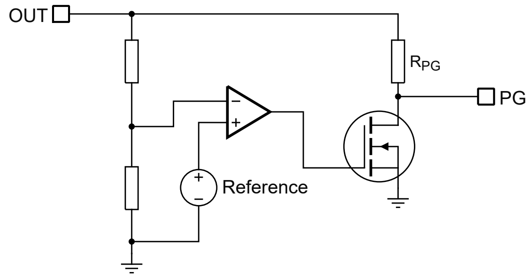


Fig. 19. Simplified power-good schematic

14.3.4. Current limit operation

The device features an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. When the device is in current limit mode, the output voltage is not regulated. During a current limit event, the device heats up due to increased power dissipation. When the device reaches the current limit (I_{CL}), the pass transistor dissipates power according to the formula [$V_{IN} – V_{OUT}$) × I_{CL}]. If thermal shutdown is triggered, the device will turn off. Once it cools down, the internal thermal shutdown circuit will turn the device back on. If the output current fault condition persists, the device will cycle between current limit and thermal shutdown.

14.3.5. Thermal shutdown

The NEX90515-Q100 integrates an internal temperature sensor to monitor the junction temperature (T_J). If T_J exceeds the thermal shutdown temperature (T_{SD}) of 175 °C, the device ceases operation. The device will resume functioning when T_J drops below the hysteresis threshold of approximately 20 °C.

Thermal shutdown may be triggered during startup due to large inrush currents charging substantial output capacitance, or under heavy loads where high ($V_{IN} – V_{OUT}$) regulations result in significant power dissipation across the die. Proper heat sinking should be considered in these high power dissipation scenarios.

15. Device functional modes

15.1. Device functional mode comparison

Table 10 shows the conditions that lead to the different modes of operation. See Table 8 for recommended operating conditions.

Table 10. Device functional mode comparison

Operating mode	Parameter			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal operation	$V_{IN} \geq V_{OUT(nom)} + V_{DO}$ and $V_{IN} \geq V_{IN(min)}$	$V_{EN} > V_{IH}$	$I_{OUT} \leq I_{OUT(max)}$	$T_J < T_{SD}$
Dropout operation	$V_{IN(min)} \leq V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{IH}$	$I_{OUT} \leq I_{OUT(max)}$	$T_J < T_{SD}$
Disabled mode	$V_{IN} < V_{ULVO}$	$V_{EN} < V_{IL}$	Not applicable	$T_J > T_{SD}$

15.2. Normal operation

The device works at nominal voltage when all the following conditions are met:

- The output current is less than the current limit
- The device junction temperature is less than thermal shutdown temperature
- The enable pin voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold

15.3. Dropout operation

The device operates in dropout mode when the input voltage falls below the target output voltage plus the dropout voltage, provided all other conditions for normal operation are met. In this mode, the output voltage tracks the input voltage. However, the transient performance significantly degrades because the pass element operates in the ohmic or triode region, acting like a switch. Line or load transients in dropout can cause substantial output voltage deviations. When the input voltage returns to a level equal to or greater than the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage may briefly overshoot while the device pulls the pass element back into the linear region.

16. Application implementation

16.1. Application information

The following section is a reference to simplify the system design with the NEX90515-Q100 typical application for external components calculation and selection.

16.2. Typical application

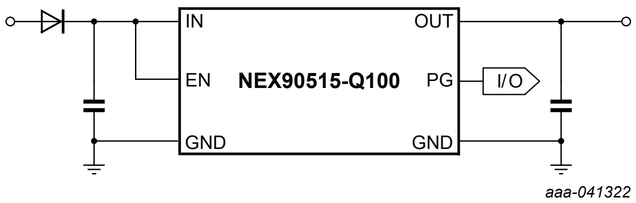


Fig. 20. NEX90515-Q100 typical application

16.2.1. Design requirements

A typical application is applied in automotive and power supply for MCU or CAN/LIN, which normally requires 5 V or 3.3 V output. The design parameters are listed in Table 11.

Table 11. Design parameters

Parameters	Values
Input voltage	6 V to 40 V
Output voltage	5 V
Output current	150 mA max
Input capacitor	10 µF
Output capacitor range	10 µF

16.2.2. Detailed design procedure

Input capacitor

The device requires an input decoupling capacitor, the value of which depends on the application. The typical recommended value for the decoupling capacitor is 2.2 µF. The voltage rating must be greater than the maximum input voltage.

Output capacitor

To ensure the stability of the NEX90515-Q100, the device requires an output capacitor with a value 1 µF to 220 µF from OUT to GND and ESR range between 0.001 Ω and 2 Ω. It is recommended to use a ceramic capacitor with low ESR to improve the load transient response and ripple performance.

17. Layout

17.1. Layout guidelines

For optimal overall performance, the following guidelines are recommended for LDO layout:

- Place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections.
- Ensure ground return connections for the input and output capacitors, as well as the LDO ground pin, are as close to each other as possible, connected by a wide copper surface on the component side.
- Avoid using vias and long traces to connect the input and output capacitors, as this can negatively impact system performance.
- In most applications, the ground plane is necessary to meet thermal requirements.

A ground reference plane should be either embedded in the PCB or located on the bottom side opposite the components. This reference plane helps ensure output voltage accuracy, shields against noise, and acts as a thermal plane to dissipate heat from the LDO device when connected to the thermal pad.

17.2. Layout examples

The figure below draws the layout example of NEX90515-Q100 (HTSSOP8) device.

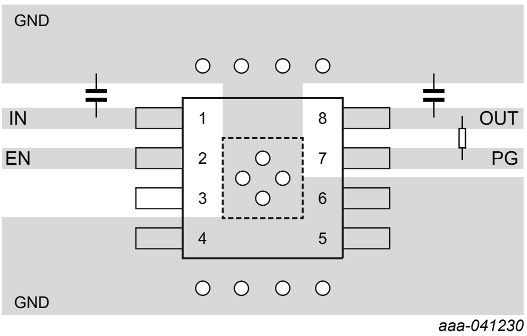
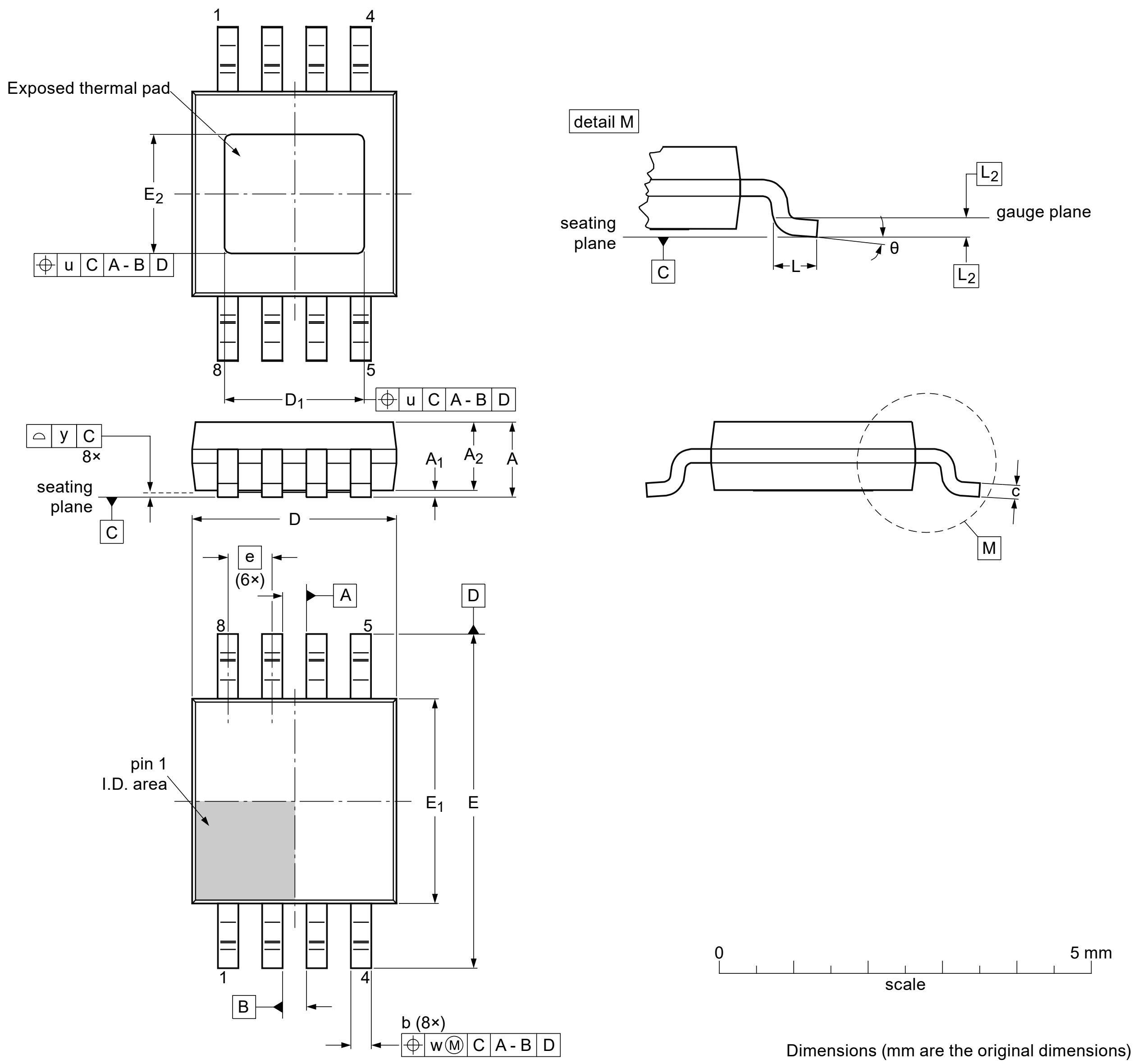


Fig. 21. NEX90515-Q100 layout example

18. Package outline

Plastic, thermal enhanced thin shrink small outline package; 8 leads, 0.65 mm pitch, 3 mm × 3 mm × 1.1 mm body

SOT8062-1



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	c	D	D_1	E	E_1	E_2	e	L	L_2	u	w	y	θ
mm	max	1.10	0.15	0.95	0.38	0.23	3.1	2.2	5.15	3.1	1.90	0.65 BSC	0.8	0.25 BSC	0.2	0.13	0.1	8°
	nom	-	-	0.85	-	-	3.0	-	4.90	3.0	-		-					-
	min	-	0.05	0.75	0.22	0.08	2.9	1.8	4.65	2.9	1.45		0.4					0°

Note:
1. Plastic protrusions of 0.15 mm maximum per side are not included for dimension D.
2. Plastic protrusions or interlead flash of 0.25 mm maximum per side are no included for dimension E_1.

sot8062-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8062-1		MO-187 (AA)				~~24-01-29~~ 24-10-29

Fig. 22. Package outline SOT8062-1 (HTSSOP8)

19. Abbreviations

Table 12. Abbreviations

Acronym	Description
AEC	Automotive Electronics Council
BCM	Body Control Modules
CAN	Controller Area Network
CDM	Charged Device Model
ESR	Equivalent Series Resistance
EV	Electric Vehicle
HBM	Human Body Model
HEV	Hybrid Electric Vehicle
LIN	Local Interconnect Network
LDO	Low-DropOut
MCU	MicroControllers
PG	Power-Good
UVLO	UnderVoltage LockOut

20. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NEX90515_Q100 v. 1	20241112	Preliminary data sheet	-	-

21. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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