NEX80806

Adaptive multi-mode flyback controller

Rev. 2.1 — 22 January 2026 Product data sheet

1. General description

The NEX80806 is an intelligent multi-mode PWM controller implemented with peak current mode control. As the load changes, it automatically switches mode between Continuous Conduction Mode (CCM), Quasi-Resonant (QR) mode, Discontinuous Conduction Mode (DCM) and Pulse Frequency Modulation (PFM) mode to maintain a high efficiency across the entire load range. To achieve an ultralow standby power, Burst Mode (BM) is implemented in very light load or no-load condition.

A peak load mode is implemented to support a peak output current requirement in a short period, which is normally required in power supply of PC, printer, etc.

The NEX80806 offers comprehensive protection including output OV/UV, V_{CC} OV/UV, OCP, line voltage BROWN-IN/OUT, secondary SR short, CS open/short, internal/external OTP, etc.

Furthermore, the spread spectrum and smart driving function can minimize the noise and improve EMI performance.

The NEX80806 comes in a cost-effective TSOT23-6 package.

2. Features and benefits

- Multimode support CCM/QR/DCM/PFM
- Peak load mode
- Valley switching operation in QR/DCM/PFM
- Burst mode with ultra-low operation current in light load and no load conditions
- 65kHz maximum frequency
- Internal Soft Start (SST)
- Output over voltage protection (OVP)
- Spread spectrum for better EMI
- Internal over temperature protection (OTP)
- External OTP by NTC resistor
- V_{CC} over/under voltage protection (V_{CC} OV/UV)
- Line voltage brown in /brown out (BNI/BNO)
- Output Short Circuit Protection (SCP)
- CS open/short protection
- Secondary Rectifier Short Protection (SRSP)
- Overload Protection (OLP)
- Over Current Protection (OCP) to meet LPS
- TSOT23-6 Package

3. Applications

- AC/DC adapters for portable devices
- Auxiliary power for industrial and home equipment
- Battery chargers for e-tools and e-bikes

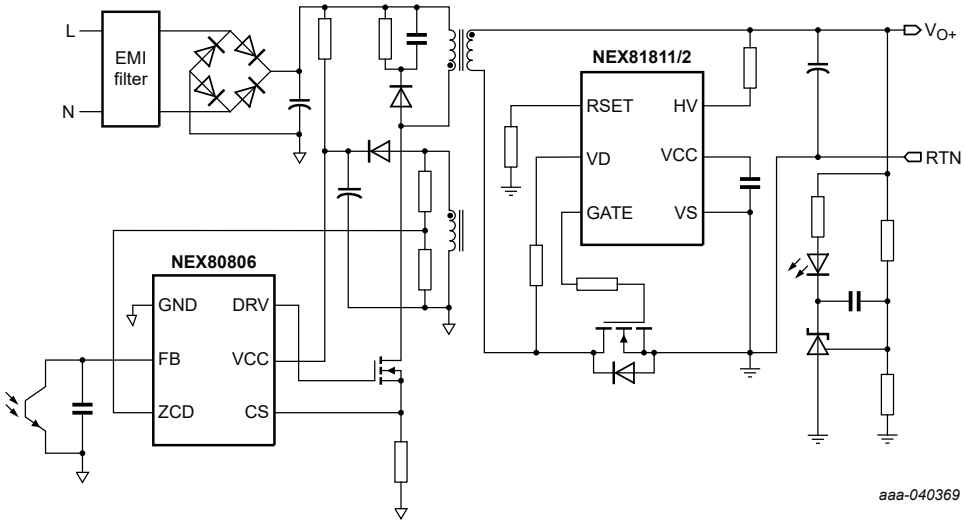


Fig. 1. Typical application

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NEX80806DA	-40 °C to +125 °C	TSOT23-6	Plastic, surface-mounted package; 6 leads	SOT8061-1

5. Marking

Table 2. Marking code

Type number	Marking code
NEX80806DA	NTG

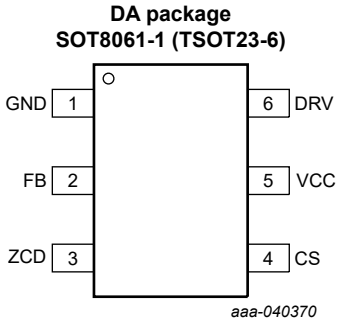
6. Device comparison

Table 3. Device comparison

Type number	F_{SW_MAX} (kHz)	Peak load mode	I_{out} limited by
NEX80806DA	65	yes	OCP

7. Pinning information

7.1. Pinning



7.2. Pin description

Pin		I/O	Description
Name	Number		
GND	1	PWR	Ground
FB	2	IN	Secondary side voltage feedback pin. Connect to the collector of the opto-coupler.
ZCD	3	IN	Auxiliary voltage sense, brown-in/-out and quasi-resonant valley detection.
CS	4	IN	Current sense pin, connect to the sense resistor of the MOSFET.
VCC	5	PWR	Supply input terminal
DRV	6	OUT	Gate drive output to drive the external MOSFET

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8. Product specifications

8.1. Limiting values

Table 4. Limiting values

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.3	40	V
DRV	gate drive voltage		-0.3	V_{DRV_H}	V
CS, FB, ZCD	CS, FB, ZCD voltage		-0.3	5.5	V
T_J	operating junction temperature		-40	T_{SD}	°C
ESD					
V_{ESD}	ESD voltage	HBM: ANSI/ESDA/JEDEC JS-001 class 2, all pins except CS	-2000	+2000	V
		HBM: ANSI/ESDA/JEDEC JS-001 class 1C, CS pin only	-1500	+1500	V
		CDM: ANSI/ESDA/JEDEC JS-002 class C2a	-500	+500	V

8.2. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	TSOT23	Unit
$R_{\Theta JA}$	junction-to-ambient thermal resistance	127	C/W

8.3. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		10	V_{CC_OVP}	V
CS, ZCD	CS, ZCD voltage		0	5	V
T_J	operating junction temperature		-40	125	°C

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8.4. Electrical characteristics

Table 7. Electrical characteristics

Where V_{CC} = 10 V to 28 V; T_J = -40 °C to 125 °C; typical values are measured at V_{CC} = 20 V, T_J = 25 °C (unless otherwise noted).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply (VCC pin)						
V_{CC_ON}	V_{CC} on threshold voltage		-	17	18	V
V_{CC_OFF}	V_{CC} off threshold voltage		-	8.4	-	V
V_{CC_HOLD}	V_{CC} hold threshold voltage		-	9	9.4	V
V_{CC_OVP}	V_{CC} OVP threshold voltage		25.5	28	30	V
V_{CC_DIS}	V_{CC} discharge threshold voltage		-	33	35	V
$V_{CC_DIS_HYS}$	V_{CC} discharge threshold hysteresis voltage		-	5	-	V
I_{DIS}	V_{CC} discharge current		-	5	-	mA
$I_{STARTUP}$	V_{CC} startup current		-	5	8	µA
I_{NORMAL}	V_{CC} normal operating current	V_{CC} = 20 V, F_{SW} = 65 kHz, 1 nF at DRV pin	-	1.25	1.75	mA
I_{BURST}	V_{CC} current in burst mode		-	270	350	µA
Feedback input (FB pin)						
V_{FB_OPEN}	FB pin open-circuit voltage		-	5	-	V
R_{FB}	FB internal pull-up resistor		-	28	-	kΩ
$V_{FB_BURST_OFF}$	FB voltage when DRV pulse is skipped		-	0.3	-	V
$V_{FB_BURST_ON}$	FB voltage when DRV pulse is resumed		-	0.35	-	V
V_{FB_OLP}	overload protection threshold voltage		-	3.5	-	V
t_{D_OLP}	overload protection deglitch time		-	50	-	ms
K_{FB}	divider ratio from FB to CS		-	5	-	V/V
t_{SS}	soft start time	0 to 0.4 V V_{CS}	-	4.3	-	ms
Current sense input (CS pin)						
T_{LEB_PWM}	leading edge blanking for PWM comparator		-	320	-	ns
$V_{CS_PWM_MAX}$	maximum current limit threshold for PWM comparator		0.365	0.4	0.43	V
T_{LEB_OCF}	leading edge blanking for OC fault protection		-	90	-	ns
V_{CS_OCF}	secondary rectifier (SR) short=circuit fault protection		0.61	0.65	0.7	V
t_{D_OCF}	SR short-circuit fault deglitch cycles		-	3	-	cycles
V_{CS_SHORT}	CS pin short detection threshold		-	0.04	-	V
$t_{BLK_CS_SHORT}$	CS pin short detection blanking time	I_{line} = 90 µA	-	4.5	-	µs
$t_{D_CS_SHORT}$	CS pin short fault deglitch cycles		-	3	-	cycles
Zero current detection (ZCD pin)						
I_{ZCD_VALLEY}	Valley detection threshold		-	9	-	µA
t_{W_VALLEY}	Valley window time		-	3	-	µs
I_{BNI}	Brown-in detection threshold	T_J = 25 °C	-	91	96	µA

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{BNO}	Brown-out detection threshold [1]		79	85	91	µA
t_{D_BNO}	Brown-out deglitch time		-	50	-	ms
V_{ZCD_OVP}	ZCD OVP threshold		3.3	3.6	3.8	V
$t_{D_ZCD_OVP}$	ZCD OVP deglitch time		-	7	-	cycles
V_{ZCD_SCP}	Output short-circuits protection threshold		-	1.2	-	V
$t_{D_ZCD_SCP}$	Output short-circuits protection deglitch time		-	7	-	cycles
t_{BLK_UVP}	UVP/SCP blanking time during softstart		-	20	-	ms
Gate Drive (DRV pin)						
V_{DRV_L}	DRV low level		-	-	0.2	V
V_{DRV_H}	DRV high level	V_{CC} = 12 V	8	-	-	V
	DRV high level clamp voltage	V_{CC} ≥ 15 V	-	11.5	-	V
t_r	DRV rising time	C_{load} = 1 nF	-	250	-	ns
t_f	DRV falling time	C_{load} = 1 nF	-	30	-	ns
Control law						
F_{MAX}	maximum switching frequency		60	65	70	kHz
F_{MIN}	minimum switching frequency		20	25	30	kHz
F_{PEAK}	maximum switching frequency in peak load mode		117	130	143	kHz
D_{MAX}	Maximum duty cycle		-	78	-	%
Over temperature protection						
T_{SD}	internal thermal shutdown threshold		-	155	-	°C
T_{SD_HYS}	internal thermal shutdown hysteresis		-	30	-	°C
V_{CS_OTP}	external OTP trigger voltage		-	V_{ZCD}/7	-	V
T_{D_OTP}	external OTP deglitch time		-	1.5	-	ms

[1] Guaranteed by design.

8.5. Typical characteristics

Table 8. Typical characteristics

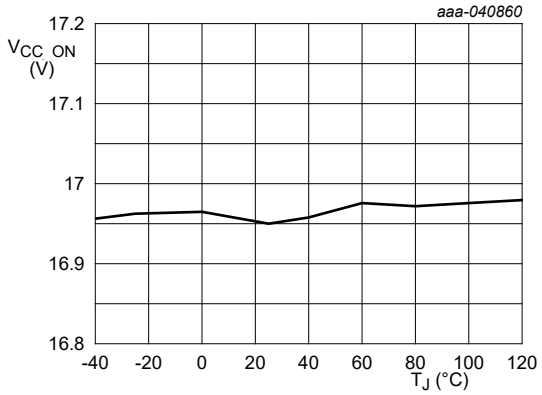

Fig. 2. V_{CC_ON} vs. junction temperature

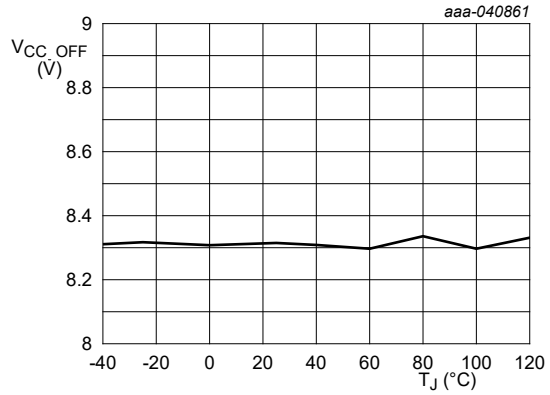

Fig. 3. V_{CC_OFF} vs. junction temperature

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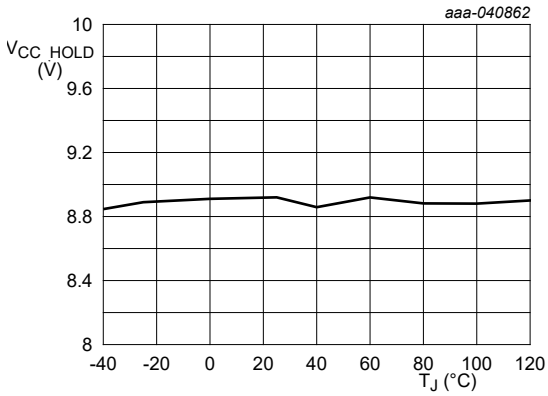


Fig. 4. V_{CC_HOLD} vs. junction temperature

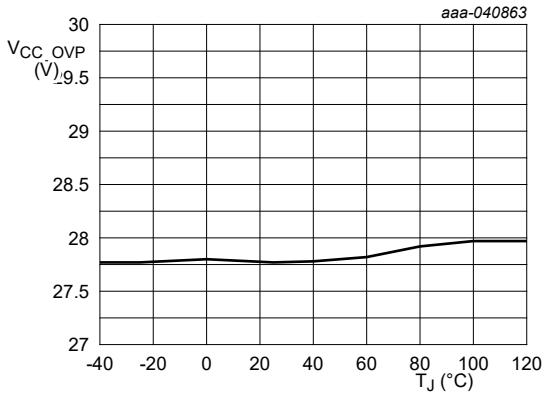
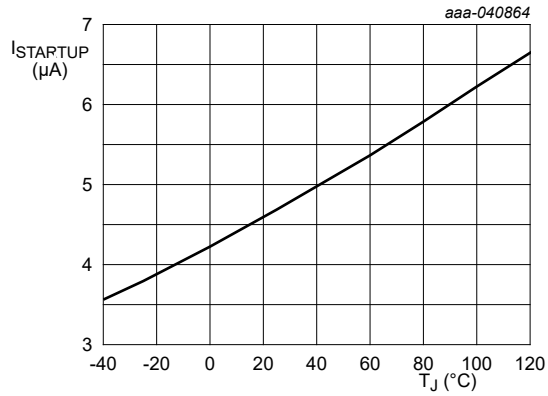
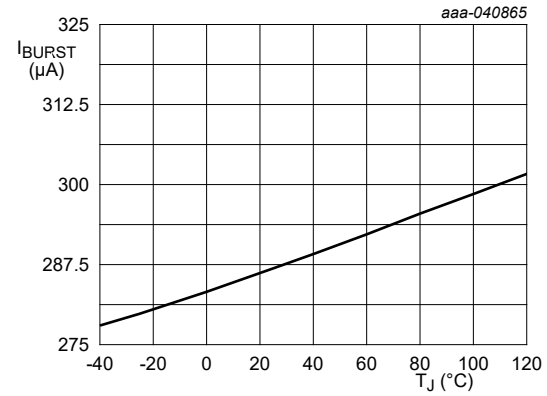


Fig. 5. V_{CC_OVP} vs. junction temperature



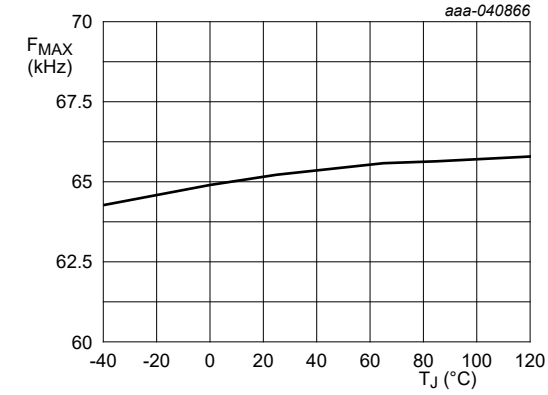
V_{CC} = 16 V

Fig. 6. $I_{STARTUP}$ vs. junction temperature



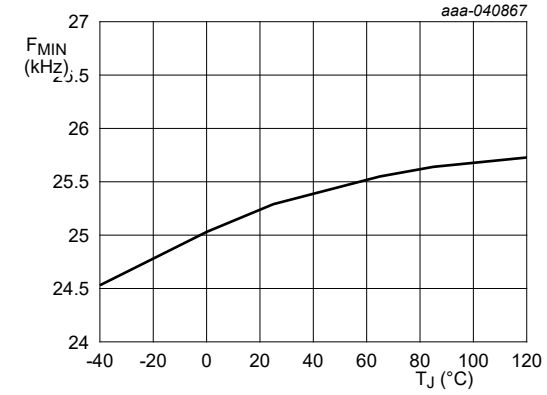
V_{CC} = 20 V

Fig. 7. I_{BURST} vs. junction temperature



V_{CC} = 20 V

Fig. 8. F_{MAX} vs. junction tempertaure



V_{CC} = 20 V

Fig. 9. F_{MIN} vs. junction tempertaure

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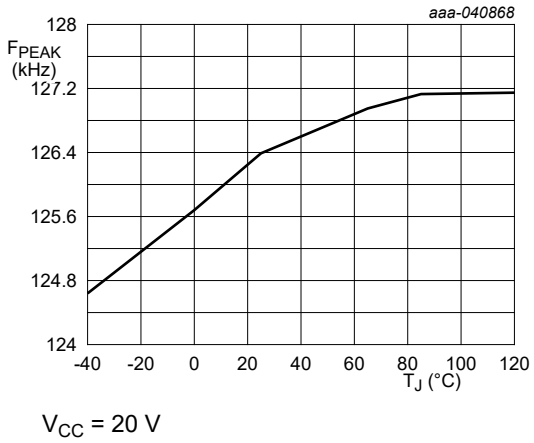

V_{CC} = 20 V

Fig. 10. F_{PEAK} vs. junction temperature

9. Detailed Description

9.1. Overview

The NEX80806 is an intelligent multi-mode PWM controller implemented with peak current mode control. In the low input line voltage and heavy load condition, the NEX80806 normally works in Continuous Conduction Mode (CCM) to reduce the conduction loss. As the input voltage increases, or the load current decreases, it enters Quasi-Resonant (QR) mode or Discontinuous Conduction Mode (DCM) with valley switching to reduce the switching loss. As the load current further decreases, it enters Pulse Frequency Modulation (PFM) mode with frequency foldback to maintain a high efficiency in the whole load range. To achieve an ultralow standby power, Burst Mode (BM) is implemented in very light load or no-load condition, while the minimum switching frequency is fixed at 25 kHz to avoid audible noise.

9.2. Functional block diagram

The NEX80806 function block diagram is shown in Fig. 11:

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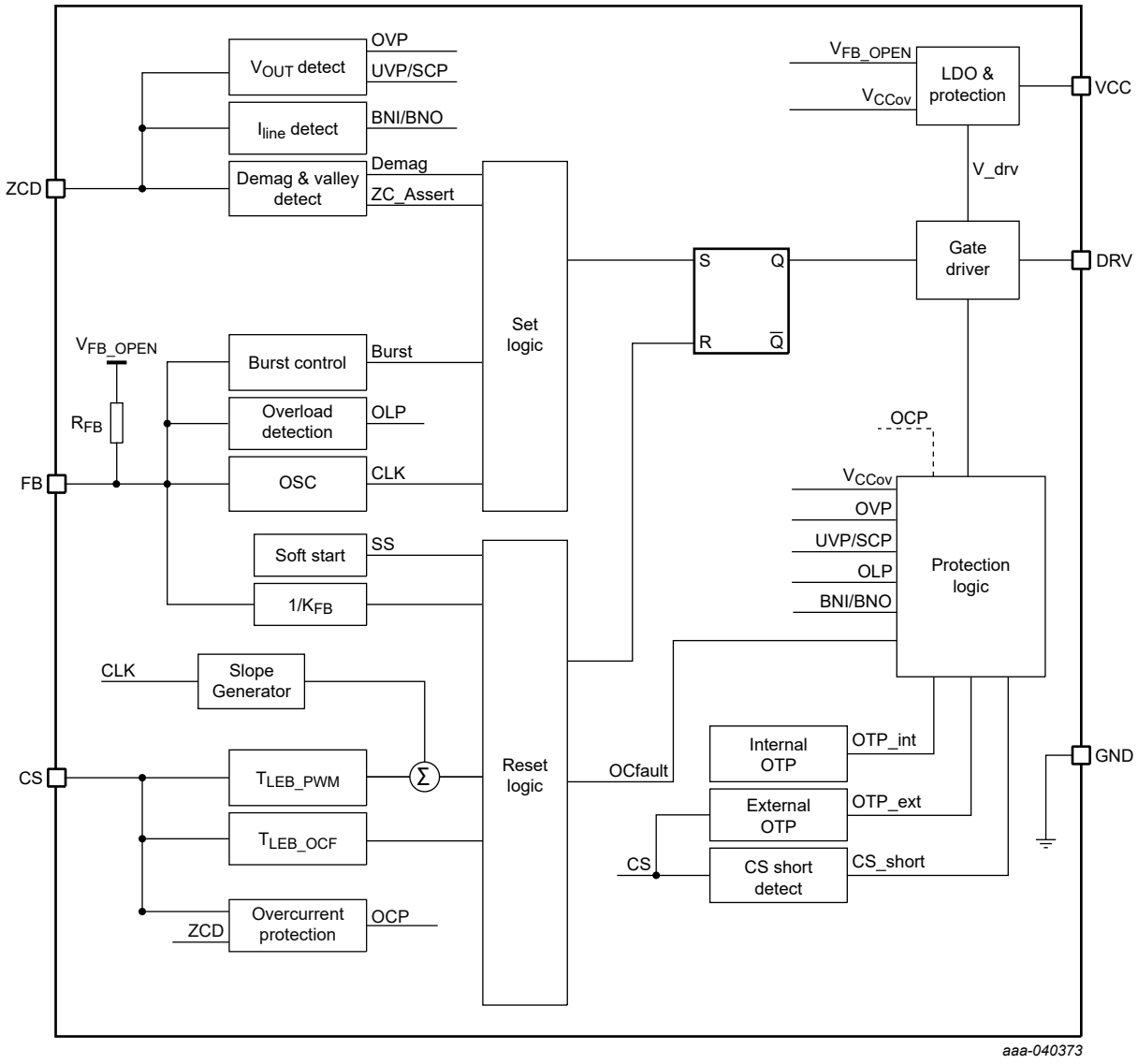

Fig. 11. Function block diagram

9.3. Feature description

9.3.1. Startup

The NEX80806 is enabled when V_{CC} voltage is higher than the turn-on threshold V_{CC_ON}, and disabled when it drops below the turn-off threshold V_{CC_OFF}. The voltage dips during startup; a hysteresis is built in to avoid shutdown during this process. As the AC input voltage is supplied, the voltage across the input bulk capacitor will charge the V_{CC} capacitor through the startup resistor R_{START} as shown in Fig. 12. Before being enabled, the VCC pin consumes only $I_{STARTUP}$ which is typically 5 µA. Thus, a relatively larger value can be chosen for R_{START} to reduce the power consumption. However, too large of a resistance for R_{START} will increase the startup time. Nexperia recommends using two 1.5 MΩ resistors with 1206 package in series for R_{START}.

Once V_{CC} voltage is higher than V_{CC_ON} threshold, the NEX80806 is enabled and the DRV pulse is generated to drive the external MOS. The current consumption at the VCC pin will increase to I_{NORMAL}, which is much higher than the current from startup resistor. Then the V_{CC} voltage decreases. It is important that the auxiliary winding voltage increases enough to take over and maintain the V_{CC} voltage in the normal range before it drops below V_{CC_OFF}. The capacitance of the V_{CC} capacitor should be carefully sized to meet this requirement. A 4.7 µF electrolytic capacitor is normally used here. The timing sequence of startup is shown in Fig. 13.

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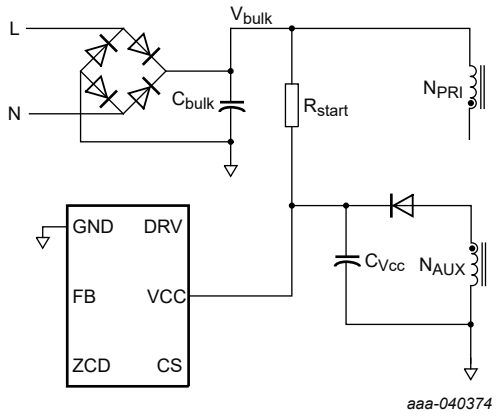

Fig. 12. Typical startup circuit

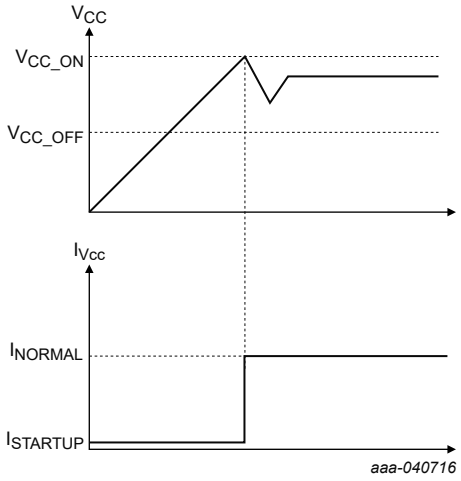

Fig. 13. Timing sequence of startup

9.3.2. Brown-in/brown-out

In addition to the detection of V_{CC} voltage, the input line voltage is also checked before the soft start is initiated. When the primary MOS is turned on, the induced auxiliary winding voltage is negative, generating a current flowing out from the ZCD pin. See Fig. 14 for reference.

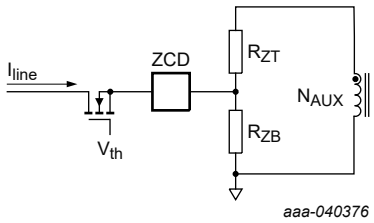

Fig. 14. Resistor divider at ZCD

Since the ZCD voltage is clamped at ~0 V by internal circuit, this current is proportional to input voltage and can be calculated as shown Equation 1:

$$I_{line} = \frac{V_{BULK} \times N_{AUX}}{N_{PRI} \times R_{ZT}} \quad (1)$$

where N_{PRI} and N_{AUX} are the number of turns of primary winding and auxiliary winding respectively, and R_{ZT} is the top side resistor of the divider from auxiliary winding to ZCD pin.

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Each time V_{CC} is higher than V_{CC_ON}, the NEX80806 will send out several narrow pulses to turn on the primary MOS, then detect I_{line}. If I_{line}>I_{BNI}, the brown-in threshold current, the NEX80806 will initiate soft start process. Otherwise it will restart.

During the normal working period, I_{line} is always checked when the primary MOS is turned on. If I_{line} below I_{BNO}(brown-out threshold current) for a continuous period larger than t_{D_BNO} (~50 ms), the NEX80806 will restart. The timing sequence of brown-out is shown in Fig. 15.

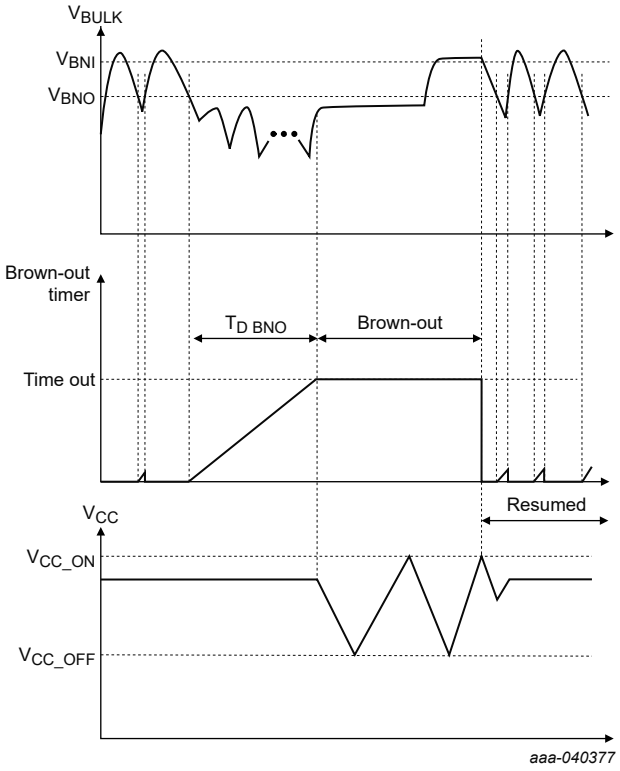

Fig. 15. Timing sequence of brown-out

9.3.3. V_{CC} holding mode

In very light load conditions, the NEX80806 may stay in the burst off-state for a long time when the output voltage is higher than the target. V_{CC} voltage may drop below V_{CC_OFF} since there is no driving pulse. This triggers the restart. To avoid this, the NEX80806 will send out the driving pulse once V_{CC} is below V_{CC_HOLD} , which is slightly higher than V_{CC_OFF}. The NEX80806 will stop the driving pulse when V_{CC} returns to V_{CC_HOLD} plus hysteresis. This is called V_{CC} Holding Mode.

The turn ratio of auxiliary winding and secondary winding should be properly selected to make sure the V_{CC} Holding Mode will not be triggered at the no-load condition, since V_{CC} Holding Mode will override the normal output voltage regulation.

9.3.4. Current sense and peak current control

To implement peak current mode control, R_S, the sense resistor, is connected between the source of primary MOS and GND to sense the primary current. The sense voltage across R_S is feedback to CS pin, compared with the peak-control voltage to decide duty cycle of primary MOS. The peak-control voltage is generated from FB voltage divided by K_{FB} (typically 5), where the FB voltage is commanded by the voltage control loop to regulate the output voltage, see Fig. 16 as reference. The maximum peak-control voltage is clamped at $V_{CS_PWM_MAX}$ (~400 mV) internally. Then the maximum transformer primary current can be obtained by Equation 2

$$I_{Peak_max} = \frac{V_{CS_PWM_MAX}}{R_S} \quad (2)$$

Due to the parasitic capacitance of primary MOS and transformer, a large voltage spike often appears on the CS pin at turn on moment. To prevent this spike from falsely triggering the current sense comparator, a leading-edge-blanking (LEB) time

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T_{LEB_PWM} (~320 ns) is included in the input of CS pin. In case this internal LEB time is not enough, an external R-C filter can be added between the sense resistor and CS pin.

For peak current mode control, when it works in CCM, there is subharmonic oscillation issue when duty cycle > 50%. The NEX80806 has internal slope compensation to address this problem.

To improve the reliability, the NEX80806 limits the maximum duty of primary MOS at D_{MAX} (~78%).

9.3.5. Soft start

Once V_{CC} is higher than V_{CC_ON} threshold, and the input voltage is higher than Brown-in threshold, soft start process is initiated. During this period, the CS peak voltage is limited by SS signal which ramp up from 0 mV to 400 mV within t_{SS} which is 4.3 ms typically. This means the primary peak current increases slowly in the soft start period.

Besides, a proprietary method is implemented to prevent device from working in CCM during soft start period. By these means, the output voltage can ramp up without overshoot, and the voltage/current stress of secondary rectifier is minimized.

9.3.6. Voltage control loop

The output voltage is sensed by a resistor divider and feedback to an error amplifier (usually TL431 is used). The output of error amplifier drives an opto-coupler to generate the command voltage at FB pin. The FB voltage, combined with the internal current loop, controls the output voltage. The typical circuit of voltage control loop is shown in Fig. 16

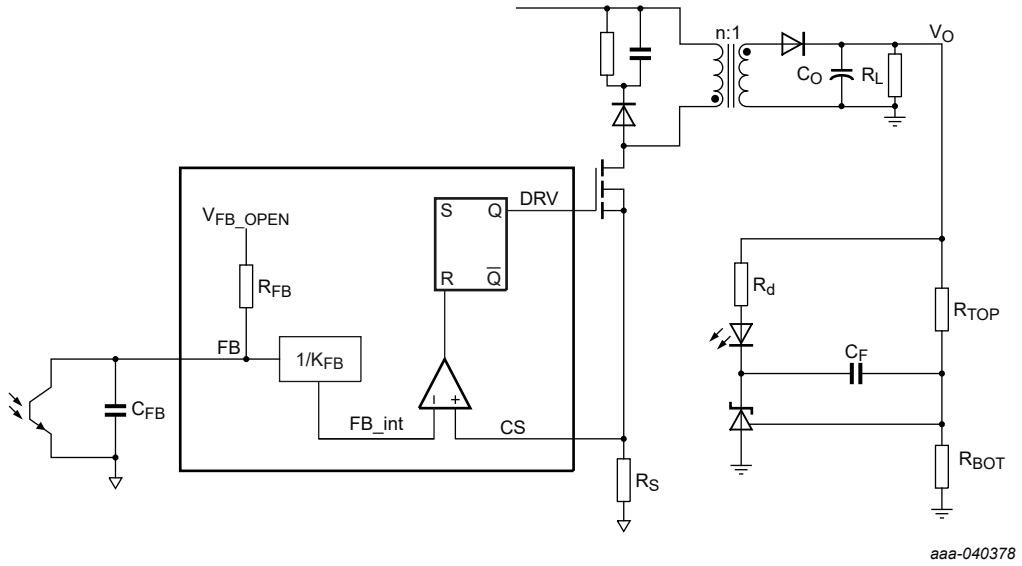

Fig. 16. Typical circuit of voltage control

9.3.7. Multimode operation

NEX80806 is a multi-mode PWM controller implemented with peak current mode control. As the load changes, it automatically switches mode between Continuous Conduction Mode (CCM), Quasi-Resonant (QR) mode, Discontinuous Conduction Mode (DCM) and Pulse Frequency Modulation (PFM) mode. To maintain a high efficiency in the whole load range, the turning-on of primary MOS is always gated by CLK signal, which is the clamping frequency commanded by FB voltage.

In heavy load and low line condition, FB is high, which means the primary peak current and clamp frequency is high. Since longer time is needed for demagnetization, normally the clock signal CLK comes earlier before demagnetization, the power MOS will be turned on by clock. At this moment, the magnetizing inductor current is not reset to zero yet, converter works in CCM.

As load decreases, or line voltage increases, FB voltage will decrease, which means the primary peak current and clamp frequency decreases. Demagnetization can be finished before the clock signal. In this condition, the power MOS will not be turned on until clock signal and the following valley moment detected, refer to Fig. 17, as well as the description in Section 9.3.10. Valley switching. In this way, power MOS turn on at the first valley after clock, the converter works in either

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QR/DCM (if clamp frequency is still at maximum frequency) or PFM (if clamp frequency already be lower than maximum value).

If the load continues to decrease, the clamp frequency will be further decreased as FB voltage decreases. The ringing amplitude at auxiliary winding may be damped too small for a valley moment to be detected after clock arrives. In this case, once T_{W_VALLEY} timer expires after CLK, the primary MOS will be forced on.

9.3.8. Burst mode control

As the load decreases, FB voltage will decrease to regulate the output voltage. As a result, the peak-control voltage (equal to the peak voltage of CS) decreases and is finally clamped at its minimum limit (typically ~90 mV). Meanwhile, the switching frequency also decreases and is clamped at F_{MIN} (typically 25 kHz) to avoid audible noise. If the load decreases further, FB voltage will drop below the $V_{FB_BURST_OFF}$ threshold (typically 0.3 V) and DRV pulse is disabled. In this burst-off period, V_{CC} current drops to I_{BURST} (typically 270 µA). At this moment, since no power is being delivered to the output anymore, the output voltage begins decrease. The voltage control loop will increase FB voltage gradually. Once FB voltage is higher than $V_{FB_BURST_ON}$ threshold (typically 0.35 V), the DRV pulse is resumed. Using this method of burst mode control improves the light load efficiency significantly.

9.3.9. ZCD voltage detection

During the flyback period, the information of output voltage can be derived by sampling ZCD voltage as shown in Fig. 17.

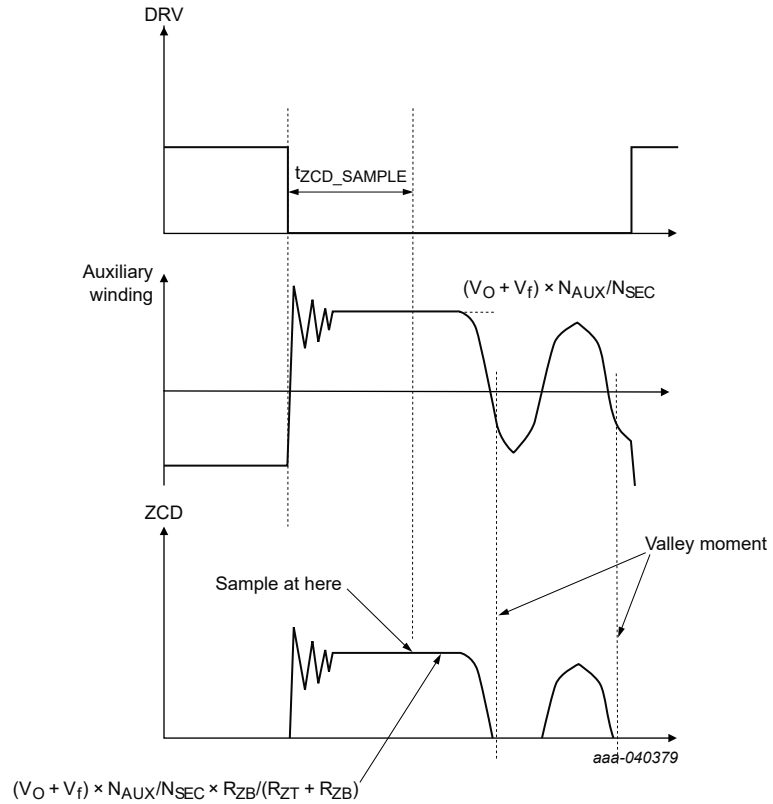

Fig. 17. ZCD voltage detection and valley detection

The output voltage OVP and UVP/SCP protection are implemented by comparing the sampled ZCD voltage with different threshold voltage.

The output voltage OVP protection is triggered if the sampled ZCD voltage is higher than OVP threshold for seven consecutive cycles.

The output voltage short-circuit protection (SCP) is triggered if the sampled ZCD voltage is lower than SCP threshold V_{ZCD_SCP} (1.2 V typically) for seven consecutive cycles.

Since the output voltage need time to setup, the UVP/SCP protection is disabled for a t_{BLK_UVP} blanking time during soft start.

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Due to the leakage inductance of transformer, there is large ringing waveform at ZCD pin at the beginning of flyback period. To avoid sampling at this ringing moment, a blanking time is added after the going-low of DRV signal. ZCD sampling is not allowed until this blanking window expires.

9.3.10. Valley switching

During QR/DCM/PFM mode, once the magnetizing current decreases to zero, the primary inductor begins oscillation with the parasitic capacitor of primary MOS. It's desired to turn on primary MOS at the valley moment of oscillation to minimize the switching loss. Referring to Fig. 17, when the auxiliary winding voltage becomes negative, ZCD pin is clamped at ~0 V internally, the current flowing out of ZCD pin is detected. Once the current is larger than I_{ZCD_VALLEY} (~9 μA), that moment is identified as a valley moment. There may be several valley moments identified before CLK signal arrives. The valley moment just behind CLK is chosen as the moment to turn on the primary MOS.

9.3.11. Oscillator frequency

As FB voltage decreases, the clamp frequency CLK will decrease from the maximum switching frequency F_{MAX} to the minimum limit F_{MIN} (typically 25 kHz , to avoid audible noise), to optimize the efficiency for different load condition.

To optimize the EMI performance, spread-spectrum function is implemented.

9.3.12. Peak load mode

Some applications require a much higher output current, normally double the full load current, in a short period (less than 200 ms normally). The output voltage must be basically stable during this short period (output voltage is allowed to drop ~10%).

For NEX80806, the primary peak current reaches its maximum limit when the voltage on FB approaches ~2 V. The switching frequency is also at maximum frequency F_{MAX} (~65 kHz) at this moment. To further improve the capability of output power, NEX80806 implemented peak load mode by increasing frequency gradually from F_{MAX} to F_{Peak} (~130 kHz) as FB voltage approaches 3.2 V.

9.3.13. Driver

The typical high level of DRV pin is clamped by an internal voltage clamp which clamps the voltage at 11.5 V under normal conditions. For a normal 12 V V_{CC} supply, the DRV amplitude is guaranteed to be higher than 8 V. This gives enough voltage to fully turn on the high-voltage MOSFETs, while providing an adequate margin to avoid overvoltage damage of the gate, since most high-voltage MOSFETs have a maximum gate voltage rating of 20 V.

9.3.14. Restart

When restart process is triggered, the DRV pulse is stopped at first, the V_{CC} voltage declines since there is no supply from auxiliary winding. Once V_{CC} voltage drops below V_{CC_OFF} threshold, the device is disabled and the V_{CC} current consumption drops to $I_{STARTUP}$ which is 5 μA typical, then V_{CC} capacitor will be charged up by startup resistor. When V_{CC} voltage rises above V_{CC_ON}, a soft start process is initiated if the line voltage meets the brown-in requirement.

9.3.15. Overload protection (OLP)

If the load current is higher than the maximum allowed output current limit, the output voltage will drop, FB voltage will increase. If FB voltage is higher than V_{FB_OLP} (3.5 V typical) for a period t_{D_OLP}, overload protection is triggered, the device will restart.

9.3.16. Over current protection (OCP)

To meet the Limited Power Source (LPS) requirements, the maximum output current of power supply should be less than 8A, and the output power should not exceed 100W at any condition. However, with a fixed primary peak current limit, the output current and output power will increase as input line voltage increase, LPS is highly possible to be violated.

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To better meet the LPS requirements, NEX80806 adopts the OCP method. By detecting the valley and peak primary current, as well as the demagnetization duty, the NEX80806 calculates the output current of the flyback circuit. If the calculated value is higher than the target current limit for a preset period, the OCP is triggered, and the device will restart.

9.3.17. Secondary rectifier short-circuit protection (SRSP)

In case the secondary rectifier is short-circuited, the primary MOS current increases very fast at the turn on moment, an immediate protection is needed here. A shorter blanking time t_{LEB_OCF} (~90 ns) is implemented to address this problem. Each time primary MOS is turned on, once the blanking time t_{LEB_OCF} expires, the primary current is sampled and feedback to CS pin. If it's higher than SR short-circuit fault protection threshold V_{CS_OCF} (~650 mV), the primary MOS is turned off immediately. If this event happens in consecutive 3 cycles, the device will restart.

9.3.18. V_{CC} over voltage protection (V_{CC} OVP)

Once V_{CC} voltage is higher than threshold V_{CC_OVP} (typically 28 V), V_{CC} OVP is triggered, and the device restarts. In some abnormal conditions, for example, when the startup resistance is too low, V_{CC} voltage is pulled up even though the device is in restart condition. If V_{CC} voltage is pulled higher than V_{CC_DIS} threshold (typically 33 V), a sink current $I_{DISCHARGE}$ (typically 5mA) will discharge V_{CC} voltage until it is below 28 V. This prevents the VCC pin from being damaged by overvoltage in abnormal conditions.

9.3.19. Over temperature protection (OTP)

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. Once the T_J exceeds the thermal shutdown threshold T_{SD} (typically 155 °C), the device shuts down and DRV pulse stops. The device temperature decreases; when T_J is below 125 °C, the device will restart.

Besides the internal OTP, the NEX8080x also has an external OTP function. By adding an NTC resistor at the key component of the power supply, that component can be protected from over temperature damage. This method is shown in Fig. 18.

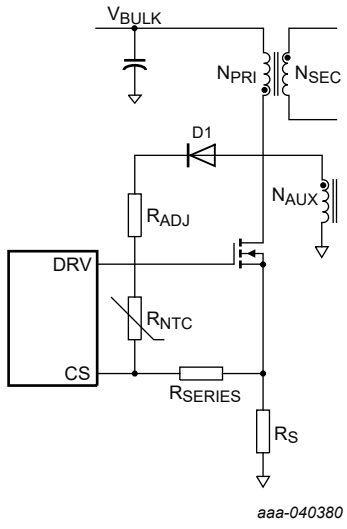

Fig. 18. Typical application circuit of external OTP

When the primary MOS is turned off, the auxiliary winding voltage is feedback to the CS pin by resistor divider. Under normal conditions, the NTC resistor R_{NTC} has a large resistance. This results in a very low voltage at the CS pin. For abnormal conditions, the NTC resistor temperature increases much higher due to the key component under protection, so the resistance of R_{NTC} decreases significantly, which leads to an increase in the divided voltage at the CS pin. If the voltage on the CS pin is higher than threshold V_{CS_OTP} for t_{D_OTP} (typically 1.5 ms), the external OTP is triggered, the device stops DRV pulse and restarts.

The resistance of R_{NTC} that triggering external OTP can be calculated in Equation 3:

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$$R_{NTC(OTP)} = R_{series} \times \left(\frac{\left(N_{AUX} / N_{SEC} \right) \times V_O - V_d}{V_{CS_OTP}} - 1 \right) - R_{ADJ} \quad (3)$$

where, N_{AUX} and N_{SEC} are the turn numbers of auxiliary and secondary windings respectively. Vd is the forward voltage of D1. The resistor R_{ADJ} is used to fine tune the external OTP temperature at target threshold.

9.3.20. CS pin short protection

In case the CS pin is shorted to GND, or the sense resistor R_S is shorted, the primary current will lose control. This is dangerous and must be prevented. Each time the primary MOS is turned on, a blanking timer $t_{BLK_CS_SHORT}$ starts. When it expires, if the MOS is not turned off yet, the CS pin voltage will be compared with V_{CS_SHORT} threshold (typcically 40 mV). If the CS pin voltage lower than threshold, this indicates a CS short failure, and the primary MOS will be turned off immediately. If this event happens for three consecutive cycles, the NEX80806 will restart.

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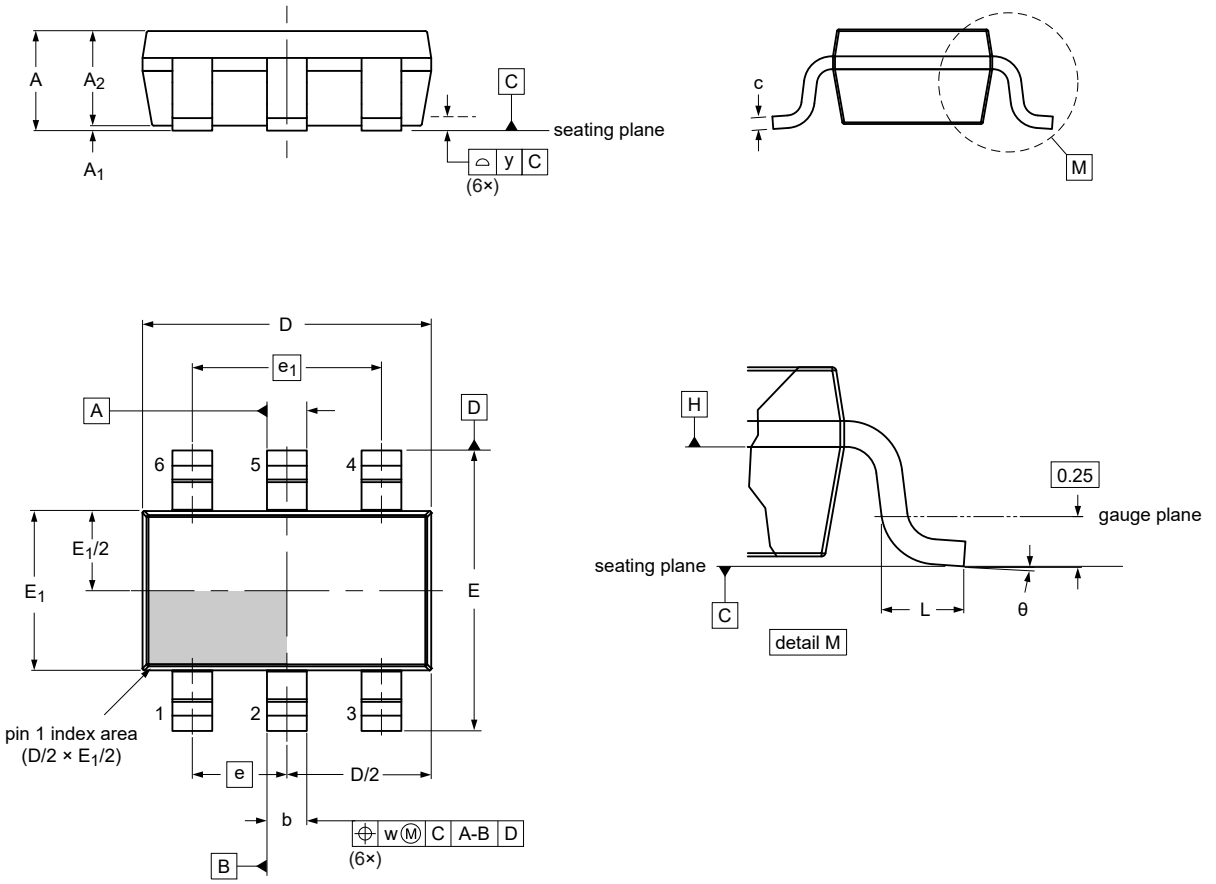
10. Package outline

Plastic, surface-mounted package (TSOT23-6); 6 leads **SOT8061-1**



Dimensions (mm are the original dimensions)

Unit[1]		A	A_1	A_2	b	c	D	E	E_1	e	e_1	L	y	w	θ
mm	max	1.10	0.10	1.00	0.50	0.20	3.05	3.00	1.75	0.95 BSC	1.90 BSC	0.60	0.10	0.20	8°
	nom						2.90	2.80	1.60						
	min		0.00	0.70	0.30	0.08	2.75	2.60	1.45			0.30			0°

Note
Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.25 mm per end.
Dimension E_1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0. 25 mm per side.
D and E_1 dimensions are determined at datum H.

sot8061-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8061-1		MO-193				~~24-09-04~~ 24-09-16

Fig. 19. Package outline SOT8061-1 (TSOT23-6)

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11. Abbreviations

Table 9. Abbreviations

Acronym	Description
AC	Alternating Current
BM	Burst Mode
CCM	Continuous Conduction Mode
CDM	Charged Device Model
DC	Direct Current
DCM	Discontinuous Conduction Mode
DUT	Device Under Test
EMI	ElectroMagnetic Interference
ESD	ElectroStatic Discharge
HBM	Human Body Model
HV	High Voltage
IC	Integrated Circuit
JEDEC	Joint Electron Device Engineering Council
LPS	Limited Power Source
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
OCP	OverCurrent Protection
OLP	OverLoad Protection
OPP	OverPower Protection
OTP	OverTemperature Protection
OVP	OverVoltage Protection
PFM	Pulse Frequency Modulation
QR	Quasi-Resonant
SRSP	Synchronous Rectifier Short Protection
USB	Universal Serial Bus
UVLO	Under-Voltage LockOut

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12. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NEX80806 v.2.1	20260122	Product data sheet	-	NEX80806 v.2
Modification	• Fig. 1 updated.			
NEX80806 v.2	20241028	Product data sheet	-	NEX80806 v.1
Modification	• Table 4: errata, max V_{CC} value changed to 40 V.			
NEX80806 v.1	20240930	Product data sheet	-	-

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Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 22 January 2026

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