



# NEH7100

Inductorless energy harvesting PMIC with battery protection, LDO, USB charging and I<sup>2</sup>C

Rev. 2 — 5 September 2025

Product data sheet

## 1. General description

The NEH7100 is a high-performance power management IC (PMIC) for energy harvesting solutions in low-power applications. It has a rich set of auxiliary features, such as storage element protection, USB charging and LDO / load switch.

The NEH7100 is optimized to harvest energy from light sources (from a wide range of indoor and outdoor PV cells). Other energy sources can also be used, such as kinetic (movement, vibrations), thermal variation and electromagnetic, but might need external auxiliary components. The NEH7100 gathers energy from a suitable harvester to charge a storage element, such as a rechargeable battery or a supercapacitor.

Nexperia's advanced maximum power point tracking (MPPT) uses an embedded hill-climbing algorithm to deliver maximum power to the storage element. The MPPT is compatible with any suitable harvester, and optimizes efficiency as frequent as every 0.5 seconds for excellent performance in rapidly changing harvesting conditions.

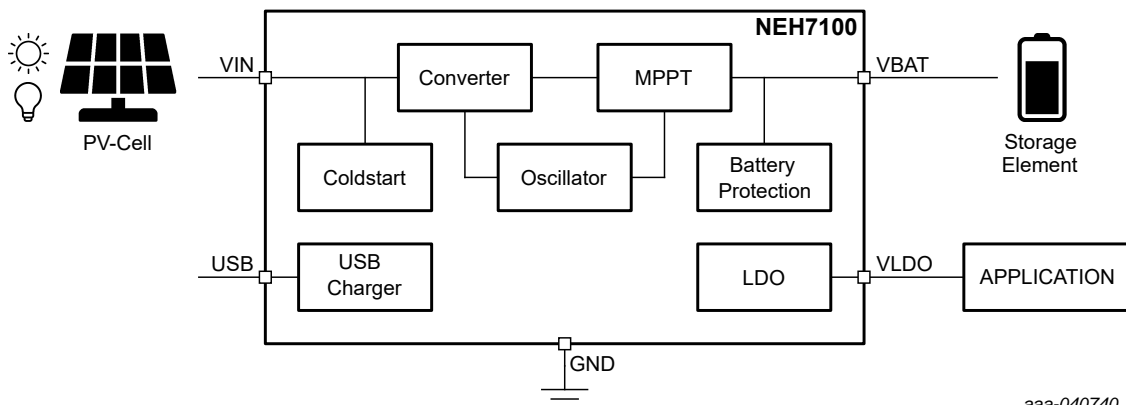
The NEH7100 is available in 28-lead, 4 mm x 4 mm HVQFN28 package.

## 2. Features and benefits

- Chip input power range: 15  $\mu$ W to 100 mW
- Efficiency up to 95%
- Ultra-fast MPPT interval
- Battery protection features:
  - Over-voltage protection (OVP)
  - Low-voltage detection (LVD)
  - Over-current protection (OCP)
- USB charging up to 200 mA
- LDO with configurable output voltage
- Configurable via hard-coding or I<sup>2</sup>C
- Coldstart, supporting "battery-less" design
- Small BOM with no inductor required
- Suitable for batteries, supercapacitors and hybrid capacitors

## 3. Applications

- Smart remote controls: TV, gaming, AV control, key-fob
- Wireless PC devices: keyboard, mouse, headphones
- Industrial sensors: electronic shelf labels, asset trackers and beacons
- Tire pressure sensors
- Wearable devices: watch, body band and health devices



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Fig. 1. NEH7100 typical solar energy harvesting system

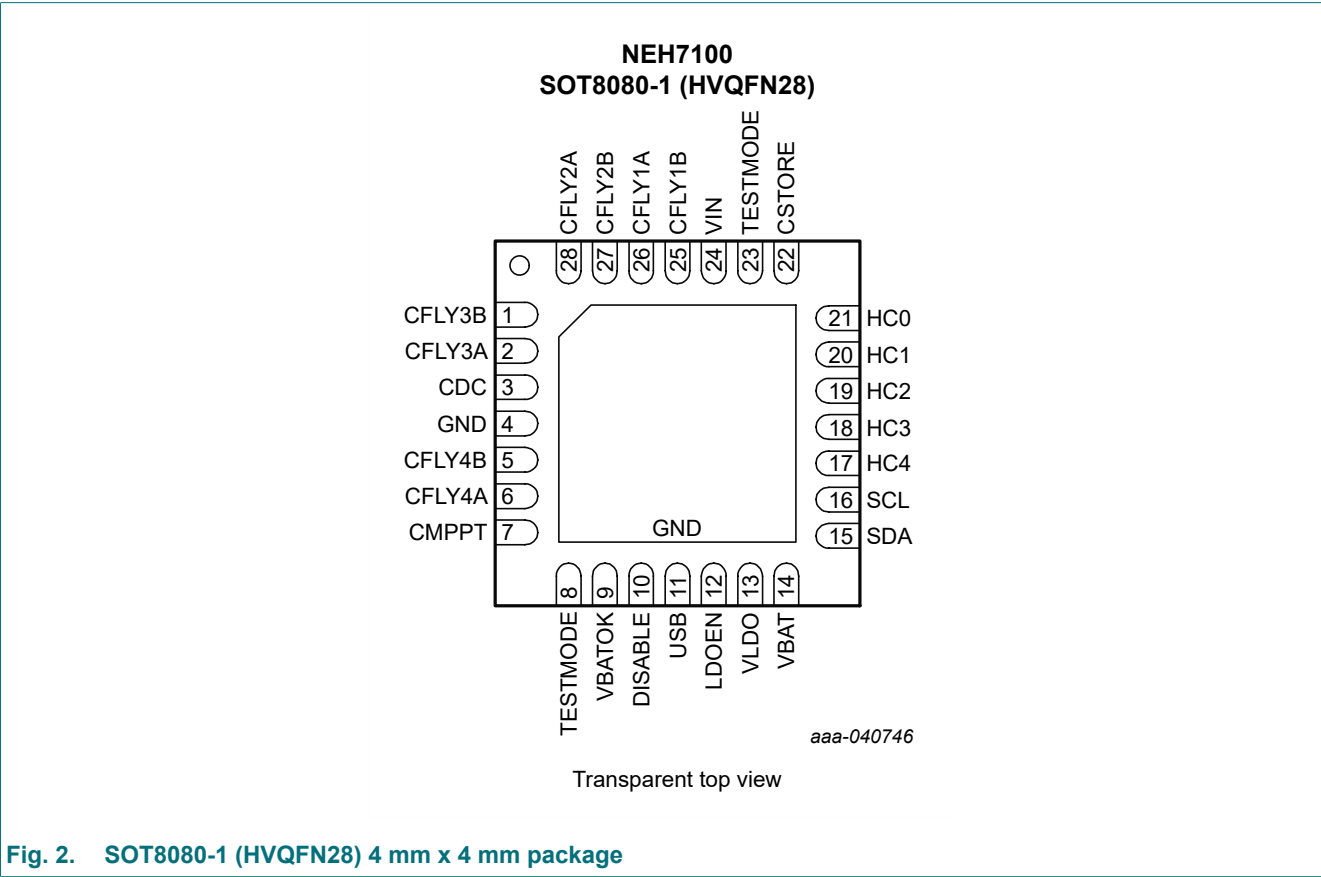
4. Ordering information

Table 1. Ordering information

| Type number               | Package           |         |  |                           |
|---------------------------|-------------------|---------|--|---------------------------|
|                           | Temperature range | Name    | Description  | Version                   |
| <a href="#">NEH7100BU</a> | -40 °C to 85 °C   | HVQFN28 | plastic, leadless thermal enhanced very thin quad flat package; 28 terminals; 0.4 mm pitch; 4 mm x 4 mm x 0.85 mm body | <a href="#">SOT8080-1</a> |

5. Pinning information

5.1. Pinning configuration



5.2. Pinning description

Table 2. Pinning description

| Pin | Symbol   | Description   |
|-----|----------|---|
| 1   | CFLY3B   | flying-capacitor terminal B, 3rd stage  |
| 2   | CFLY3A   | flying-capacitor terminal A, 3rd stage  |
| 3   | CDC      | boost converter filter capacitor  |
| 4   | GND      | ground  |
| 5   | CFLY4B   | flying-capacitor terminal B, 4th stage  |
| 6   | CFLY4A   | flying-capacitor terminal A, 4th stage  |
| 7   | CMPPT    | filter capacitor for MPPT   |
| 8   | TESTMODE | reserved; should be left floating   |
| 9   | VBATOK   | indicates if battery voltage is above configured LVD level  |
| 10  | DISABLE  | active high. Disable mode sets the device in low-power consumption. Connect to GND to enable, connect to V <sub>BAT</sub> to disable. |
| 11  | USB      | USB 5V input for charging storage element connected to V <sub>BAT</sub> .   |
| 12  | LDOEN    | LDO enable, active high. Connect to V <sub>BAT</sub> level to enable. Connect to GND to disable                                       |
| 13  | VLDO     | LDO output. LDO input is internally connected to VBAT. Connect to application load.   |
| 14  | VBAT     | output of the energy harvester and power supply for PMIC. Connect storage element to this pin.  |
| 15  | SDA      | I <sup>2</sup> C serial data input / output   |
| 16  | SCL      | I <sup>2</sup> C serial clock input   |
| 17  | HC4      | hard-code bit [4]. Connect to GND for a logic low, to CSTORE for a logic high   |
| 18  | HC3      | hard-code bit [3]. Connect to GND for a logic low, to CSTORE for a logic high   |
| 19  | HC2      | hard-code bit [2]. Connect to GND for a logic low, to CSTORE for a logic high   |
| 20  | HC1      | hard-code bit [1]. Connect to GND for a logic low, to CSTORE for a logic high   |
| 21  | HC0      | hard-code bit [0]. Connect to GND for a logic low, to CSTORE for a logic high   |
| 22  | CSTORE   | internal supply pin   |
| 23  | TESTMODE | reserved; should be left either floating or connected to GND  |
| 24  | VIN      | input for connecting a harvester  |
| 25  | CFLY1B   | flying-capacitor terminal B, 1st stage  |
| 26  | CFLY1A   | flying-capacitor terminal A, 1st stage  |
| 27  | CFLY2B   | flying-capacitor terminal B, 2nd stage  |
| 28  | CFLY2A   | flying-capacitor terminal A, 2nd stage  |
| PAD | GND      | ground pad, should be connected to ground plane with vias   |

6. Specifications

6.1. Absolute maximum ratings

Table 3. Absolute maximum ratings

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol              | Parameter  | Conditions   | Min  | Max  | Unit |
|---------------------|--|--|------|------|------|
| V <sub>PC</sub>     | power converter pins:<br>CFLY1x, CFLY2x                        |  | -0.3 | 2.0  | V    |
|                     | power converter pins:<br>CFLY3x, CFLY4x, CDC,<br>CMPPT, CSTORE |  | -0.3 | 5.5  | V    |
| V <sub>CONFIG</sub> | configuration pins:<br>DISABLE, LDOEN, SDA,<br>SCL, HCx        |  | -0.3 | 5.5  | V    |
| V <sub>IN</sub>     | input pin: VIN   | using bench power supply with low series<br>resistance | -0.3 | 2.0  | V    |
|                     |  | using PV-cell or current-limited source                | -0.3 | 5.5  | V    |
| V <sub>POWER</sub>  | power pins: VBAT, USB  |  | -0.3 | 5.5  | V    |
| I <sub>IN</sub>     | input current (VIN pin)  |  | -    | 140  | mA   |
| T <sub>j</sub>      | junction temperature   |  | -50  | +125 | °C   |
| T <sub>stg</sub>    | storage temperature  |  | -65  | +150 | °C   |

6.2. ESD ratings

Table 4. ESD ratings

| Symbol           | Parameter                          | Conditions                  | Value  | Unit |
|------------------|------------------------------------|-----------------------------|--------|------|
| V <sub>ESD</sub> | electrostatic discharge<br>voltage | HBM: ANSI/ESDA/JEDEC JS-001 | ± 2000 | V    |
|                  |                                    | CDM: ANSI/ESDA/JEDEC JS-002 | ± 500  | V    |

6.3. Recommended operating conditions

Table 5. Recommended operating conditions

| Symbol           | Parameter           | Conditions | Min | Typ | Max | Unit |
|------------------|---------------------|------------|-----|-----|-----|------|
| V <sub>BAT</sub> | battery voltage     |            | 0   | -   | 4.5 | V    |
| T <sub>amb</sub> | ambient temperature |            | -40 | -   | +85 | °C   |

6.4. Thermal information

Table 6. Thermal characteristics

| Symbol             | Parameter   | SOT8080-1 | Unit |
|--------------------|---|-----------|------|
| R <sub>θ(ja)</sub> | junction-to-ambient thermal resistance                    | 57.8      | °C/W |
| R <sub>θ(jc)</sub> | junction-to-case (top) thermal resistance                 | 73.4      | °C/W |
| Ψ <sub>(jt)</sub>  | junction-to-case (top) thermal characterization parameter | 25.1      | °C/W |

## 6.5. Electrical characteristics

**Table 7. Electrical characteristics**

$V_{BAT} = 3.7\text{ V}$ . Typical values specified at  $T_{amb} = 25\text{ °C}$ , Min and Max values specified at  $T_{amb} = -40\text{ °C}$  to  $85\text{ °C}$ . Voltages are referenced to GND (ground = 0 V).  $V_{MPP}$  represents the maximum power point voltage at  $V_{IN}$ .

| Symbol                       | Parameter                           | Conditions  | Min | Typ  | Max | Unit |
|------------------------------|-------------------------------------|---|-----|------|-----|------|
| <b>Supplies and start-up</b> |                                     |   |     |      |     |      |
| $V_{BAT}$                    | battery voltage                     | To start device with input power on $V_{IN}$  | 0   |      | 4.5 | V    |
|                              |                                     | Minimum voltage to start device without input power on $V_{IN}$                             | -   | 2.9  | 3.6 | V    |
|                              |                                     | Minimum voltage required to keep device running after start and without power on $V_{IN}$   | -   | 2    | -   | V    |
| $I_{DISABLE}$                | disable mode current                | $V_{DISABLE} = V_{BAT}$   | -   | 13   | 150 | nA   |
| $I_Q$                        | quiescent current (LDO disabled)    | no input power, $V_{IN}$ is floating; LDO disabled  | -   | 1.5  | 5   | μA   |
| $I_{Q(LDO)}$                 | quiescent current (LDO enabled)     | no input power, $V_{IN}$ is floating; LDO enabled   | -   | 2.1  | 6.5 | μA   |
| $t_{start}$                  | start-up time                       | time from applying $V_{BAT}$ to rising edge of $VBATOK$ ; No input power on $V_{IN}$        | -   | 720  | -   | ms   |
| <b>Power converter</b>       |                                     |   |     |      |     |      |
| $\eta$                       | nominal efficiency                  | $V_{MPP} = 2\text{ V}$  | -   | 94   | -   | %    |
|                              |                                     | $V_{MPP} = 1\text{ V}$  | -   | 90   | -   | %    |
|                              |                                     | $V_{MPP} = 0.5\text{ V}$  | -   | 85   | -   | %    |
|                              |                                     | $V_{MPP} = 0.25\text{ V}$   | -   | 75   | -   | %    |
| $P_{IN(low)}$                | input power range, low end          | efficiency = 70%; $V_{MPP} = 2\text{ V}$  | -   | 65   | -   | μW   |
|                              |                                     | efficiency = 60%; $V_{MPP} = 1\text{ V}$  | -   | 55   | -   | μW   |
|                              |                                     | efficiency = 50%; $V_{MPP} = 0.5\text{ V}$  | -   | 45   | -   | μW   |
|                              |                                     | efficiency = 40%; $V_{MPP} = 0.25\text{ V}$   | -   | 53   | -   | μW   |
| $P_{IN(high)}$               | input power range, high end         | efficiency = 70%; $V_{MPP} = 2\text{ V}$  | -   | 69   | -   | mW   |
|                              |                                     | efficiency = 60%; $V_{MPP} = 1\text{ V}$  | -   | 52   | -   | mW   |
|                              |                                     | efficiency = 50%; $V_{MPP} = 0.5\text{ V}$  | -   | 23   | -   | mW   |
|                              |                                     | efficiency = 40%; $V_{MPP} = 0.25\text{ V}$   | -   | 10   | -   | mW   |
| $V_{IN(min)}$                | minimum input voltage               | Main converter active, cold start inactive; efficiency $\geq 40\%$ . $I_{IN} = 1\text{ mA}$ | -   | 0.23 | -   | V    |
| $f_{CONV(low)}$              | frequency at low-end power          |   | -   | 30   | -   | kHz  |
| $f_{CONV(high)}$             | frequency at high-end power         |   | -   | 1.1  | -   | MHz  |
| $t_{MPPT}$                   | MPPT interval                       | Set values (Table 8)  | 0.5 |      | 64  | sec  |
| $t_{MPPT(acc)}$              | MPPT interval inaccuracy            |   | -   | 10   | -   | %    |
| <b>Cold start</b>            |                                     |   |     |      |     |      |
| $V_{IN(CS)}$                 | minimum $V_{IN}$ cold start voltage | $P_{IN} > 12\text{ μW}$   | -   | 270  | -   | mV   |
| $P_{IN\_CS(min)}$            | minimum cold start input power      | $V_{IN} = 270\text{ mV}$  | -   | 12   | -   | μW   |

Inductorless energy harvesting PMIC with battery protection, LDO, USB charging and I<sup>2</sup>C

| Symbol                           | Parameter  | Conditions  | Min | Typ           | Max | Unit |
|----------------------------------|--|---|-----|---------------|-----|------|
| <b>Battery protection</b>        |  |   |     |               |     |      |
| V <sub>BAT_OVP</sub>             | over-voltage protection (OVP)  | Set value (see <a href="#">Table 17</a> )   | 2.7 | -             | 4.5 | V    |
| V <sub>BAT_LVD</sub>             | low-voltage detection (LVD)  | Set value (see <a href="#">Table 18</a> )   | 2.2 | -             | 3.7 | V    |
| V <sub>BAT(acc)</sub>            | over-voltage protection (OVP) and low-voltage detection (LVD) threshold inaccuracy |   | -   | -1            | -   | %    |
| V <sub>LVD(hys)</sub>            | low-voltage detection (LVD) hysteresis   | Voltage difference between LVD falling and rising threshold   | -   | 150           | -   | mV   |
| <b>USB features</b>              |  |   |     |               |     |      |
| USB_OVP                          | USB over-voltage   | Set value (see <a href="#">Table 17</a> )   | 2.7 | -             | 4.5 | V    |
| USB_OCP                          | USB over-current   | Set value (see <a href="#">Table 13</a> )   | 0.5 | -             | 200 | mA   |
| I <sub>BAT</sub>                 | storage element charging current via USB   |   | -   | 0.8 × setting | -   | mA   |
| V <sub>BAT(acc)</sub>            | storage element over-voltage inaccuracy via USB                                    | 5 V on USB pin  | -   | -1            | -   | %    |
| I <sub>BAT(acc)</sub>            | storage element charging current inaccuracy  | 5 V on USB pin; relative to 0.8 × setting   | -   | -6            | -   | %    |
| <b>LDO features</b>              |  |   |     |               |     |      |
| V <sub>LDO</sub>                 | LDO voltage  | Set value (see <a href="#">Table 14</a> )   | 1.2 | -             | 3.6 | V    |
| V <sub>LDO(acc)</sub>            | LDO voltage inaccuracy   | I <sub>LDO</sub> = 1 mA   | -   | -1            | -   | %    |
| I <sub>LDO(max)</sub>            | maximum LDO output current   | V <sub>BAT</sub> = VLDO_nom + 0.5 V;<br>V <sub>BAT(min)</sub> = 2.5 V   | -   | 200           | -   | mA   |
| V <sub>LDO(drop)</sub>           | LDO dropout voltage  | I <sub>LDO</sub> = 200mA  | -   | 130           | -   | mV   |
| t <sub>LDO_on</sub>              | LDO turn-on time   | from LDO_EN rising edge until V <sub>LDO</sub> = 95%; I <sub>LDO</sub> = 200 mA; V <sub>LDO</sub> = 3.6 V; V <sub>BAT</sub> = 4 V                                   | -   | 0.5           | -   | s    |
| ΔV <sub>LDO(line)</sub>          | LDO line regulation  | V <sub>LDO</sub> inaccuracy over V <sub>BAT</sub> range. I <sub>LDO</sub> = 1 mA; 2.5 V < V <sub>BAT</sub> < 4.5 V and V <sub>BAT</sub> > V <sub>LDO</sub> + 0.5 V  | -   | 0.2           | -   | %    |
| ΔI <sub>LDO(load)</sub>          | LDO load regulation  | V <sub>LDO</sub> inaccuracy over I <sub>LDO</sub> range. I <sub>LDO</sub> < 200 mA; V <sub>BAT</sub> = V <sub>LDO(nom)</sub> + 0.5 V; V <sub>BAT(min)</sub> = 2.5 V | -   | -1.5          | -   | %    |
| <b>I<sup>2</sup>C parameters</b> |  |   |     |               |     |      |
| I <sup>2</sup> C_addr            | I <sup>2</sup> C address   |   | 3C  |               |     | hex  |
| V <sub>DD(I<sup>2</sup>C)</sub>  | I <sup>2</sup> C bus voltage   |   | 1.2 | -             | 4.5 | V    |
| V <sub>IL</sub>                  | SDA/SCL input logic low level  |   | -   | -             | 0.5 | V    |
| V <sub>IH</sub>                  | SDA/SCL input logic high level   |   | 1.0 | -             | -   | V    |
| V <sub>OL</sub>                  | SDA output logic low level   | I <sub>SDA</sub> = 3 mA   | -   | -             | 0.4 | V    |
| f <sub>SCL</sub>                 | SCL clock frequency  |   | -   | -             | 100 | kHz  |
| t <sub>LOW</sub>                 | low period of SCL clock  |   | 4.7 | -             | -   | μs   |
| t <sub>HIGH</sub>                | high period of SCL clock   |   | 4.0 | -             | -   | μs   |
| t <sub>HD</sub>                  | data hold time   |   | 300 | -             | -   | ns   |
| t <sub>SU</sub>                  | data set-up time   |   | 250 | -             | -   | ns   |

Inductorless energy harvesting PMIC with battery protection, LDO, USB charging and I<sup>2</sup>C

| Symbol                      | Parameter                                     | Conditions                 | Min                    | Typ | Max | Unit |
|-----------------------------|---|----------------------------|------------------------|-----|-----|------|
| Logic levels                |   |                            |                        |     |     |      |
| V <sub>OL_BATOK(low)</sub>  | VBATOK output logic low level                 | I <sub>sink</sub> = 1 mA   | -                      | -   | 0.2 | V    |
| V <sub>OH_BATOK(high)</sub> | VBATOK output logic high level                | I <sub>source</sub> = 1 mA | V <sub>BAT</sub> - 0.4 | -   | -   | V    |
| V <sub>IL_LDOEN(low)</sub>  | LDO enable pin (LDOEN) input logic low level  |                            | -                      | -   | 0.5 | V    |
| V <sub>IH_LDOEN(high)</sub> | LDO enable pin (LDOEN) input logic high level |                            | 1                      | -   | -   | V    |
| V <sub>IL_DIS(low)</sub>    | DISABLE input logic low level                 |                            | -                      | -   | 0.4 | V    |
| V <sub>IH_DIS(high)</sub>   | DISABLE input logic high level                |                            | V <sub>BAT</sub> - 0.4 | -   | -   | V    |

6.6. Typical characteristics

At recommended operating conditions; V<sub>BAT</sub> = 3.7 V; typical values are at 25°C (unless otherwise noted). V<sub>MPP</sub> represents the maximum power point voltage at V<sub>IN</sub>.

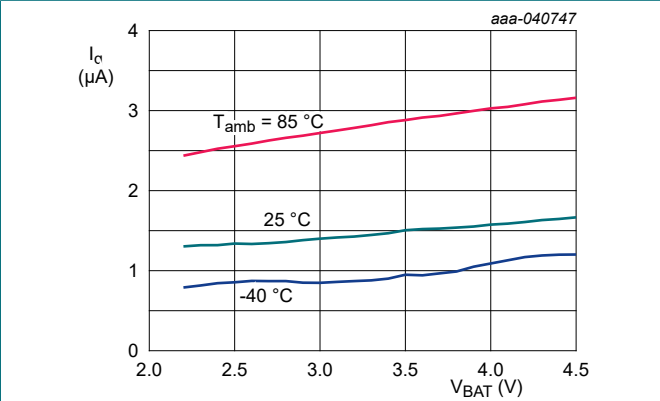


Fig. 3. Quiescent current vs. V<sub>BAT</sub> over temperature, LDO disabled

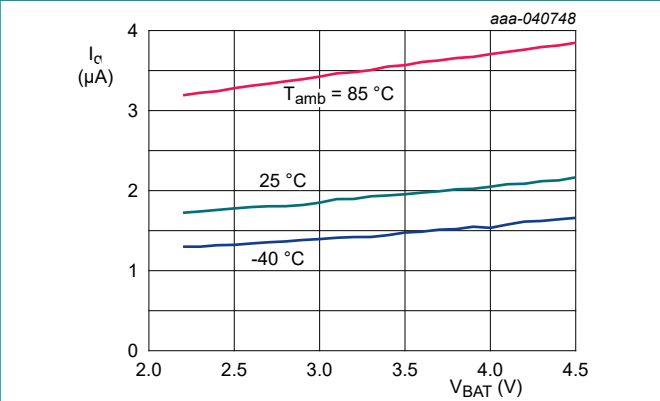


Fig. 4. Quiescent current vs. V<sub>BAT</sub> over temperature, LDO enabled

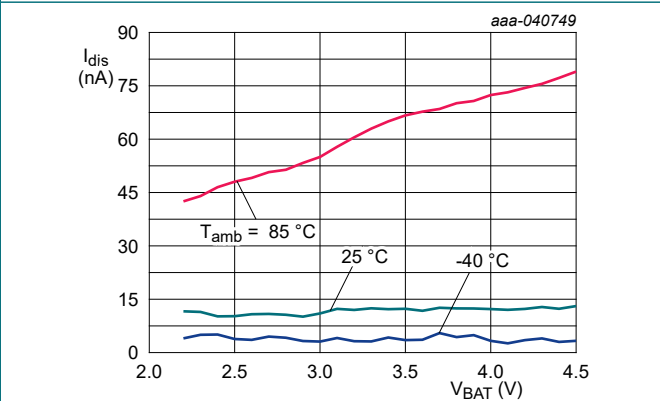


Fig. 5. Disable current vs. V<sub>BAT</sub> over temperature

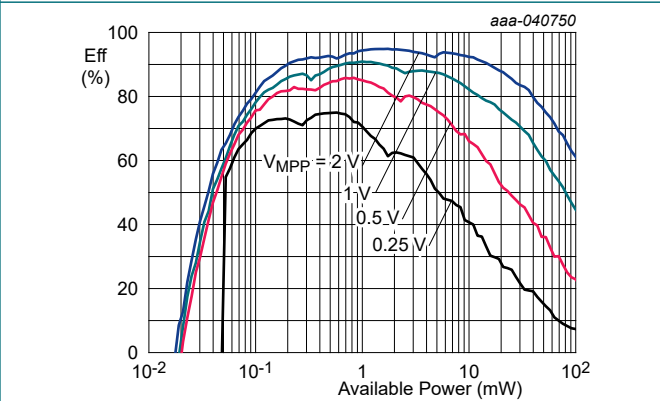


Fig. 6. Efficiency versus P<sub>av</sub> over boosting factors

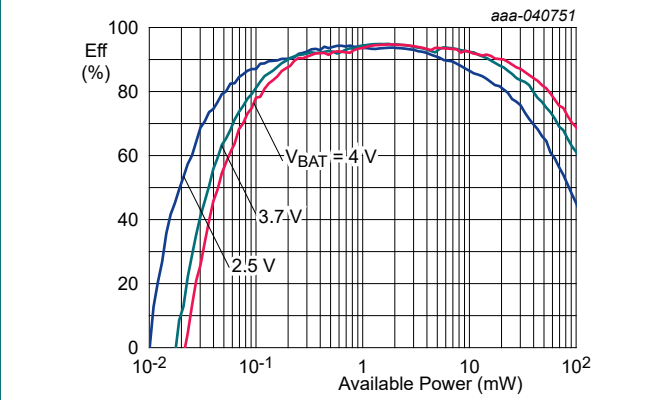


Fig. 7. Efficiency vs. P<sub>av</sub> over V<sub>BAT</sub>, V<sub>IN</sub> = V<sub>MPP</sub>

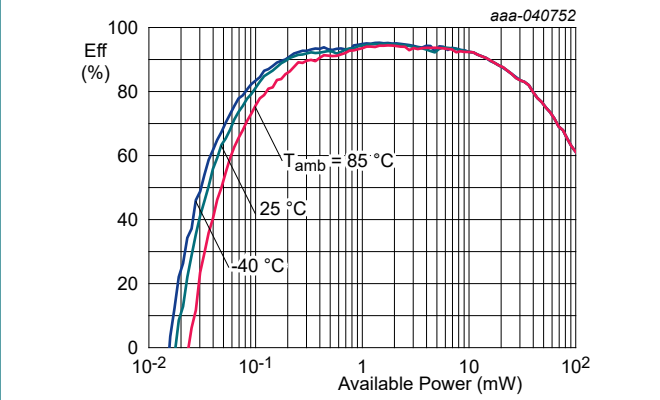


Fig. 8. Efficiency vs. P<sub>av</sub> over temperature, V<sub>MPP</sub> = 2 V



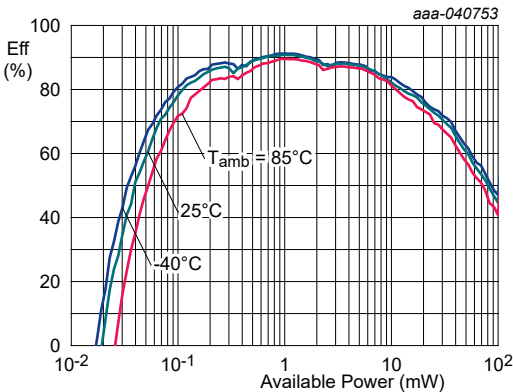


Fig. 9. Efficiency vs.  $P_{av}$  over temperature,  $V_{MPP} = 1\text{ V}$

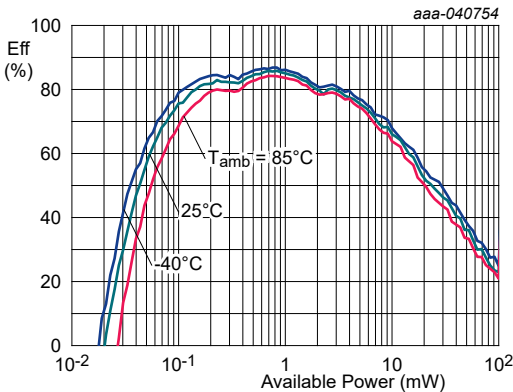


Fig. 10. Efficiency vs.  $P_{av}$  over temperature,  $V_{MPP} = 0.5\text{ V}$

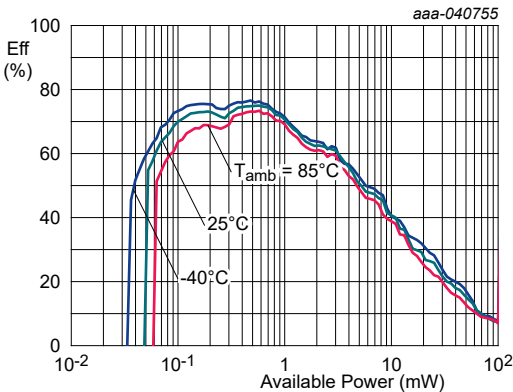


Fig. 11. Efficiency vs.  $P_{av}$  over temperature,  $V_{MPP} = 0.25\text{ V}$

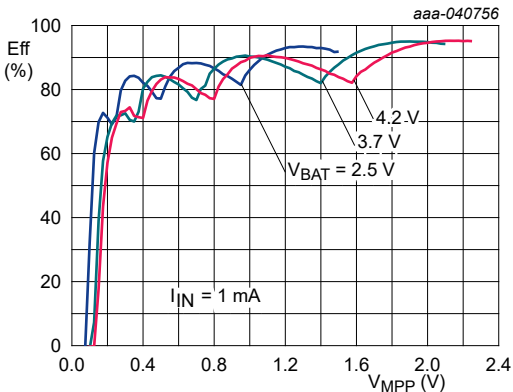


Fig. 12. Efficiency vs.  $V_{MPP}$  over  $V_{BAT}$

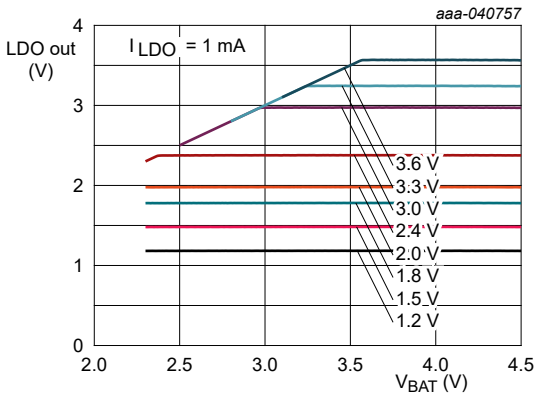


Fig. 13.  $V_{LDO}$  vs.  $V_{BAT}$  over LDO set voltages

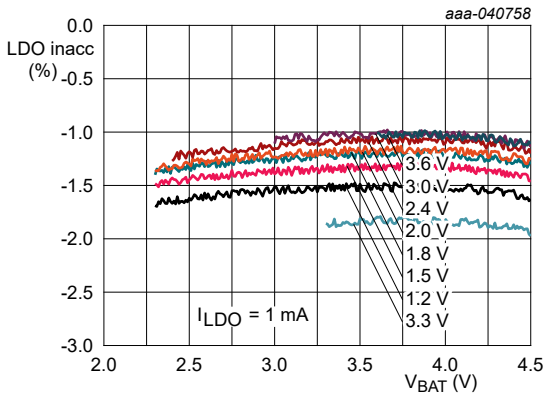


Fig. 14. LDO inaccuracy vs.  $V_{BAT}$  over LDO set voltages

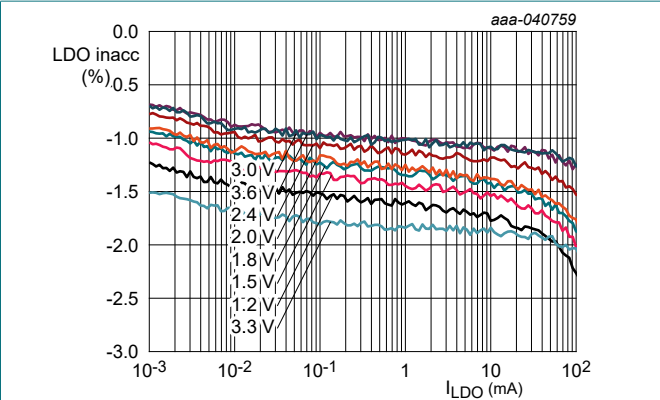


Fig. 15. LDO inaccuracy vs.  $I_{LDO}$  over LDO set voltages

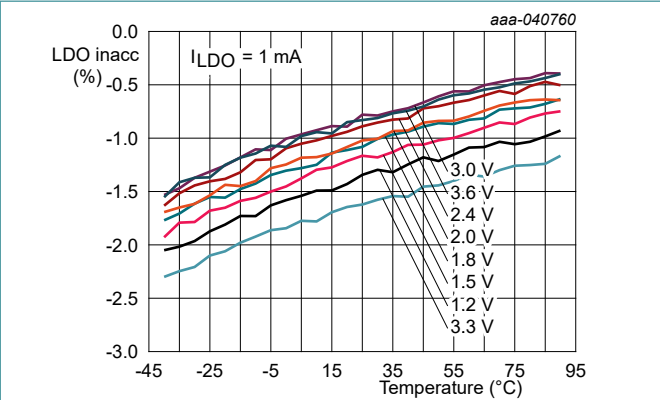
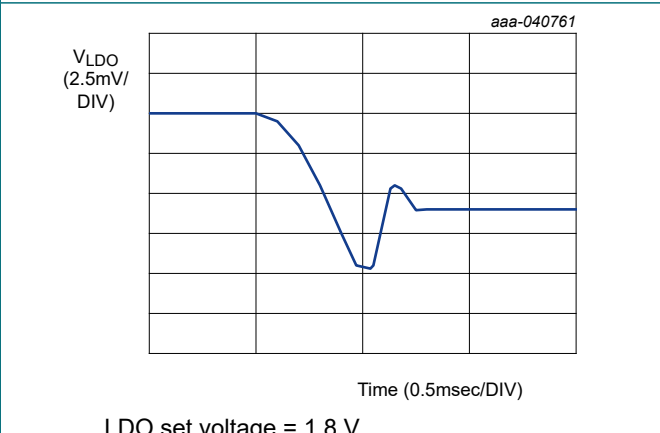
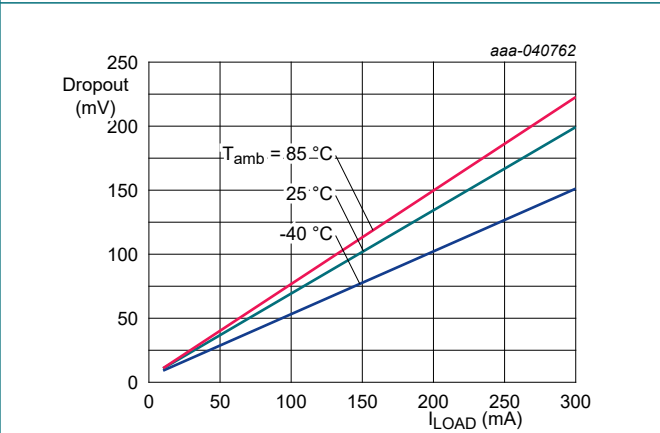


Fig. 16. LDO inaccuracy vs. temperature over LDO set voltages



LDO set voltage = 1.8 V  
Load step from no load to 1 mA

Fig. 17. LDO load transient vs. time



LDO set voltage = 3.6 V

Fig. 18. LDO dropout voltage vs.  $I_{LDO}$  over temperature

## 7. Detailed description

### 7.1. Overview

NEH7100 is an energy harvesting PMIC with a wide variety of auxiliary features as shown in the block diagram in [Fig. 19](#).

The converter boosts the input voltage at VIN of the NEH7100 to a level suitable to charge the storage element connected to VBAT. The MPPT block searches for the best configuration of the power converter for the highest output power. The storage element is protected against over charging by OVP circuitry. Similarly, the LVD circuit indicates when the storage element voltage is too low. In case the storage element is empty, the NEH7100 can resume operation via coldstart. As an alternative to energy harvesting, the storage element can also be charged via USB. The integrated LDO connected to VBAT provides a stable, regulated output voltage for the application. The NEH7100 can be configured via hard-code pins and I<sup>2</sup>C.

### 7.2. Block diagram

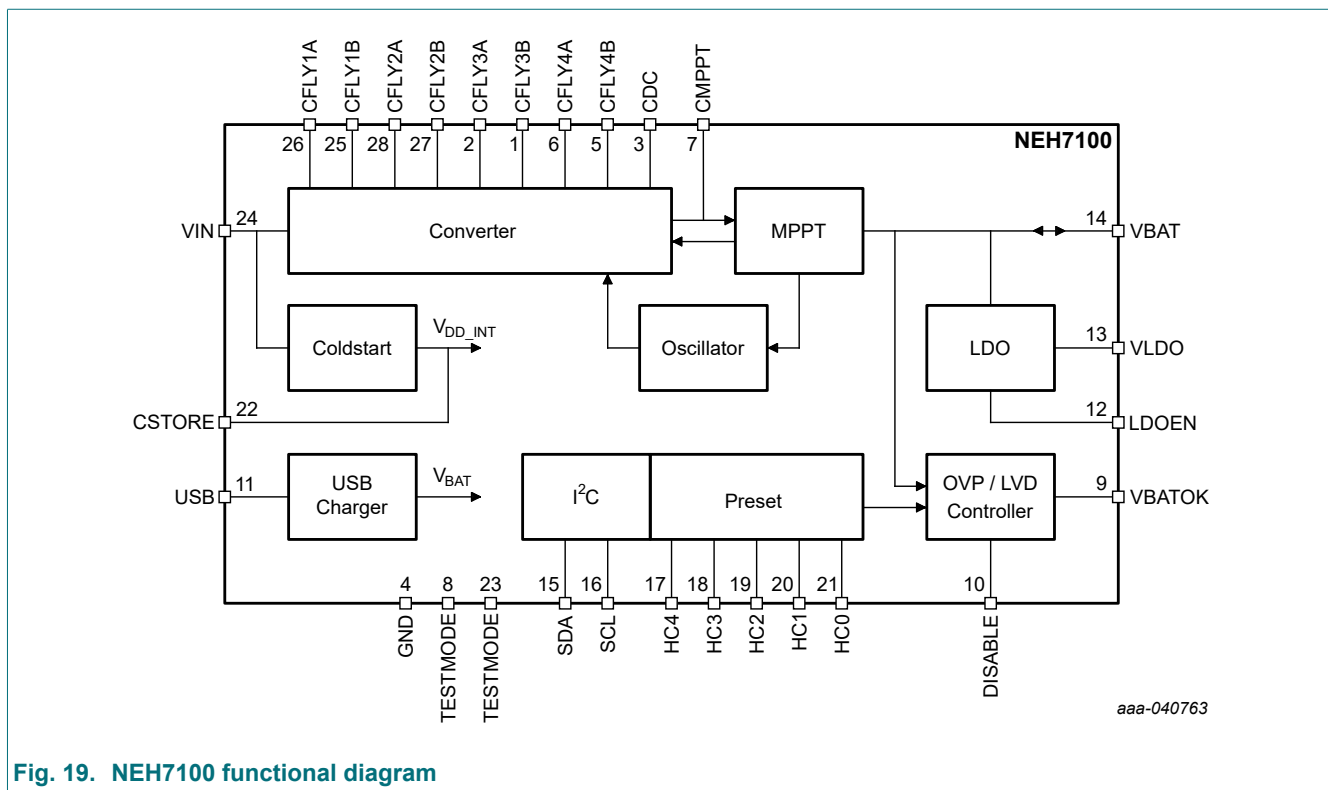


Fig. 19. NEH7100 functional diagram

### 7.3. Feature descriptions

#### 7.3.1. Converter / MPPT

The main converter of the NEH7100 boosts the input voltage,  $V_{IN}$ , to the storage element voltage,  $V_{BAT}$ . In normal operation,  $V_{STORE}$  is internally connected to  $V_{BAT}$ . Boosting factor and switching frequency of the converter are dynamically chosen by the MPPT hill-climbing algorithm for the best efficiency. Regularly, the MPPT engine checks whether a better configuration is available. The MPPT procedure is performed once every MPPT interval. The default MPPT interval is 1 second. The MPPT interval can be changed via register 0x05 defining the range from 0.5 to 64 s, see [Table 8](#).

**Table 8. MPPT interval, register 0x05 <2:0>**

| Bit <2> | Bit <1> | Bit <0> | MPPT interval (s) |
|---------|---------|---------|-------------------|
| 0       | 0       | 0       | 0.5               |
| 0       | 0       | 1       | 1                 |
| 0       | 1       | 0       | 2                 |
| 0       | 1       | 1       | 4                 |
| 1       | 0       | 0       | 8                 |
| 1       | 0       | 1       | 16                |
| 1       | 1       | 0       | 32                |
| 1       | 1       | 1       | 64                |

The MPPT search range for selecting the optimal boosting factor and switching frequency can be reduced. Both the lower and upper search boundaries can be set via I<sup>2</sup>C. Tightening the search boundaries can help in shortening MPPT search time and therewith (slightly) reducing current consumption. By default the full range is used by the MPPT engine.

The boosting factor (BF) boundaries can be configured via register 0x04.

**Table 9.  $BF_{(min)}$ , register 0x04 <1:0>**

| Bit <1> | Bit <0> | Lower boundary boosting factor range |
|---------|---------|--------------------------------------|
| 0       | 0       | 2x                                   |
| 0       | 1       | 4x                                   |
| 1       | 0       | 8x                                   |
| 1       | 1       | 16x                                  |

**Table 10.  $BF_{(max)}$ , register 0x04 <5:4>**

| Bit <5> | Bit <4> | Upper boundary boosting factor range |
|---------|---------|--------------------------------------|
| 0       | 0       | 2x                                   |
| 0       | 1       | 4x                                   |
| 1       | 0       | 8x                                   |
| 1       | 1       | 16x                                  |

Similar to limiting boosting factor range, frequency range can also be limited. This is done via register 0x03.

**Table 11. Frequency<sub>(min)</sub>, register 0x03 <2:0>**

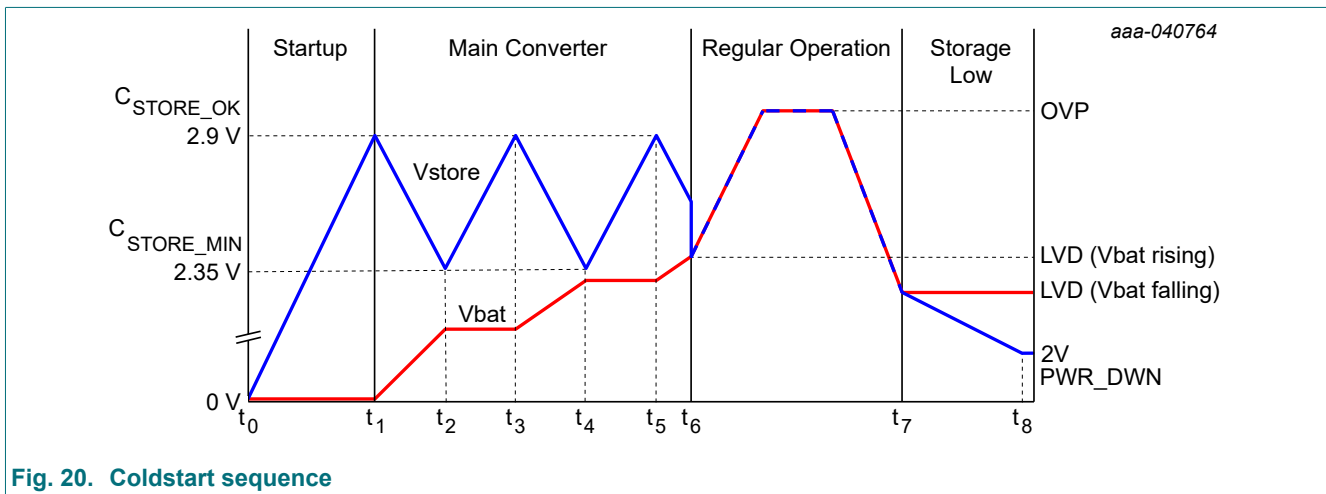
| Bit <2> | Bit <1> | Bit <0> | Lower boundary frequency range |
|---------|---------|---------|--------------------------------|
| 0       | 0       | 0       | 32 kHz                         |
| 0       | 0       | 1       | 64 kHz                         |
| 0       | 1       | 0       | 128 kHz                        |
| 0       | 1       | 1       | 256 kHz                        |
| 1       | 0       | 0       | 512 kHz                        |
| 1       | 0       | 1       | 1.024 MHz                      |
| 1       | 1       | 0       | 32 kHz                         |
| 1       | 1       | 1       | 32 kHz                         |

**Table 12. Frequency<sub>(max)</sub>, register 0x03 <6:4>**

| Bit <6> | Bit <5> | Bit <4> | Upper boundary frequency range |
|---------|---------|---------|--------------------------------|
| 0       | 0       | 0       | 32 kHz                         |
| 0       | 0       | 1       | 64 kHz                         |
| 0       | 1       | 0       | 128 kHz                        |
| 0       | 1       | 1       | 256 kHz                        |
| 1       | 0       | 0       | 512 kHz                        |
| 1       | 0       | 1       | 1.024 MHz                      |
| 1       | 1       | 0       | 1.024 MHz                      |
| 1       | 1       | 1       | 1.024 MHz                      |

### 7.3.2. Coldstart

Normally, the NEH7100 operates from the storage element, connected to V<sub>BAT</sub>. In case the storage element is depleted, the NEH7100 can resume operation via its coldstart feature. The device will collect energy from the harvester to power itself (via C<sub>STORE</sub>) and subsequently charge the storage element (via V<sub>BAT</sub>). The coldstart feature of the NEH7100 implements a controlled process, see Fig. 20. It needs a minimum input voltage of 270 mV and a minimum available input power of 12 µW to get the device running.



**Fig. 20. Coldstart sequence**

At the beginning of the coldstart operation, the coldstart power converter charges C<sub>STORE</sub> using energy available from V<sub>IN</sub>. Once the voltage across C<sub>STORE</sub> reaches 2.9 V (C<sub>STORE\_OK</sub>) at t<sub>1</sub>, the device starts up. At this moment, the coldstart power converter is disabled and the main power converter is enabled. The main power converter starts charging the storage element at V<sub>BAT</sub>, C<sub>STORE</sub> is not being charged anymore. Since the main power converter consumes current from C<sub>STORE</sub>, V<sub>STORE</sub> starts to go down. At t<sub>2</sub>, when it reaches 2.35 V (C<sub>STORE\_MIN</sub>) the main power converter switches to charging C<sub>STORE</sub>. This behavior continues to be repeated until V<sub>BAT</sub> reaches the LVD(Rising) threshold at t<sub>6</sub>, on which V<sub>BAT</sub> and C<sub>STORE</sub> are shorted together.

The main power converter continues to charge V<sub>BAT</sub> until the OVP threshold is reached. If there is no available energy at V<sub>IN</sub>, the storage element at V<sub>BAT</sub> and C<sub>STORE</sub> will be discharged due to the current consumption of the chip and the application. Once V<sub>BAT</sub> reaches the LVD(Falling) threshold while discharging, V<sub>BAT</sub> and C<sub>STORE</sub> are disconnected from each other. The device is still turned on and checking if there is any available power on V<sub>IN</sub>. In case power is available at V<sub>IN</sub> the process as indicated between t<sub>1</sub> and t<sub>6</sub> applies. In case no energy is available at V<sub>IN</sub>, V<sub>STORE</sub> keeps on lowering. Finally, if V<sub>STORE</sub> falls below 2 V (PWR\_DWN), the device is turned off. As soon as minimum power and voltage are present at V<sub>IN</sub>, the device will automatically start the sequence at t<sub>0</sub>.

### 7.3.3. USB charging

In addition to obtaining energy via the harvester, the storage element can also be charged via the USB pin. The charger can be configured for a certain current limit, see [Table 13](#). USB charging is automatically enabled when a voltage higher than 4 V is detected on the USB pin. The USB Charger uses CC charging until the OVP limit is reached where the charger changes to CV charging. The nominal USB charging current is equal to 80% of the maximum charging current setting. This is done to ensure that the maximum charging current, due to process and temperature variation, does not exceed the values shown in [Table 13](#).

**Table 13. USB charging current, register 0x01 <2:0>**

| Bit <2> | Bit <1> | Bit <0> | USB maximum charging current (mA) |
|---------|---------|---------|-----------------------------------|
| 0       | 0       | 0       | 0.5                               |
| 0       | 0       | 1       | 1                                 |
| 0       | 1       | 0       | 2                                 |
| 0       | 1       | 1       | 10                                |
| 1       | 0       | 0       | 50                                |
| 1       | 0       | 1       | 100                               |
| 1       | 1       | 0       | 150                               |
| 1       | 1       | 1       | 200                               |

NEH7100 USB charging current is defaulted during start up to assume the HC pin configuration. The charging current level is applied according to [Table 19](#).

### 7.3.4. Application LDO

To provide the required voltage to the application, an LDO is integrated. The LDO can be enabled and disabled using the LDOEN pin. The LDO output voltage can be set via register 0x01 over the range of 1.2 V to 3.6 V, see [Table 14](#) as well as [Section 7.3.7](#).

The LDO is supplied from VBAT and can deliver 200 mA with a dropout voltage below 300 mV. Optimal closed-loop stability requires the LDO capacitor value to be 47 µF. The capacitor should be placed as close as possible to the VLDO pin.

**Table 14. LDO output, register 0x01 <5:3>**

| Bit <5> | Bit <4> | Bit <3> | LDO output (V) |
|---------|---------|---------|----------------|
| 0       | 0       | 0       | 1.2            |
| 0       | 0       | 1       | 1.5            |
| 0       | 1       | 0       | 1.8            |
| 0       | 1       | 1       | 2.0            |
| 1       | 0       | 0       | 2.4            |
| 1       | 0       | 1       | 3.0            |
| 1       | 1       | 0       | 3.3            |
| 1       | 1       | 1       | 3.6            |

The LDO has a bypass mode to connect the VLDO pin to V<sub>BAT</sub>. In this case V<sub>VLDO</sub> will follow V<sub>BAT</sub> instead of regulating to the set voltage. There is also a control option on how the LDO is disabled. It can be either automatically disabled when the internal BATOK flag drops to 0, which happens when V<sub>BAT</sub> drops below the LVD threshold, or disabled only when the LDOEN pin voltage is set to 0 V. The bypass and LDO control can both be configured through register 0x01

Table 15. LDO Bypass, register 0x01 &lt;7&gt;

| Bit <7> | LDO Bypass  |
|---------|---|
| 0       | Normal mode: Operating as LDO   |
| 1       | Bypass mode: LDO acts as a switch. $V_{VLDO}$ will follow $V_{BAT}$ when the LDO is enabled |

Table 16. LDO Control, register 0x01 &lt;6&gt;

| Bit <6> | LDO CTRL   |
|---------|--|
| 0       | The LDO is enabled by the LDOEN pin.<br>The LDO is disabled either by the LDOEN pin or the internal VBATOK flag. |
| 1       | LDO is enabled and disabled by the LDOEN pin setting   |

### 7.3.5. Storage element over-voltage protection (OVP)

$V_{BAT}$  of NEH7100 is actively limited to a programmable voltage level to protect the storage element against over-charging. The level should be chosen such that it is close to, but below the allowed maximum charge voltage as specified in the storage element data sheet. This over-voltage protection applies for both charging via energy harvesting and charging via USB port. The OVP level can be set via register 0x00, see [Table 17](#) as well as [Section 7.3.7](#).

Table 17. Over-voltage protection levels, register 0x00 &lt;3:0&gt;

| Bit <3> | Bit <2> | Bit <1> | Bit <0> | Limit voltage (V) |
|---------|---------|---------|---------|-------------------|
| 0       | 0       | 0       | 0       | 2.7               |
| 0       | 0       | 0       | 1       | 2.9               |
| 0       | 0       | 1       | 0       | 3.1               |
| 0       | 0       | 1       | 1       | 3.3               |
| 0       | 1       | 0       | 0       | 3.4               |
| 0       | 1       | 0       | 1       | 3.5               |
| 0       | 1       | 1       | 0       | 3.6               |
| 0       | 1       | 1       | 1       | 3.7               |
| 1       | 0       | 0       | 0       | 3.8               |
| 1       | 0       | 0       | 1       | 3.9               |
| 1       | 0       | 1       | 0       | 4.0               |
| 1       | 0       | 1       | 1       | 4.1               |
| 1       | 1       | 0       | 0       | 4.2               |
| 1       | 1       | 0       | 1       | 4.3               |
| 1       | 1       | 1       | 0       | 4.4               |
| 1       | 1       | 1       | 1       | 4.5               |

7.3.6. Low voltage detection (LVD)

NEH7100 measures the storage element voltage to detect a too low voltage. The LVD threshold voltage can be set via register 0x00, see [Table 18](#) as well as [Section 7.3.7](#). If the storage element voltage is below the LVD threshold voltage, VBATOK is low. The LVD rising threshold voltage is LVD falling threshold voltage plus 150 mV. When V<sub>BAT</sub> rises above the LVD rising threshold, the VBATOK pin voltage rises to V<sub>BAT</sub>.

Table 18. Low-voltage detection levels, (falling storage element voltage) register 0x00 <7:4>

| Bit <7> | Bit <6> | Bit <5> | Bit <4> | LVD (V) |
|---------|---------|---------|---------|---------|
| 0       | 0       | 0       | 0       | 2.2     |
| 0       | 0       | 0       | 1       | 2.3     |
| 0       | 0       | 1       | 0       | 2.4     |
| 0       | 0       | 1       | 1       | 2.5     |
| 0       | 1       | 0       | 0       | 2.6     |
| 0       | 1       | 0       | 1       | 2.7     |
| 0       | 1       | 1       | 0       | 2.8     |
| 0       | 1       | 1       | 1       | 2.9     |
| 1       | 0       | 0       | 0       | 3.0     |
| 1       | 0       | 0       | 1       | 3.1     |
| 1       | 0       | 1       | 0       | 3.2     |
| 1       | 0       | 1       | 1       | 3.3     |
| 1       | 1       | 0       | 0       | 3.4     |
| 1       | 1       | 0       | 1       | 3.5     |
| 1       | 1       | 1       | 0       | 3.6     |
| 1       | 1       | 1       | 1       | 3.7     |



### 7.3.7. Hard-code settings and I<sup>2</sup>C

The NEH7100 can be configured in two ways: by hard-code settings pins HC0 to HC4 or via I<sup>2</sup>C programming. The hard-code settings enable easy configuration of the few most important parameters, while the I<sup>2</sup>C provide a wide range of configurable parameters. The hard-code settings are interpreted at the moment of power-up,  $V_{STORE}$  reaching  $C_{STORE\_OK}$  level of the device, and are not read again until the next power cycle. The HC input should be either connected to a logic "0" (GND) or "1" ( $V_{STORE}$ ). It is required to use  $V_{STORE}$ , rather than  $V_{BAT}$ , as a logic "1" or "HIGH" reference to guarantee correct HC settings during coldstart operation. The hard-code configuration options can be found in [Table 19](#). An I<sup>2</sup>C controller can communicate to NEH7100 using SDA and SCL pins on address 0x3C. Communication to the NEH7100 via I<sup>2</sup>C is based upon a register map table, see [Table 24](#).

**Table 19. Hard-code settings**

| HC4 | HC3 | HC2 | HC1 | HC0 | OVP (V) | LVD (V) | LDO (V) | OCP (mA) |
|-----|-----|-----|-----|-----|---------|---------|---------|----------|
| 0   | 0   | 0   | 0   | 0   | 4.2     | 3.5     | 3.3     | 200      |
| 0   | 0   | 0   | 0   | 1   |         | 3.2     | 3.0     |          |
| 0   | 0   | 0   | 1   | 0   |         | 2.6     | 2.4     |          |
| 0   | 0   | 0   | 1   | 1   |         | 2.2     | 2.0     |          |
| 0   | 0   | 1   | 0   | 0   |         |         | 1.8     |          |
| 0   | 0   | 1   | 0   | 1   |         |         | 1.5     |          |
| 0   | 0   | 1   | 1   | 0   |         |         | 1.2     |          |
| 0   | 0   | 1   | 1   | 1   |         |         | By-pass |          |
| 0   | 1   | 0   | 0   | 0   | 4.0     | 3.5     | 3.3     | 100      |
| 0   | 1   | 0   | 0   | 1   |         |         |         | 50       |
| 0   | 1   | 0   | 1   | 0   |         | 3.3     | 3.0     | 100      |
| 0   | 1   | 0   | 1   | 1   |         |         | 2.4     |          |
| 0   | 1   | 1   | 0   | 0   |         |         | 2.0     |          |
| 0   | 1   | 1   | 0   | 1   |         |         | 1.8     | 50       |
| 0   | 1   | 1   | 1   | 0   |         |         | 1.5     | 100      |
| 1   | 0   | 0   | 0   | 0   |         |         | 1.2     |          |
| 1   | 0   | 0   | 0   | 1   |         |         | By-pass | 10       |
| 1   | 0   | 0   | 1   | 0   |         |         | By-pass | 100      |
| 1   | 0   | 0   | 1   | 1   | 3.5     | 2.6     | 2.4     | 150      |
| 1   | 0   | 1   | 0   | 0   |         | 2.5     | 2.0     |          |
| 1   | 0   | 1   | 0   | 1   |         |         | 1.8     | 200      |
| 1   | 0   | 1   | 1   | 0   |         |         | 1.5     | 150      |
| 1   | 0   | 1   | 1   | 1   |         |         | 1.5     | 200      |
| 1   | 1   | 0   | 0   | 0   |         |         | 1.2     | 150      |
| 1   | 1   | 0   | 0   | 1   |         |         | By-pass |          |
| 1   | 1   | 0   | 1   | 0   |         |         | By-pass |          |
| 1   | 1   | 0   | 1   | 1   | 3.1     | 2.2     | 2.0     | 2        |
| 1   | 1   | 1   | 0   | 0   |         |         | 1.8     |          |
| 1   | 1   | 1   | 0   | 1   |         |         | 1.5     |          |
| 1   | 1   | 1   | 1   | 0   |         |         | 1.2     |          |
| 1   | 1   | 1   | 1   | 1   |         |         | By-pass |          |

8. Application and implementation

8.1. Typical application

A typical PV-cell application is shown in Fig. 21. Table 20 lists the Bill of Materials.

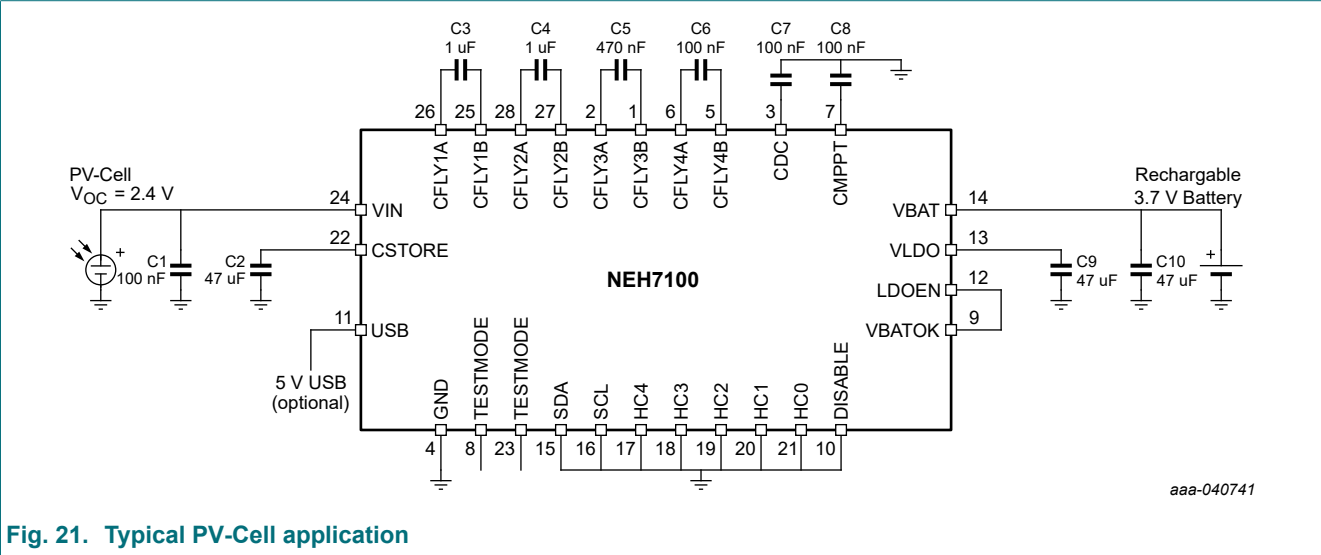


Fig. 21. Typical PV-Cell application

Table 20. Bill of Materials

| Quantity | Reference designator | Value                       | Description                              | Manufacturer Part Number |
|----------|----------------------|-----------------------------|--|--------------------------|
| 1        | U1                   | NEH7100                     | Energy Harvesting PMIC                   | NEH7100                  |
| 4        | C1, C6, C7, C8       | 0.1 $\mu$ F $\pm$ 10% 10 V  | ceramic capacitor X5R 0402 (1005 Metric) | GRM155R61A104KA01J       |
| 3        | C2, C9, C10          | 47 $\mu$ F $\pm$ 20% 6.3 V  | ceramic Capacitor X5R 0603 (1608 Metric) | GRM188R60J476ME15D       |
| 2        | C3, C4               | 1 $\mu$ F $\pm$ 20% 10 V    | ceramic capacitor X5R 0402 (1005 Metric) | GRM153R61A105ME95D       |
| 1        | C5                   | 0.47 $\mu$ F $\pm$ 10% 10 V | ceramic capacitor X5R 0402 (1005 Metric) | GRM155R61A474KE15D       |
| 1        | PV-Cell              | -                           | PV-cell with V <sub>OC</sub> = 2.4 V     | -                        |
| 1        | rechargeable battery | -                           | 3.7 V battery                            | -                        |

## 8.2. Optimizing application, reducing number of capacitors

The NEH7100 is capable of boosting the input voltage by 2, 4, 8 or 16 times to  $V_{BAT}$ . Depending on the used harvester and storage element, not all boosting factors might be needed. In this case one or more boosting factors can be bypassed. The associated capacitor(s) can be removed resulting in a reduced bill-of-material (BOM) and thus cost saving.

For best overall performance, the harvester's maximum-power-point voltage,  $V_{MPP}$ , should fit within the configured input voltage range. Fig. 22 depicts the overall efficiency versus the harvester's  $V_{MPP}$  given  $V_{BAT} = 3.7$  V. In case a harvester is not likely to operate in a part of the input voltage range, the input range might be reduced by excluding boosting factors. The maximum-power-point voltage is a characteristic of a harvester and varies based on environmental conditions such as light intensity and temperature. The  $V_{MPP}$  of a harvester is not always explicitly mentioned in its datasheet. For PV-cells, a good indicator for  $V_{MPP}$  is the open-circuit voltage ( $V_{OC}$ ) parameter. The relation between  $V_{OC}$  and  $V_{MPP}$ :

$$V_{MPP} = 0.7 \dots 0.9 \cdot V_{OC}$$

The typical MPP ratio ( $V_{MPP}/V_{OC}$ ) of a PV-cell is 0.8.

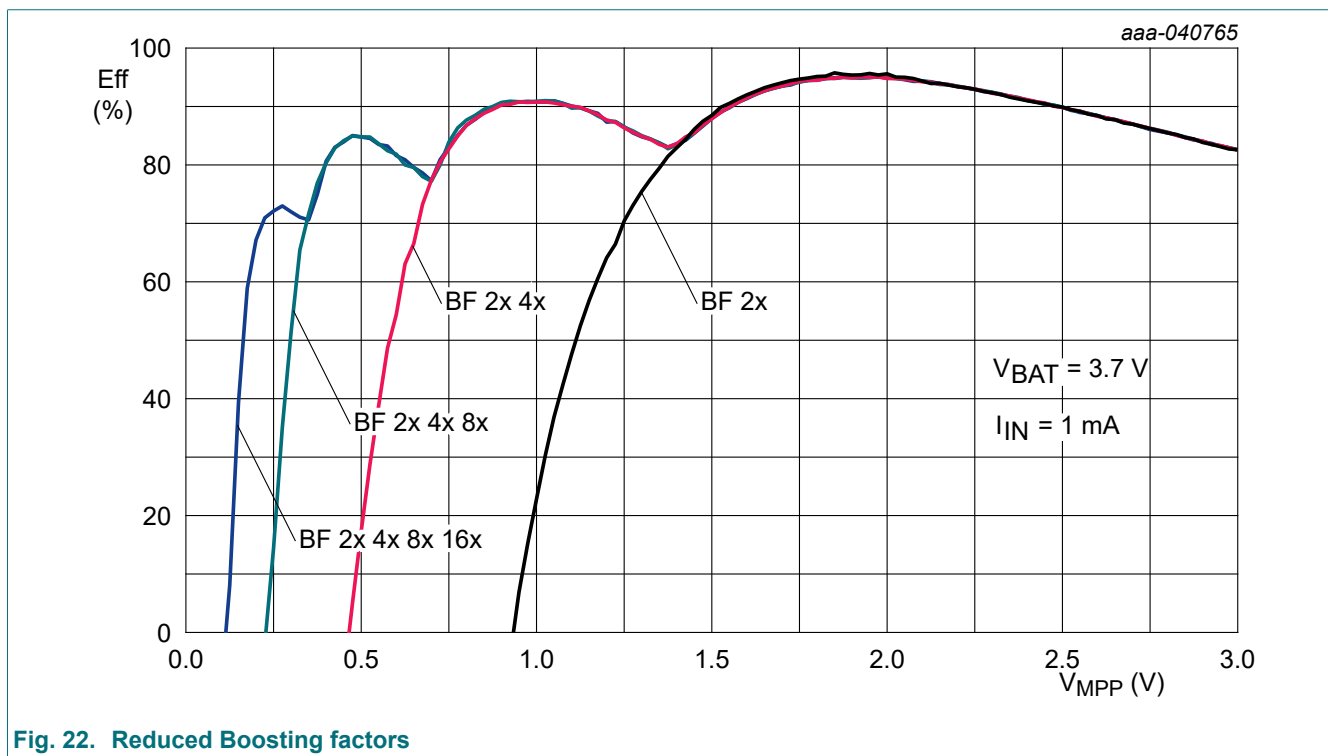


Table 21 provides the overview of  $V_{MPP}$  range for each boosting factor combination. The overall efficiency is not affected by reducing boosting factors if the harvester's  $V_{MPP}$  fits within the configured voltage range. The recommended  $V_{OC}$  range assumes a MPP ratio of 0.8.

**Table 21.  $V_{MPP}$  range for boosting factor combinations,  $V_{BAT} = 3.7$  V**

| Available Boosting Factors | $V_{MPP}$ (V) | $V_{OC}$ (V) |
|----------------------------|---------------|--------------|
| 2, 4, 8, 16                | 0.15 to 3     | 0.19 to 3.75 |
| 2, 4, 8                    | 0.3 to 3      | 0.38 to 3.75 |
| 2, 4                       | 0.63 to 3     | 0.78 to 3.75 |
| 2                          | 1.25 to 3     | 1.56 to 3.75 |

Fig. 23 to Fig. 26 show the four related configurations with different number of boosting factors enabled.

Inductorless energy harvesting PMIC with battery protection, LDO, USB charging and I<sup>2</sup>C

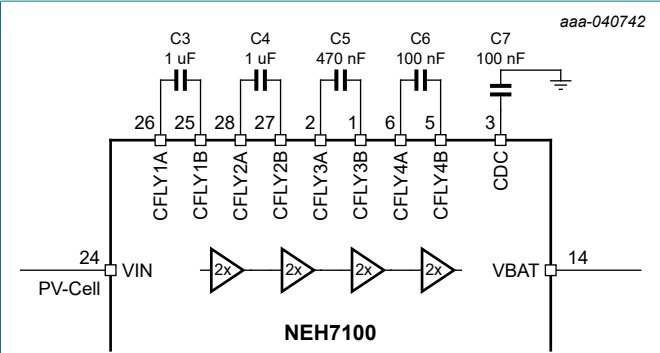


Fig. 23. Boosting factors: 2, 4, 8, 16

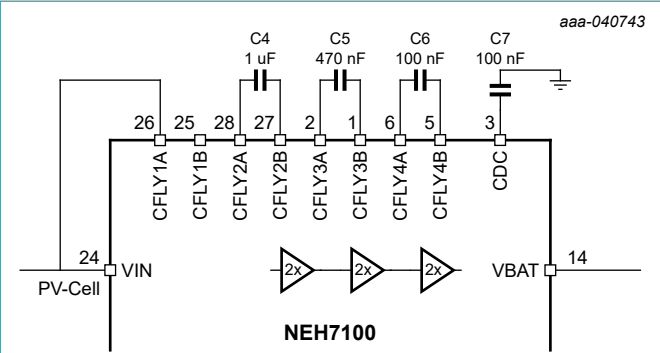


Fig. 24. Boosting factors: 2, 4, 8

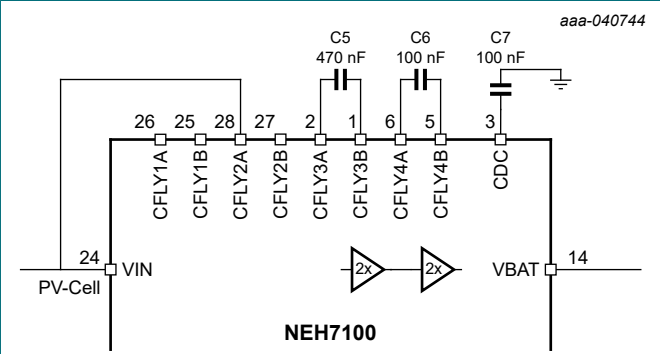


Fig. 25. Boosting factors: 2, 4

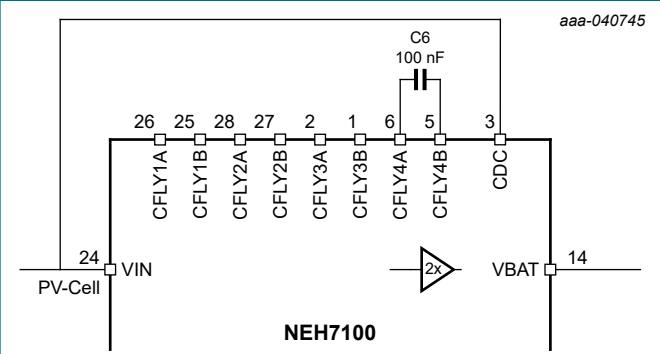


Fig. 26. Boosting factor: 2

Table 22 summarizes which capacitors can be omitted. For the reduced boosting factor configurations, a connection should be made between the input (VIN) and a particular flying-capacitor input pin.

Table 22. Configuration for reduced boosting factors

| Available Boosting Factors | Capacitor(s) removed | Connection from VIN to |
|----------------------------|----------------------|------------------------|
| 2, 4, 8, 16                | -                    | -                      |
| 2, 4, 8                    | C3                   | CFLY1A                 |
| 2, 4                       | C3, C4               | CFLY2A                 |
| 2                          | C3, C4, C5, C7       | CDC                    |

### 8.3. Harvesting efficiency

The overall efficiency (Eff) of the NEH7100 in combination with a harvester comprises two components (see Fig. 27):

- 1) Eff<sub>converter</sub> The efficiency of the power converter in the NEH7100
- 2) Eff<sub>match</sub> The matching efficiency between the NEH7100 and the harvester

The total efficiency can be described as:

$$\text{Eff} = \text{Eff}_{\text{converter}} \cdot \text{Eff}_{\text{match}}$$

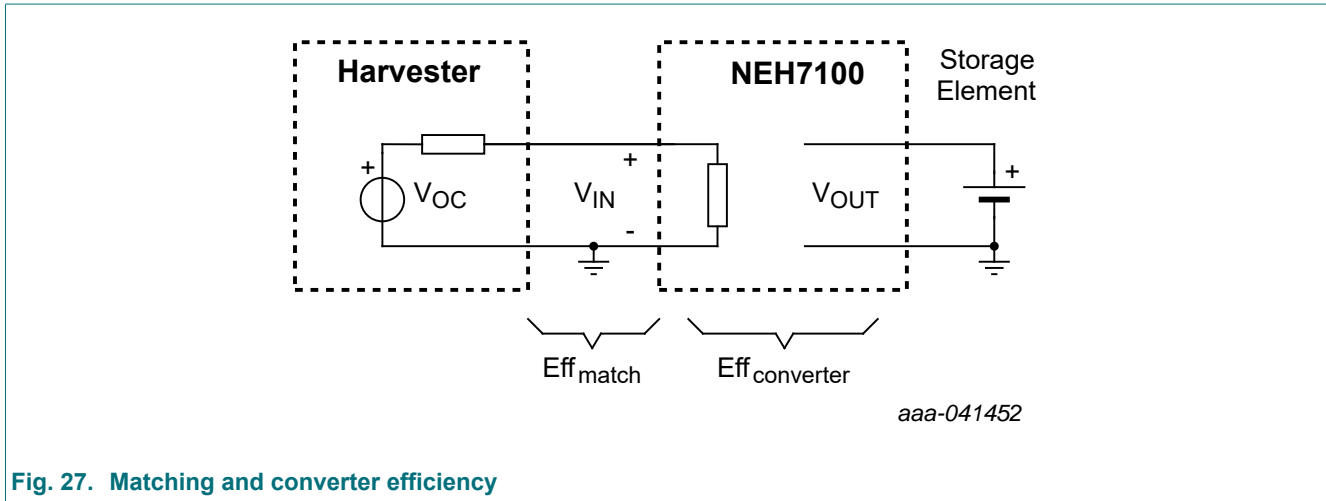


Fig. 27. Matching and converter efficiency

#### 8.3.1. Power converter efficiency

In practice, a power converter has losses from input power ( $P_{\text{IN}}$ ) to output power ( $P_{\text{OUT}}$ ). The ratio of the output power and input power is typically referred to as the power-converter efficiency:

$$\text{Eff}_{\text{converter}} = \frac{P_{\text{OUT}}}{P_{\text{IN}}} \cdot 100 \%$$

For common inductive and capacitive power converters this efficiency is in the range of 80 % to 95 %. Several characteristics can have an impact on this efficiency, such as: ratio of the output voltage and input voltage, quality and size of the converter capacitors. In its targeted power range the converter efficiency of the NEH7100 is about 94 %.

#### 8.3.2. Matching efficiency

In general, power transfer between components is optimized by matching the receiving input impedance with the transmitting output impedance. In a harvesting system it is also important to transfer power from harvester to the power converter in the most efficient manner to minimize loss of harvested energy. How optimal the power transfer between harvester and power converter is, can be expressed by matching efficiency.

The matching efficiency is defined as:

$$\text{Eff}_{\text{match}} = \frac{P_{\text{IN}}}{P_{\text{available}}} \cdot 100 \%$$

Where  $P_{\text{IN}}$  is the actual power at the input of the power converter and  $P_{\text{available}}$  is the maximum power that can be achieved at the input (which is at 100% matching).

From the graphs in Section 6.6, (Fig. 6 to Fig. 12), it can be seen that the matching efficiency as part of the overall efficiency has a dependency on the ratio of  $V_{\text{MPP}}$  and  $V_{\text{BAT}}$ . The  $V_{\text{BAT}}$  relation can be understood from the perspective that the capacitive power converter has a given boost factor between input and output:

$$V_{\text{IN}} = \frac{V_{\text{BAT}}}{\text{boosting factor}}$$

Where the boosting factor of the NEH7100 can be 2, 4, 8 or 16. The maximum power-point voltage ( $V_{MPP}$ ) is the voltage on the power converter's input where most power is delivered by the harvester.

Thus, for optimal matching efficiency a harvester should be chosen with a  $V_{MPP}$  close to  $V_{BAT}$  / boosting factor. Since the efficiency of the PMIC is highest at the lowest boosting factor, this is the preferred boosting factor. In case the optimum PV cell is not available, the impact on the overall efficiency is limited, i.e. up to about 10 %, see Fig. 12. This limited efficiency impact is as a result of the MPPT algorithm that can change more configuration parameters of the power converter than only the boosting factor.

8.4. Charge current measurement

For determining the best possible power converter configuration, the NEH7100 has an integrated current measurement. The measurement engine can be used to estimate the charging current to the storage element.

The current is measured across a sense resistor. There are four possible sense resistors. Each sense resistor is dedicated for a certain current range. Depending on the current, a sense resistor is dynamically chosen. Which current range is applied for the measurement can be read from the I\_RANGE register 0x09. After every MPPT optimization cycle, a new value is written in I\_MEASURE register 0x0A. The register value needs to be converted into a charge current.

Table 23. Calculating charge current

| I_RANGE<br>0x09<1:0> | I <sub>BAT</sub> (A)       |
|----------------------|----------------------------|
| 00                   | 70.6 nA * I_MEASURE (0x0A) |
| 01                   | 478 nA * I_MEASURE (0x0A)  |
| 10                   | 4.71 μA * I_MEASURE (0x0A) |
| 11                   | 67.5 μA * I_MEASURE (0x0A) |

9. Register map

Table 24. Register map

| Address (HEX) | Bits | Field name | Description (Bold face values are reset values) | READ WRITE | Power ON value (HEX)  |
|---------------|------|------------|---|------------|-----------------------|
| 0x00          | 7:4  | LVD        | falling low-voltage detection level (V)         | R/W        | set by hard-code pins |
|               |      |            | 0000: 2.2                                       |            |                       |
|               |      |            | 0001: 2.3                                       |            |                       |
|               |      |            | 0010: 2.4                                       |            |                       |
|               |      |            | 0011: 2.5                                       |            |                       |
|               |      |            | 0100: 2.6                                       |            |                       |
|               |      |            | 0101: 2.7                                       |            |                       |
|               |      |            | 0110: 2.8                                       |            |                       |
|               |      |            | 0111: 2.9                                       |            |                       |
|               |      |            | 1000: 3.0                                       |            |                       |
|               |      |            | 1001: 3.1                                       |            |                       |
|               |      |            | 1010: 3.2                                       |            |                       |
|               |      |            | 1011: 3.3                                       |            |                       |
|               |      |            | 1100: 3.4                                       |            |                       |
|               |      |            | 1101: 3.5                                       |            |                       |
|               |      |            | 1110: 3.6                                       |            |                       |
|               |      |            | 1111: 3.7                                       |            |                       |
|               | 3:0  | OVP        | over-voltage protection level (V)               |            |                       |
|               |      |            | 0000: 2.7                                       |            |                       |
|               |      |            | 0001: 2.9                                       |            |                       |
|               |      |            | 0010: 3.1                                       |            |                       |
|               |      |            | 0011: 3.3                                       |            |                       |
|               |      |            | 0100: 3.4                                       |            |                       |
|               |      |            | 0101: 3.5                                       |            |                       |
|               |      |            | 0110: 3.6                                       |            |                       |
|               |      |            | 0111: 3.7                                       |            |                       |
|               |      |            | 1000: 3.8                                       |            |                       |
|               |      |            | 1001: 3.9                                       |            |                       |
|               |      |            | 1010: 4.0                                       |            |                       |
|               |      |            | 1011: 4.1                                       |            |                       |
|               |      |            | 1100: 4.2                                       |            |                       |
|               |      |            | 1101: 4.3                                       |            |                       |
|               |      |            | 1110: 4.4                                       |            |                       |
|               |      |            | 1111: 4.5                                       |            |                       |

Inductorless energy harvesting PMIC with battery protection, LDO, USB charging and I<sup>2</sup>C

| Address (HEX) | Bits | Field name           | Description (Bold face values are reset values)                                     | READ<br>WRITE | Power ON<br>value (HEX) |
|---------------|------|----------------------|---|---------------|-------------------------|
| 0x01          | 7    | LDO_BP               | mode control of the LDO when LDOEN is high.   | R/W           | set by hard-code pins   |
|               |      |                      | 0: Normal mode: Operating as LDO  |               |                         |
|               |      |                      | 1: Bypass mode: LDO acts as a switch. V <sub>LDO</sub> will follow V <sub>BAT</sub> |               |                         |
|               | 6    | LDO_CTRL             | Sets how LDO responds on VBATOK = 0   |               |                         |
|               |      |                      | 0: LDO automatically disables on VBATOK = 0, even if LDOEN is high                  |               |                         |
|               |      |                      | <b>1: LDO acts based on LDOEN setting</b>   |               |                         |
|               | 5:3  | VLDO                 | LDO output voltage (V)  |               |                         |
|               |      |                      | 000: 1.2  |               |                         |
|               |      |                      | 001: 1.5  |               |                         |
|               |      |                      | 010: 1.8  |               |                         |
|               |      |                      | 011: 2.0  |               |                         |
|               |      |                      | 100: 2.4  |               |                         |
|               |      |                      | 101: 3.0  |               |                         |
|               |      |                      | 110: 3.3  |               |                         |
|               |      |                      | 111: 3.6  |               |                         |
|               | 2:0  | I <sub>USB_max</sub> | maximum storage element charging current (mA) via USB                               |               |                         |
|               |      |                      | 000: 0.5  |               |                         |
|               |      |                      | 001: 1  |               |                         |
|               |      |                      | 010: 2  |               |                         |
|               |      |                      | 011: 10   |               |                         |
|               |      |                      | 100: 50   |               |                         |
|               |      |                      | 101: 100  |               |                         |
|               |      |                      | 110: 150  |               |                         |
|               |      |                      | 111: 200  |               |                         |
| 0x02          | 7:0  | Reserved             | reserved  | R/W           | -                       |



Inductorless energy harvesting PMIC with battery protection, LDO, USB charging and I<sup>2</sup>C

| Address (HEX) | Bits | Field name    | Description (Bold face values are reset values) | READ<br>WRITE | Power ON<br>value (HEX) |
|---------------|------|---------------|---|---------------|-------------------------|
| 0x03          | 7    | Reserved      | reserved  | R/W           | 70                      |
|               | 6:4  | $f_{(max)}$   | PC upper boundary frequency range               |               |                         |
|               |      |               | 000: 32 kHz                                     |               |                         |
|               |      |               | 001: 64 Hz                                      |               |                         |
|               |      |               | 010: 128 kHz                                    |               |                         |
|               |      |               | 011: 256 kHz                                    |               |                         |
|               |      |               | 100: 512 kHz                                    |               |                         |
|               |      |               | 101: 1.024 MHz                                  |               |                         |
|               |      |               | 110 and 111: <b>1.024 MHz</b>                   |               |                         |
|               | 3    | Reserved      | reserved  |               |                         |
|               | 2:0  | $f_{(min)}$   | PC lower boundary frequency range               |               |                         |
|               |      |               | <b>000: 32 kHz</b>                              |               |                         |
|               |      |               | 001: 64 kHz                                     |               |                         |
|               |      |               | 010: 128 kHz                                    |               |                         |
|               |      |               | 011: 256 kHz                                    |               |                         |
|               |      |               | 100: 512 kHz                                    |               |                         |
|               |      |               | 101: 1.024 MHz                                  |               |                         |
|               |      |               | 110 and 111: 32 kHz                             |               |                         |
| 0x04          | 7:6  | Reserved      | reserved  | R/W           | 30                      |
|               | 5:4  | $BF_{MAX}$    | upper boundary boosting factor range            |               |                         |
|               |      |               | 00: 2x  |               |                         |
|               |      |               | 01: 4x  |               |                         |
|               |      |               | 10: 8x  |               |                         |
|               |      |               | <b>11: 16x</b>                                  |               |                         |
|               | 3:2  | Reserved      | reserved  |               |                         |
|               | 1:0  | $BF_{MIN}$    | lower boundary boosting factor range            |               |                         |
|               |      |               | <b>00: 2x</b>                                   |               |                         |
|               |      |               | 01: 4x  |               |                         |
|               |      |               | 10: 8x  |               |                         |
|               |      |               | 11: 16x   |               |                         |
| 0x05          | 7:3  | Reserved      | reserved  | R/W           | 01                      |
|               | 2:0  | MPPT interval | MPPT interval                                   |               |                         |
|               |      |               | 000: 0.5 s                                      |               |                         |
|               |      |               | <b>001: 1 s</b>                                 |               |                         |
|               |      |               | 010: 2 s  |               |                         |
|               |      |               | 011: 4 s  |               |                         |
|               |      |               | 100: 8 s  |               |                         |
|               |      |               | 101: 16 s                                       |               |                         |
|               |      |               | 110: 32s  |               |                         |
|               |      |               | 111: 64 s                                       |               |                         |
| 0x06          | 7:0  | Reserved      | reserved  | R/W           | -                       |
| 0x07          | 7:0  | Chip_ID       | product ID and version                          | R             | -                       |
|               |      |               | Chip_ID = '0x15'                                |               |                         |

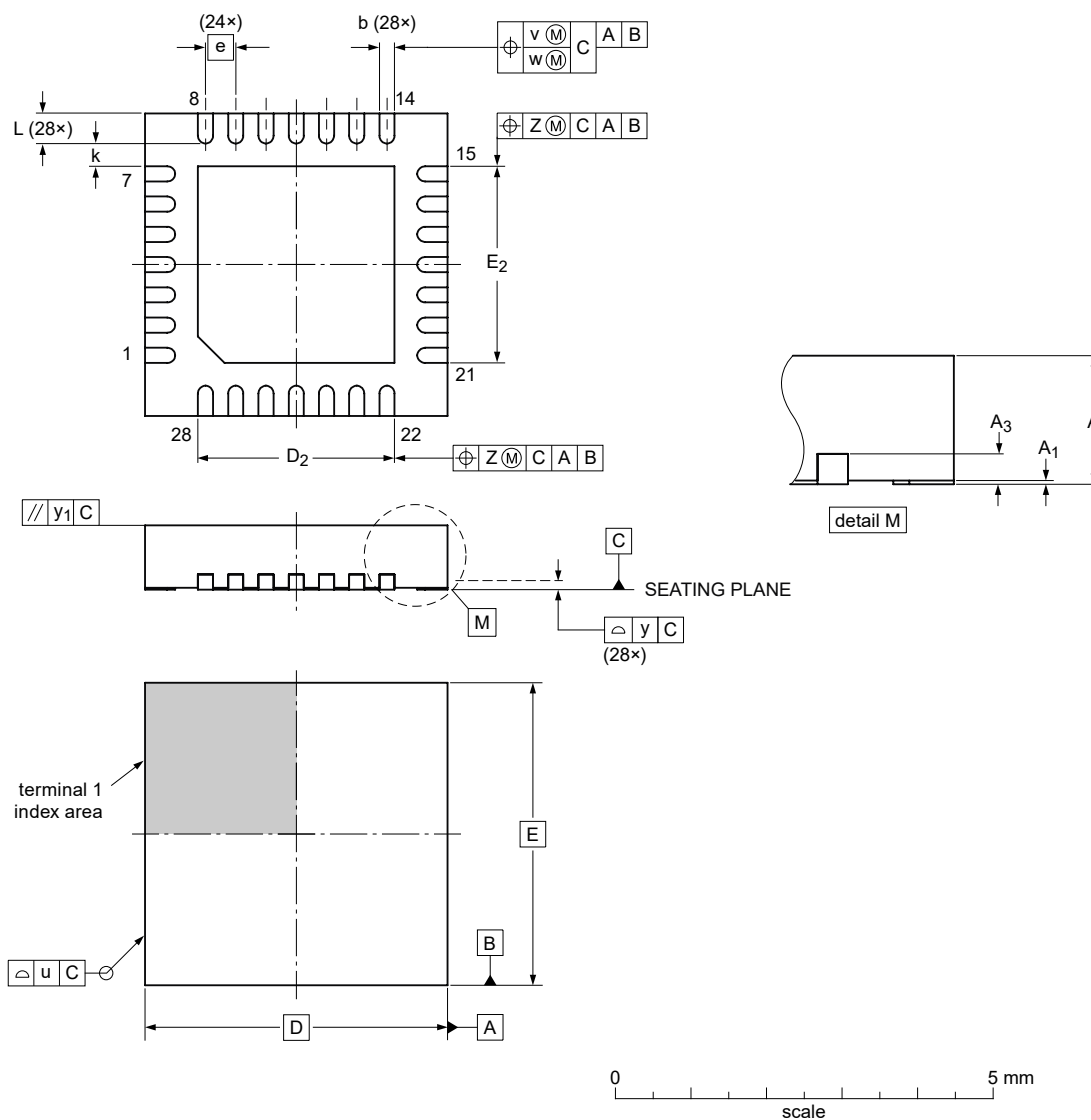
Inductorless energy harvesting PMIC with battery protection, LDO, USB charging and I<sup>2</sup>C

| Address (HEX) | Bits | Field name | Description (Bold face values are reset values)  | READ<br>WRITE | Power ON<br>value (HEX) |
|---------------|------|------------|--|---------------|-------------------------|
| 0x08          | 7:5  | Reserved   | reserved   | R             | -                       |
|               | 4    | OVP_OUT    | OVP flag (active high)   |               |                         |
|               |      |            | 0: V <sub>BAT</sub> is below OVP threshold   |               |                         |
|               |      |            | 1: V <sub>BAT</sub> is above OVP threshold   |               |                         |
|               | 3    | LVD_OUT    | LVD flag (active high)   |               |                         |
|               |      |            | 0: V <sub>BAT</sub> is above LVD threshold   |               |                         |
|               |      |            | 1: V <sub>BAT</sub> is below LVD threshold   |               |                         |
|               | 2    | SDF        | shutdown flag (active high)  |               |                         |
|               |      |            | 0: Harvesting mode, sufficient harvesting  |               |                         |
|               |      |            | 1: Device will be in low-power consumption mode, (too) low battery harvesting current measured. When current increases, harvesting will resume.        |               |                         |
|               | 1    | OCF        | overcurrent flag (active high)   |               |                         |
|               |      |            | 0: I <sub>BAT</sub> is below OCP level as specified in <a href="#">Table 19</a>  |               |                         |
|               |      |            | 1: I <sub>BAT</sub> is above OCP level as specified in <a href="#">Table 19</a>  |               |                         |
| 0x09          | 7:2  | Reserved   | reserved   | R             | -                       |
|               |      |            |  |               |                         |
| 0x0A          | 7:0  | I_MEASURED | MPPT engine latest selected current range  | R             | -                       |
|               |      |            | MPPT engine latest current measurement. The formula for I <sub>BAT</sub> current depends on the used I_RANGE (register 0x09<1:0>) for the measurement. |               |                         |
|               |      |            | I <sub>BAT</sub> = I_MEASURED * 70.6 nA (I_RANGE 00)   |               |                         |
|               |      |            | I <sub>BAT</sub> = I_MEASURED * 478 nA (I_RANGE 01)  |               |                         |
|               |      |            | I <sub>BAT</sub> = I_MEASURED * 4.71 μA (I_RANGE 10)   |               |                         |
|               |      |            | I <sub>BAT</sub> = I_MEASURED * 67.5 μA (I_RANGE 11)   |               |                         |

## 10. Package outline

**HVQFN28: plastic, leadless thermal enhanced very thin quad flat package; 28 terminals; 0.4 mm pitch; 4 mm x 4 mm x 0.85 mm body**


**SOT8080-1**



Dimensions (mm are the original dimensions)

| Unit <sup>(1)</sup> |     | A    | A <sub>1</sub> | A <sub>3</sub> | b    | <span style="border: 1px solid black;">D</span> | D <sub>2</sub> | <span style="border: 1px solid black;">E</span> | E <sub>2</sub> | <span style="border: 1px solid black;">e</span> | k   | L   | u   | v    | w    | y    | y <sub>1</sub> | z   |
|---------------------|-----|------|----------------|----------------|------|---|----------------|---|----------------|---|-----|-----|-----|------|------|------|----------------|-----|
| mm                  | max | 0.90 | 0.05           |                | 0.25 |   | 2.7            |   | 2.7            |   |     | 0.5 |     |      |      |      |                |     |
|                     | nom | 0.85 | 0.02           | 0.2            | 0.20 | 4.0   | 2.6            | 4.0   | 2.6            | 0.4   | 0.3 | 0.4 | 0.1 | 0.07 | 0.05 | 0.08 | 0.1            | 0.1 |
|                     | min | 0.80 | 0              | REF            | 0.17 | BSC   | 2.5            | BSC   | 2.5            | BSC   | REF | 0.3 |     |      |      |      |                |     |

sot8080-1 po

| Outline version | References |        |       |  | European projection   | Issue date |
|-----------------|------------|--------|-------|--|---|------------|
|                 | IEC        | JEDEC  | JEITA |  |   |            |
| SOT8080-1       |            | MO-220 |       |  |  | 23-09-12   |

**Fig. 28. Package outline SOT8080-1 (HVQFN28)**

## 11. Revision history

Table 25. Revision history

| Document ID  | Release date  | Data sheet status  | Change notice | Supersedes  |
|--------------|---|--------------------|---------------|-------------|
| NEH7100 v.2  | 20250905  | Product data sheet | -             | NEH7100 v.1 |
| Modification | For <a href="#">Section 2</a> : <ul style="list-style-type: none"><li>Added a new feature.</li><li>Updated "Harvesting power range" to "Chip input power range: 15 µW to 100 mW".</li></ul> |                    |               |             |
| NEH7100 v.1  | 20241217  | Product data sheet | -             | -           |

## 12. Legal information

### Data sheet status

| Document status [1][2]         | Product status [3] | Definition  |
|--------------------------------|--------------------|---|
| Objective [short] data sheet   | Development        | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification      | This document contains data from the preliminary specification.                       |
| Product [short] data sheet     | Production         | This document contains the product specification.                                     |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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## Contents

|  |           |
|--|-----------|
| <b>1. General description</b>                              | <b>1</b>  |
| <b>2. Features and benefits</b>                            | <b>1</b>  |
| <b>3. Applications</b>                                     | <b>1</b>  |
| <b>4. Ordering information</b>                             | <b>2</b>  |
| <b>5. Pinning information</b>                              | <b>2</b>  |
| 5.1. Pinning configuration                                 | 2         |
| 5.2. Pinning description                                   | 3         |
| <b>6. Specifications</b>                                   | <b>4</b>  |
| 6.1. Absolute maximum ratings                              | 4         |
| 6.2. ESD ratings   | 4         |
| 6.3. Recommended operating conditions                      | 4         |
| 6.4. Thermal information                                   | 4         |
| 6.5. Electrical characteristics                            | 5         |
| 6.6. Typical characteristics                               | 8         |
| <b>7. Detailed description</b>                             | <b>11</b> |
| 7.1. Overview  | 11        |
| 7.2. Block diagram   | 11        |
| 7.3. Feature descriptions                                  | 12        |
| 7.3.1. Converter / MPPT                                    | 12        |
| 7.3.2. Coldstart   | 13        |
| 7.3.3. USB charging  | 14        |
| 7.3.4. Application LDO                                     | 14        |
| 7.3.5. Storage element over-voltage protection (OVP)       | 15        |
| 7.3.6. Low voltage detection (LVD)                         | 16        |
| 7.3.7. Hard-code settings and I <sup>2</sup> C             | 17        |
| <b>8. Application and implementation</b>                   | <b>18</b> |
| 8.1. Typical application                                   | 18        |
| 8.2. Optimizing application, reducing number of capacitors | 19        |
| 8.3. Harvesting efficiency                                 | 21        |
| 8.3.1. Power converter efficiency                          | 21        |
| 8.3.2. Matching efficiency                                 | 21        |
| 8.4. Charge current measurement                            | 22        |
| <b>9. Register map</b>                                     | <b>23</b> |
| <b>10. Package outline</b>                                 | <b>27</b> |
| <b>11. Revision history</b>                                | <b>28</b> |
| <b>12. Legal information</b>                               | <b>29</b> |

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