



MMBZ33VBQC-Q

Low capacitance bidirectional dual line ESD protection diode

18 July 2024

Product data sheet

1. General description

ESD protection device in an ultra small DFN1412D-3 (SOT8009) leadless Surface-Mounted Device (SMD) plastic package with side wettable flanks, designed to protect two lines from the damage caused by ElectroStatic Discharge (ESD) and other transients.

2. Features and benefits

- Reverse stand-off voltage: $V_{RWM} = 27\text{ V}$
- Low clamping voltage: $V_{CL} = 33\text{ V}$ at $I_{PP} = 2.5\text{ A}$
- ESD protection up to 20 kV (IEC 61000-4-2)
- ESD protection up to 20 kV (ISO 10605)
- Low capacitance: $C_d = 8\text{ pF}$
- Qualified according to AEC-Q101 and recommended for use in automotive applications

3. Applications

- Computers and peripherals
- Audio and video equipment
- Cellular handsets and accessories
- Automotive electronic control units
- Portable electronics

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	$T_{amb} = 25\text{ °C}$		-	-	27	V
I_{PPM}	rated peak pulse current	$t_p = 8/20\text{ }\mu\text{s}$	[1] [2]	-	-	2.5	A
V_{CL}	clamping voltage	$I_{PPM} = 2.5\text{ A}$; $t_p = 8/20\text{ }\mu\text{s}$; $T_{amb} = 25\text{ °C}$	[2] [3]	-	33	44	V

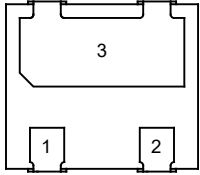
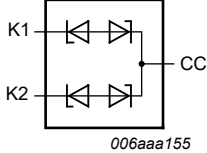
[1] According to IEC 61000-4-5

[2] Measured from pin 1 or 2 to pin 3

[3] Device stressed with 8/20 μs exponential decay waveform according to IEC 61000-4-5

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode (diode 1)	 <p>Transparent top view DFN1412D-3 (SOT8009)</p>	 <p>006aaa155</p>
2	K2	cathode (diode 2)		
3	CC	common cathode		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
MMBZ33VBQC-Q	DFN1412D-3	plastic, leadless ultra small outline package with side-wettable flanks (SWF); 3 terminals; 0.8 mm pitch; 1.4 mm x 1.2 mm x 0.48 mm body	SOT8009

7. Marking

Table 4. Marking codes

Type number	Marking code
MMBZ33VBQC-Q	Q6

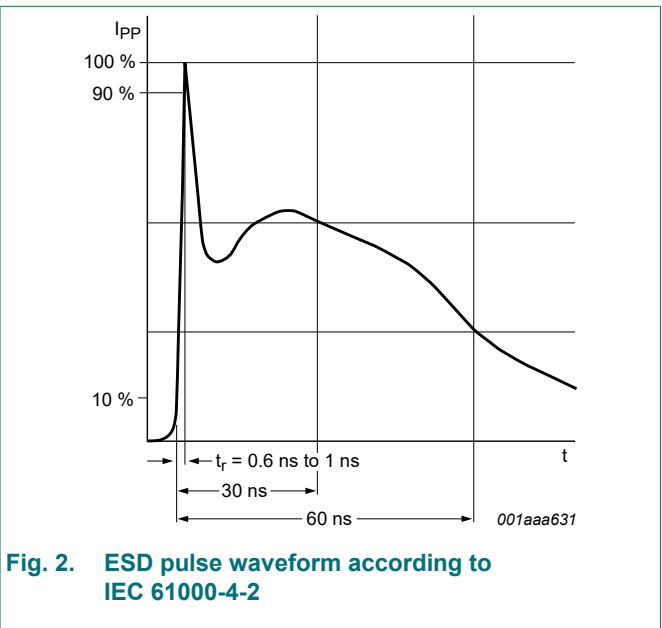
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
I_{PPM}	rated peak pulse current	$t_p = 8/20 \mu s$	[1] [2]	-	2.5	A
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
ESD maximum ratings						
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (contact discharge)	[3] [2]	-	20	kV
		ISO10605; contact discharge; C = 330 pF, R = 330 Ω	[3] [2]	-	17	kV
		ISO10605; contact discharge; C = 150 pF, R = 330 Ω	[3] [2]	-	20	kV

- [1] According to IEC 61000-4-5
- [2] Measured from pin 1 or 2 to pin 3
- [3] Device stressed with ten non-repetitive ESD pulses



9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
V_{RWM}	reverse standoff voltage	$T_{amb} = 25\text{ °C}$	-	-	27	V	
V_{BR}	breakdown voltage	$I_R = 10\text{ mA}; T_{amb} = 25\text{ °C}$	[1]	28	38	V	
I_{RM}	reverse leakage current	$V_{RWM} = 27\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	1	nA	
C_d	diode capacitance	$f = 1\text{ MHz}; V_R = 0\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	6	pF	
V_{CL}	clamping voltage	$I_{PPM} = 2.5\text{ A}; t_p = 8/20\text{ }\mu\text{s}; T_{amb} = 25\text{ °C}$	[1] [2]	-	33	44	V
		$I_{PP} = 16\text{ A}; t_p = 100\text{ ns}; T_{amb} = 25\text{ °C}$	[1] [3]	-	44	-	V

[1] Measured from pin 1 or 2 to pin 3

[2] Device stressed with 8/20 μs exponential decay waveform according to IEC 61000-4-5

[3] Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008

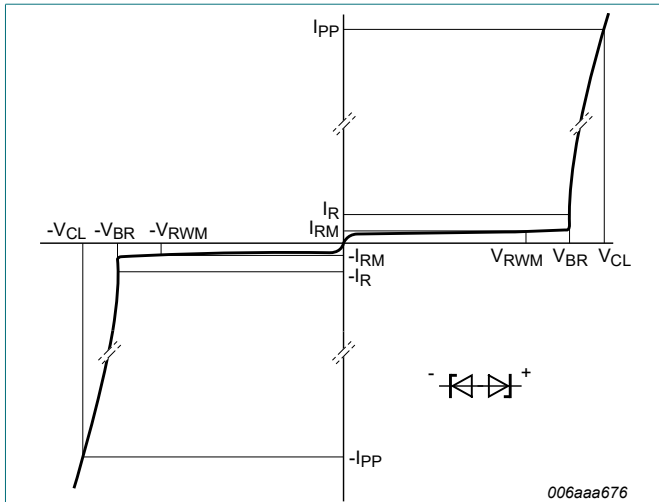


Fig. 3. V-I characteristics for a bidirectional ESD protection diode

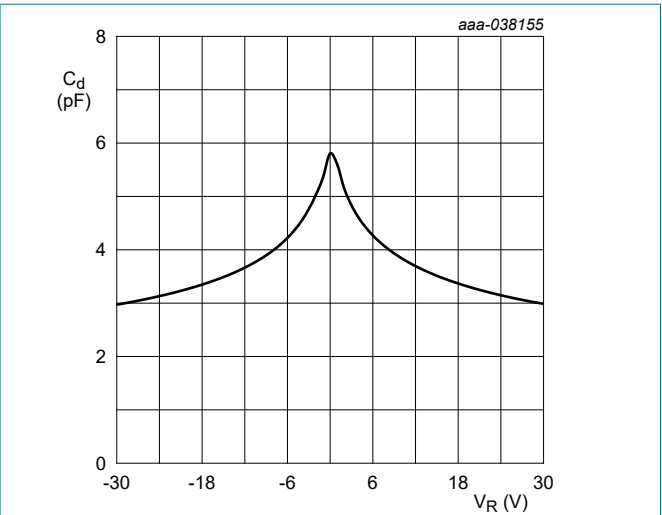
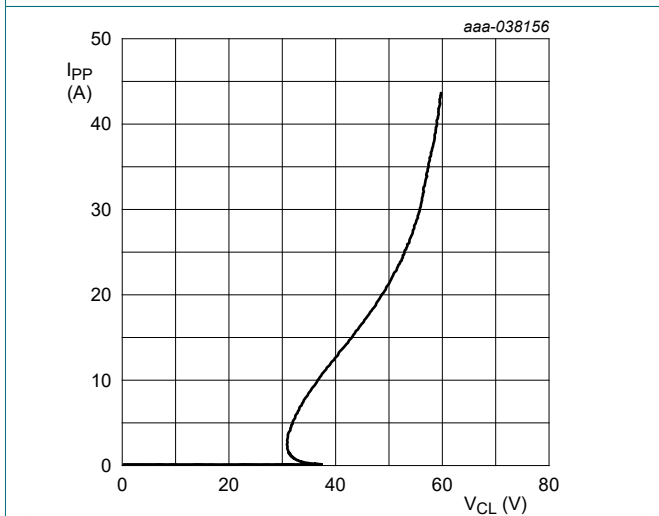
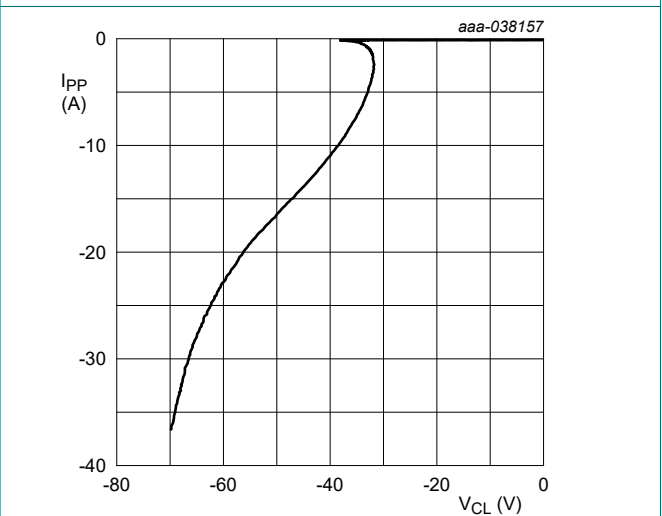


Fig. 4. Diode capacitance as a function of reverse voltage; typical values



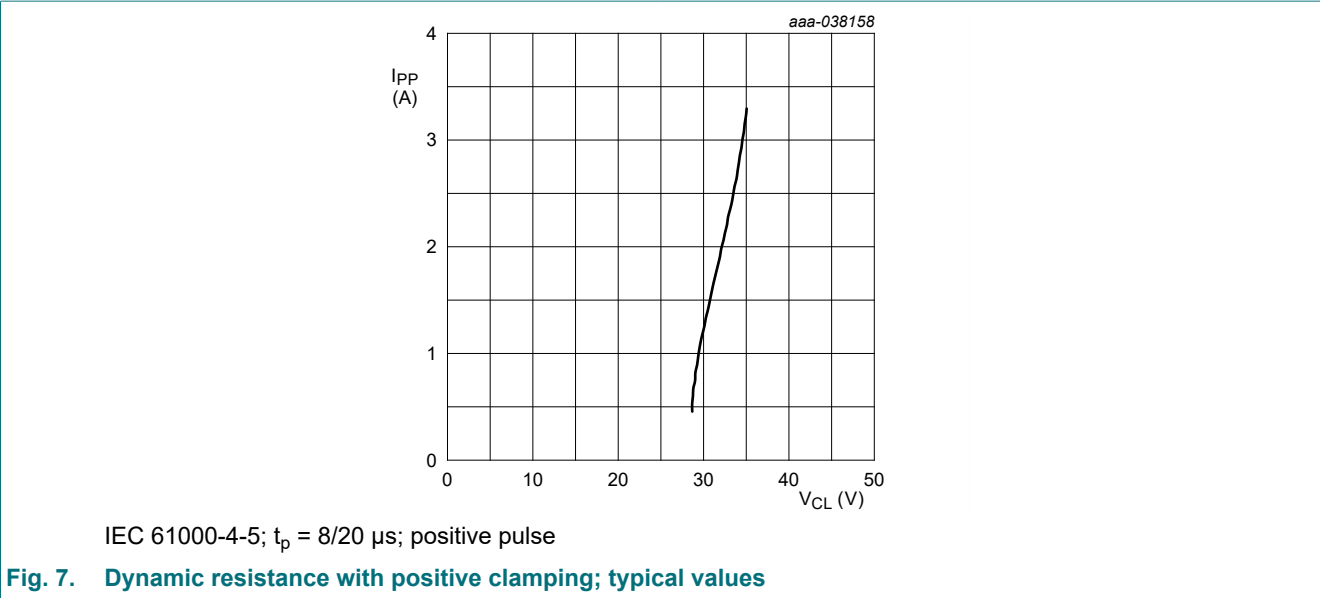
Transmission Line Pulse (TLP);
 $t_p = 100\text{ ns}$

Fig. 5. Dynamic resistance with positive clamping; typical values



Transmission Line Pulse (TLP);
 $t_p = 100\text{ ns}$

Fig. 6. Dynamic resistance with negative clamping; typical values



10. Application information

The device is designed for the protection of two lines from the damage caused by ESD and surge pulses.

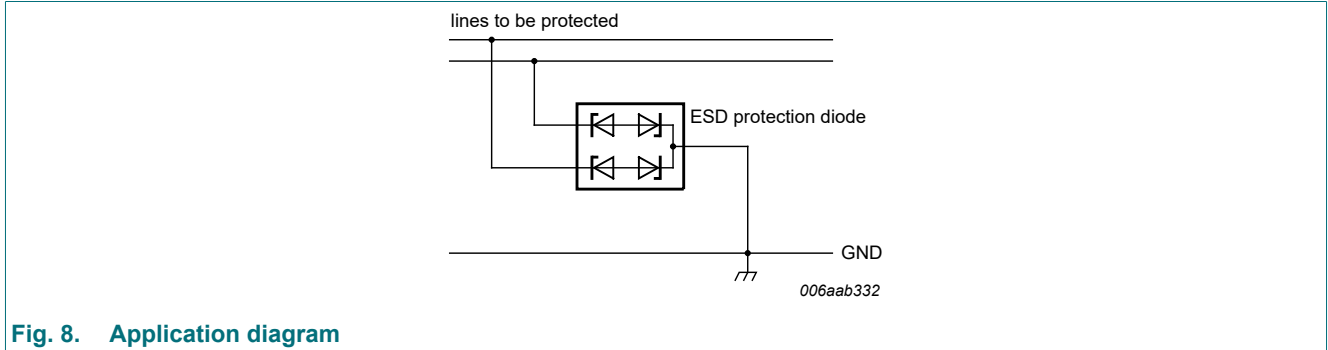


Fig. 8. Application diagram

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Test information

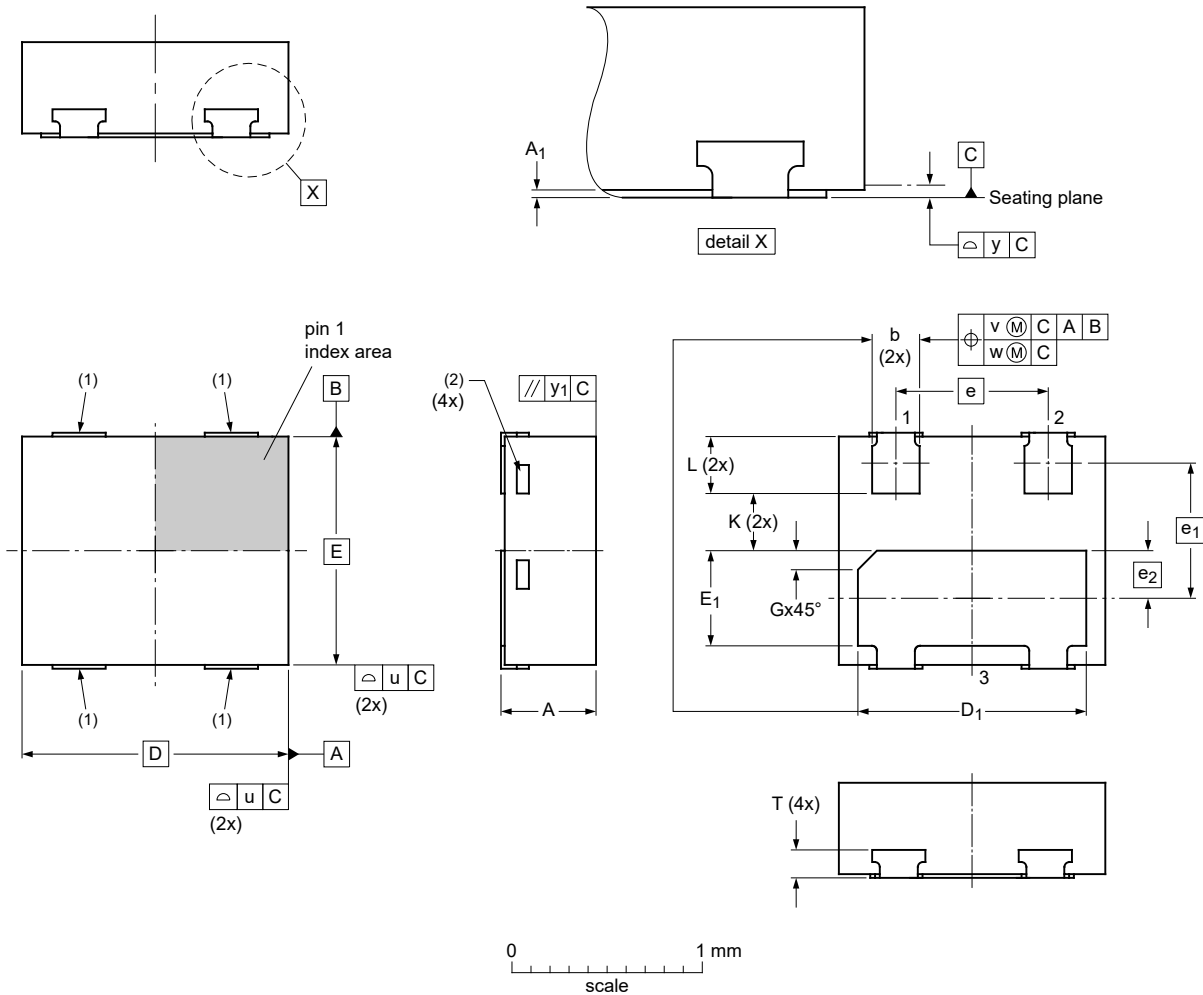
Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

DFN1412D-3: plastic, leadless ultra small outline package with side-wettable flanks (SWF); 3 terminals; 0.8 mm pitch; 1.4 mm x 1.2 mm x 0.48 mm body

SOT8009



Dimensions (mm are the original dimensions)

Unit	A	A ₁	b	D	D ₁	E	E ₁	e	e ₁	e ₂	G	K	L	T	u	v	w	y	y ₁
max	0.50	0.04	0.30	1.25	0.55								0.35	0.22					
nom	0.47		0.25	1.4	1.20	1.2	0.50	0.8	0.71	0.26	0.09		0.30	0.16	0.05	0.1	0.05	0.05	0.05
min	0.44		0.22	1.17	0.47						(ref)	0.25	0.27	0.10					

Note

- 1. Side Wettable Flank, protrusion max. 0.02 mm.
 - 2. Visible depend upon used manufacturing technology.
- Dimension A and T are including plating thickness.

sot8009_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8009		MO-340CA				19-12-06 20-12-13

Fig. 9. Package outline DFN1412D-3 (SOT8009)

13. Soldering

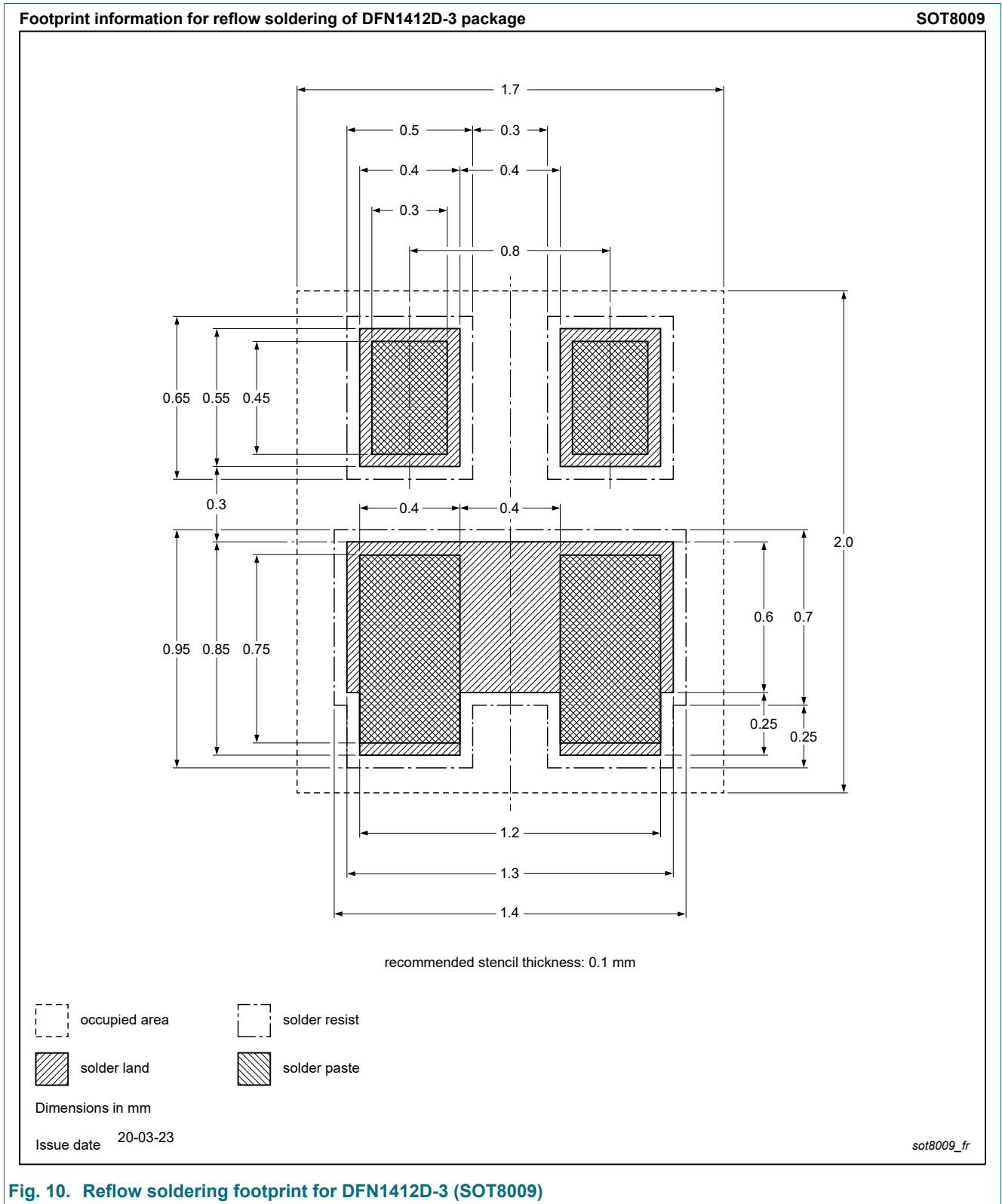


Fig. 10. Reflow soldering footprint for DFN1412D-3 (SOT8009)

14. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
MMBZ33VBQC-Q v.2	20240718	Product data sheet	-	MMBZ33VBQC-Q v.1
Modifications:	• Chapter "Characteristics": removed figures 8, 9 and 10			
MMBZ33VBQC-Q v.1	20240515	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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