

LSF0101

1-bit bidirectional multi-voltage level translator; open-drain;
push-pull

Rev. 4.1 — 25 July 2024

Product data sheet

1. General description

The LSF0101 is an 1 channel bidirectional multi-voltage level translator for open-drain and push-pull applications. It supports up to 100 MHz up translation and ≥ 100 MHz down translation at ≤ 30 pF capacitive load. There is no need for a direction pin which minimizes system effort. The LSF0101 supports 5 V tolerant I/O pins for compatibility with TTL levels in a variety of applications. The ability to set up different voltage translation levels on each channel makes the device very flexible and suitable for a lot of different applications.

2. Features and benefits

- Bidirectional voltage translation with no direction pin
- Up translation
 - ≤ 100 MHz; $C_L = 30$ pF
 - ≤ 50 MHz; $C_L = 50$ pF
- Down translation
 - ≥ 100 MHz; $C_L = 30$ pF
 - ≥ 50 MHz; $C_L = 50$ pF
- Hot insertion
- Bidirectional voltage level translation between:
 - 0.95 V and 1.8 V, 2.5 V, 3.3 V and 5.0 V
 - 1.2 V and 1.8 V, 2.5 V, 3.3 V and 5.0 V
 - 1.8 V and 2.5 V, 3.3 V and 5.0 V
 - 2.5 V and 3.3 V and 5.0 V
 - 3.3 V and 5.0 V
- Low standby current
- 5 V tolerant I/O pins to support TTL
- Low R_{ON} provides less signal distortion
- High-impedance I/O pins for $EN = Low$.
- Flow-through pinout for easy PCB trace routing.
- Latch-up performance exceeds 100 mA per JESD78 class II level A
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to $+125$ °C

3. Applications

- GPIO, MDIO, PMBus, SMBus, SDIO, UART, I²C, and other interfaces in Telecom infrastructure
- Industrial
- Personal computing

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
LSF0101GW	-40 °C to +125 °C	TSSOP6	plastic thin shrink small outline package; 6 leads; body width 1.25 mm	SOT363-2
LSF0101GM	-40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm	SOT886
LSF0101GX	-40 °C to +125 °C	X2SON6	plastic thermal enhanced extremely thin small outline package; no leads; 6 terminals; body 1.0 × 0.8 × 0.32 mm	SOT1255-2

5. Marking

Table 2. Marking

Type number	Marking code ^[1]
LSF0101GW	h1
LSF0101GM	h1
LSF0101GX	h1

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

6. Functional diagram

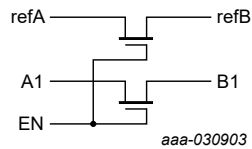
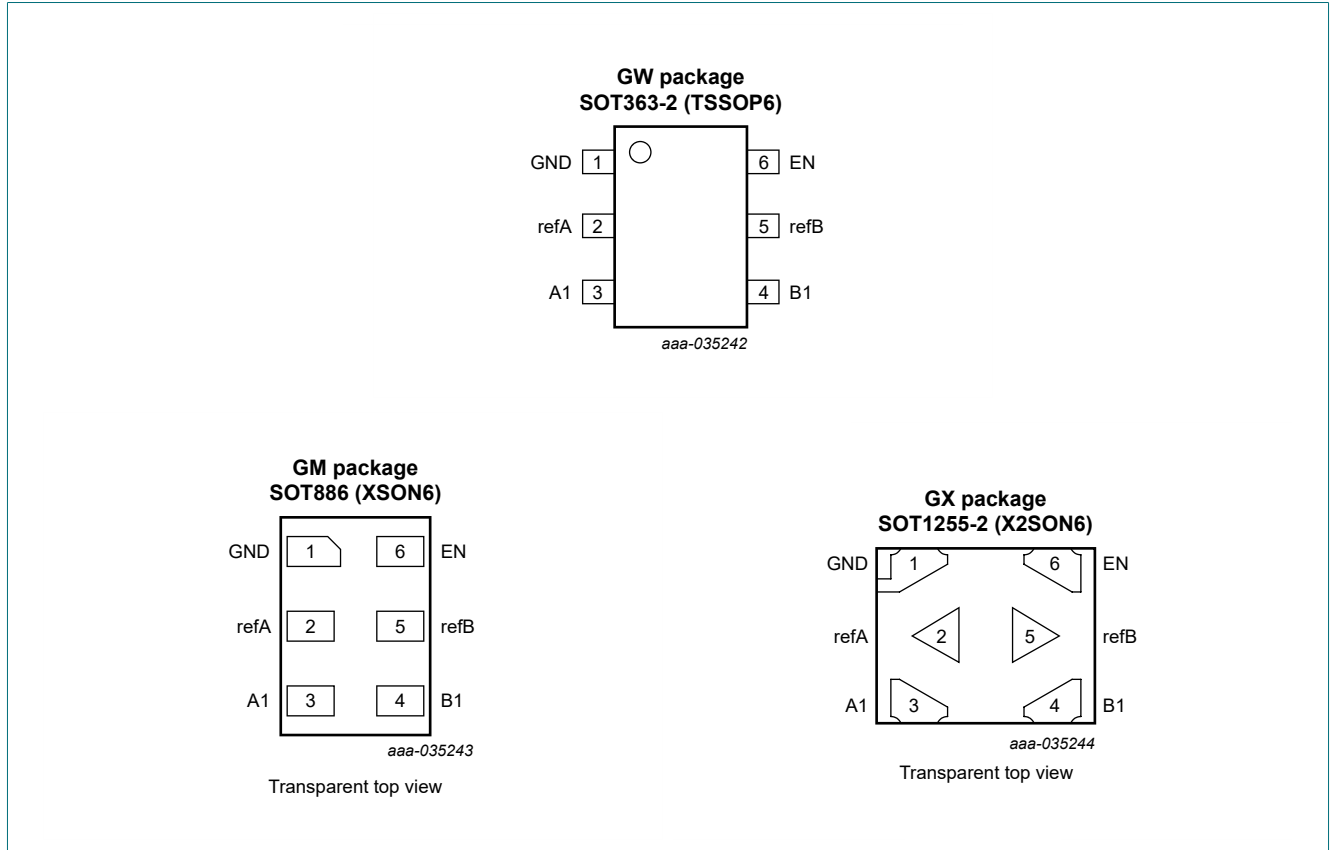


Fig. 1. Logic symbol

7. Pinning information

7.1. Pinning



7.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
GND	1	ground (0 V)
refA	2	reference voltage A
A1	3	data input/output A
B1	4	data input/output B
refB	5	reference voltage B
EN	6	enable input (active HIGH)

8. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

Input	input/output
EN	A1, B1 channel
H	A1 = B1
L	Z

9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_I	input voltage	pins refA, refB, A1, B1 and EN [1]	-0.5	+7.0	V
$I_{I/O}$	input/output current	pins refA, refB, A1 and B1; continuous channel current	-	+128	mA
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C [2]	-	250	mW

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.

[2] For SOT363-2 (TSSOP6) package: P_{tot} derates linearly with 3.7 mW/K above 83 °C.

For SOT886 (XSON6) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.

For SOT1255-2 (X2SON6) package: P_{tot} derates linearly with 3.3 mW/K above 75 °C.

10. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_I	input voltage	pins refA, refB, A1, B1 and EN	0.0	5.0	V
$I_{I/O}$	input/output current	pins refA, refB, A1 and B1; continuous channel current	-	+64	mA
T_{amb}	ambient temperature		-40	+125	°C

11. Static characteristics

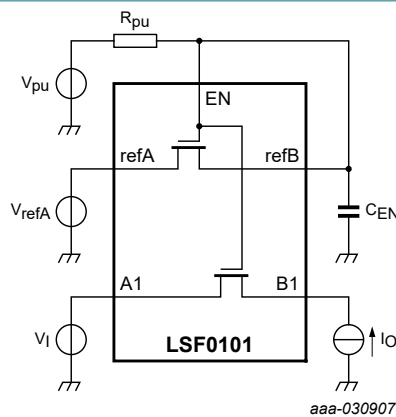
Table 7. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +125 °C			Unit
			Min	Typ[1]	Max	
V _{IK}	input clamping voltage	V _{EN} = 0 V; I _I = -18 mA	-1.2	-	-	V
I _I	leakage current	pins A1, B1, refA, refB and EN; V _I = GND to 5.0 V	-	1	5	μA
C _I	input capacitance	pins refA, refB and EN; V _I = 0 V or 3 V	-	6	-	pF
C _{io(off)}	OFF-state input/output capacitance	pins A1, B1; V _O = 0 V or 3 V; V _{EN} = 0.0 V	-	3.7	6.0	pF
C _{io(on)}	ON-state input/output capacitance	pins A1, B1; V _O = 0 V or 3 V; V _{EN} = 3.0 V	-	6.0	12.5	pF
R _{ON}	ON resistance	see Fig. 2 [2]				
		V _I = 0 V; V _{pu} = 5.0 V; I _O = 64 mA				
		V _{refA} = 3.3 V	-	3	-	Ω
		V _{refA} = 1.8 V	-	4	-	Ω
		V _{refA} = 1.0 V	-	7	-	Ω
		V _I = 0 V; V _{pu} = 5.0 V; I _O = 32 mA				
		V _{refA} = 1.8 V	-	4	-	Ω
		V _{refA} = 2.5 V	-	3	-	Ω
		V _I = 1.8 V; V _{pu} = 5.0 V; I _O = 15 mA				
		V _{refA} = 3.3 V	-	4	-	Ω
		V _I = 1.0 V; V _{pu} = 3.3 V; I _O = 10 mA				
		V _{refA} = 1.8 V	-	7	-	Ω
		V _I = 0 V; V _{pu} = 3.3 V; I _O = 10 mA				
V _{refA} = 1.0 V	-	5	-	Ω		
V _I = 0 V; V _{pu} = 1.8 V; I _O = 10 mA						
V _{refA} = 1.0 V	-	6	-	Ω		

[1] All typical values are measured at T_{amb} = 25 °C.

[2] Measured by the voltage drop between the An and Bn pins at the indicated current through the switch. ON resistance is determined by the lowest voltage of the two (An or Bn) pins.



The A1 and B1 pins may be exchanged.

R_{pu} = 200 kΩ; C_{EN} = 100 nF

Fig. 2. Test circuit for measuring R_{ON}

12. Dynamic characteristics

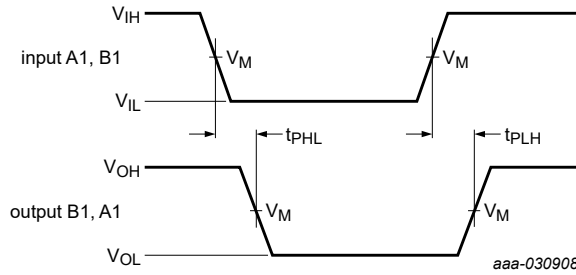
Table 8. Switching characteristics

$GND = 0\text{ V}$; for waveform see [Fig. 3](#); for test circuit see [Fig. 4](#)

Symbol	Parameter	Conditions	$T_{amb} = -40\text{ °C to }+125\text{ °C}$			Unit
			Min	Typ[1]	Max	
Translating down						
t_{PLH}	LOW to HIGH propagation delay	A1 to B1 or B1 to A1; $V_{IH} = V_{pu} = V_{refA} + 1\text{ V}$				
		$V_{refA} = 1.5\text{ V}; C_L = 15\text{ pF}$	-	0.35	-	ns
		$V_{refA} = 1.5\text{ V}; C_L = 30\text{ pF}$	-	0.8	-	ns
		$V_{refA} = 1.5\text{ V}; C_L = 50\text{ pF}$	-	1.2	-	ns
		$V_{refA} = 2.3\text{ V}; C_L = 15\text{ pF}$	-	0.3	-	ns
		$V_{refA} = 2.3\text{ V}; C_L = 30\text{ pF}$	-	0.7	-	ns
		$V_{refA} = 2.3\text{ V}; C_L = 50\text{ pF}$	-	1.1	-	ns
t_{PHL}	HIGH to LOW propagation delay	A1 to B1 or B1 to A1; $V_{IH} = V_{pu} = V_{refA} + 1\text{ V}$				
		$V_{refA} = 1.5\text{ V}; C_L = 15\text{ pF}$	-	0.5	-	ns
		$V_{refA} = 1.5\text{ V}; C_L = 30\text{ pF}$	-	1.0	-	ns
		$V_{refA} = 1.5\text{ V}; C_L = 50\text{ pF}$	-	1.3	-	ns
		$V_{refA} = 2.3\text{ V}; C_L = 15\text{ pF}$	-	0.4	-	ns
		$V_{refA} = 2.3\text{ V}; C_L = 30\text{ pF}$	-	0.8	-	ns
		$V_{refA} = 2.3\text{ V}; C_L = 50\text{ pF}$	-	1.2	-	ns
Translating up						
t_{PLH}	LOW to HIGH propagation delay	A1 to B1 or B1 to A1; $V_{IH} = V_{refA}; V_{EXT} = V_{pu} = V_{refA} + 1\text{ V}$				
		$V_{refA} = 1.5\text{ V}; C_L = 15\text{ pF}$	-	0.5	-	ns
		$V_{refA} = 1.5\text{ V}; C_L = 30\text{ pF}$	-	0.9	-	ns
		$V_{refA} = 1.5\text{ V}; C_L = 50\text{ pF}$	-	1.1	-	ns
		$V_{refA} = 2.3\text{ V}; C_L = 15\text{ pF}$	-	0.4	-	ns
		$V_{refA} = 2.3\text{ V}; C_L = 30\text{ pF}$	-	0.8	-	ns
		$V_{refA} = 2.3\text{ V}; C_L = 50\text{ pF}$	-	1.0	-	ns
t_{PHL}	HIGH to LOW propagation delay	A1 to B1 or B1 to A1; $V_{IH} = V_{refA}; V_{EXT} = V_{pu} = V_{refA} + 1\text{ V}$				
		$V_{refA} = 1.5\text{ V}; C_L = 15\text{ pF}$	-	0.6	-	ns
		$V_{refA} = 1.5\text{ V}; C_L = 30\text{ pF}$	-	1.1	-	ns
		$V_{refA} = 1.5\text{ V}; C_L = 50\text{ pF}$	-	1.3	-	ns
		$V_{refA} = 2.3\text{ V}; C_L = 15\text{ pF}$	-	0.4	-	ns
		$V_{refA} = 2.3\text{ V}; C_L = 30\text{ pF}$	-	0.9	-	ns
		$V_{refA} = 2.3\text{ V}; C_L = 50\text{ pF}$	-	1.0	-	ns

[1] All typical values are measured at $T_{amb} = 25\text{ °C}$.

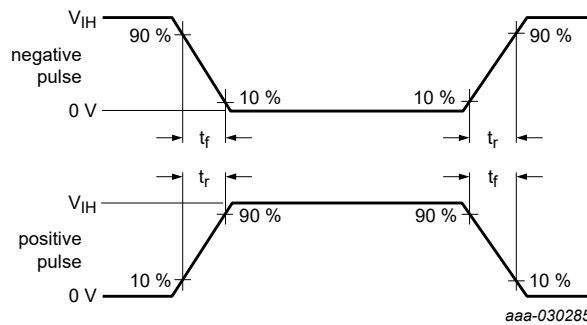
12.1. Waveforms and test circuit



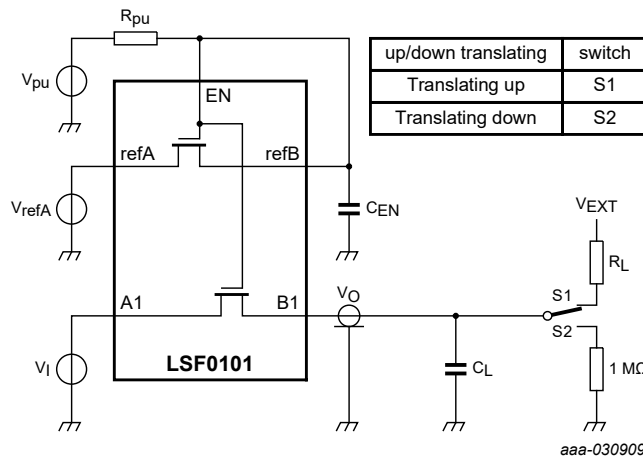
Measurement points are given in [Table 9](#).

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 3. The data input (A1, B1) to output (B1, A1) propagation delay times



a. V_I source waveform



b. Test circuit

Test data is given in [Table 9](#).

The A1 and B1 pins may be exchanged.

All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz; $Z_O = 50 \Omega$.

Definitions test circuit:

C_L = Load capacitance including jig and probe capacitance;

C_{EN} = Decoupling capacitance;

R_{pu} = Pull-up resistance;

R_L = Load resistance;

S1/S2 = Test selection switch.

Fig. 4. Test circuit for measuring switching times

1-bit bidirectional multi-voltage level translator; open-drain; push-pull

Table 9. Test data

Input		Output	Load			
t_r, t_f	V_M	V_M	C_L	C_{EN} [1]	R_L [1]	R_{pu}
≤ 2 ns	$0.5 \times V_{refA}$	$0.5 \times V_{refA}$	15 pF, 30 pF, 50 pF	100 nF	300 Ω	200 k Ω

[1] All typical values are measured at $T_{amb} = 25$ °C.

13. Package outline

TSSOP6: plastic thin shrink small outline package; 6 leads; body width 1.25 mm

SOT363-2



Fig. 5. Package outline SOT363-2 (TSSOP6)

1-bit bidirectional multi-voltage level translator; open-drain; push-pull

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm

SOT886



Fig. 6. Package outline SOT886 (XSON6)

1-bit bidirectional multi-voltage level translator; open-drain; push-pull

X2SON6: plastic thermal enhanced extremely thin small outline package; no leads; 6 terminals; body 1.0 x 0.8 x 0.32 mm

SOT1255-2

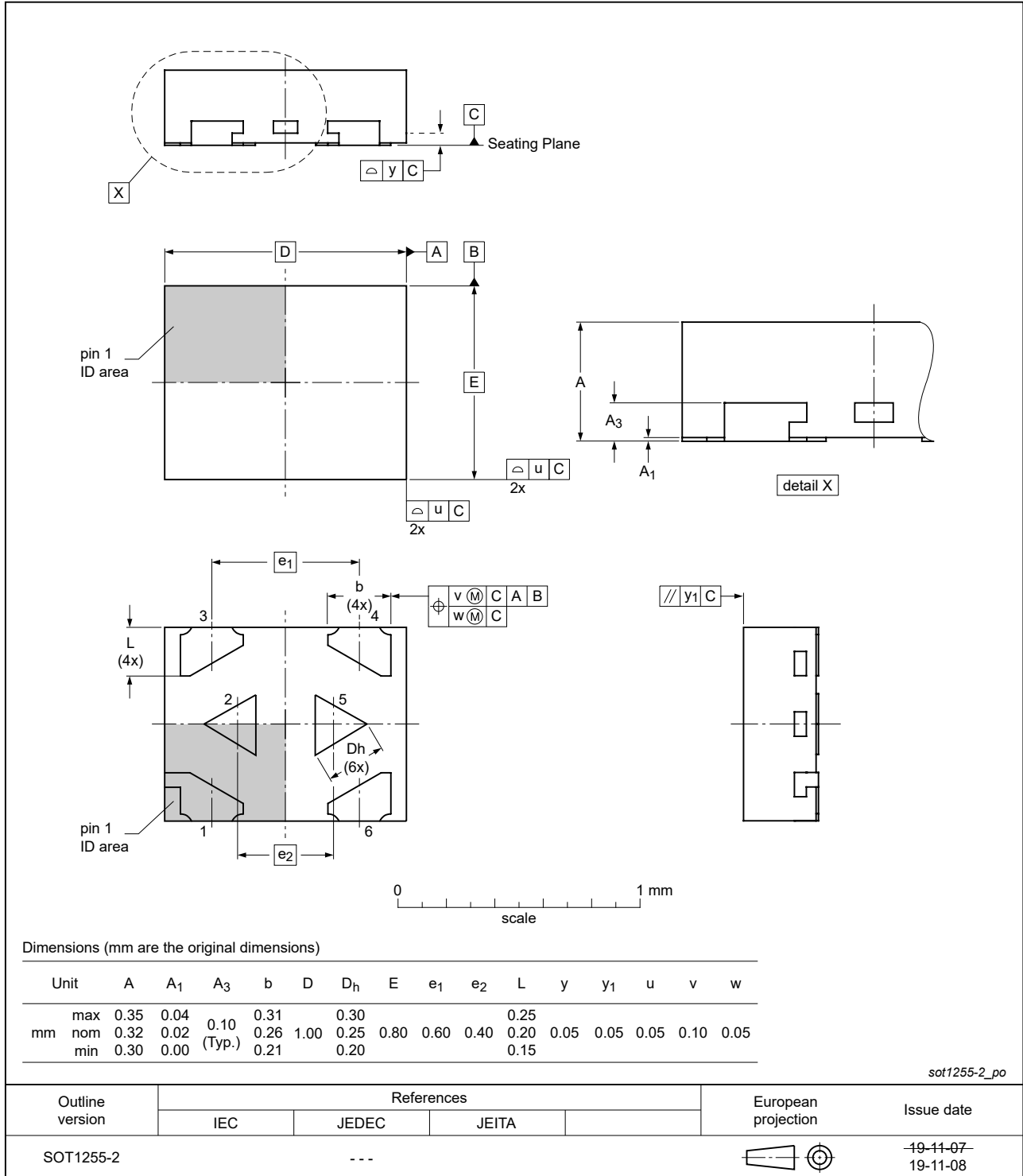


Fig. 7. Package outline SOT1255-2 (X2SON6)

14. Abbreviations

Table 10. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
PCB	Printed Circuit Board
PRR	Pulse Rate Repetition
TTL	Transistor-Transistor Logic

15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LSF0101 v.4.1	20240725	Product data sheet	-	LSF0101 v.4
LSF0101 v.4	20231127	Product data sheet	-	LSF0101 v.3
Modifications:	<ul style="list-style-type: none"> Section 2: up- and down-translation typo corrected. 			
LSF0101 v.3	20220208	Product data sheet	-	LSF0101 v.2
Modifications:	<ul style="list-style-type: none"> Package SOT363 (SC-88) changed to SOT363-2 (TSSOP6). 			
LSF0101 v.2	20200923	Product data sheet	-	LSF0101 v.1.1
Modifications:	<ul style="list-style-type: none"> Type number LSF0101GW (SOT363/SC-88) added. 			
LSF0101 v.1.1	20200626	Product data sheet	-	LSF0101 v.1
Modifications:	<ul style="list-style-type: none"> Type number LSF0101GW (SOT363/SC-88) is in development and removed from this product data sheet. Preliminary data sheet is available upon request. 			
LSF0101 v.1	20200414	Product data sheet	-	-

16. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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