

# HEF4069UB-Q100

Hex unbuffered inverter

Rev. 4 — 5 September 2024

Product data sheet

## 1. General description

The HEF4069UB-Q100 is a hex unbuffered inverter. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of  $V_{DD}$ .

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 3.0 V to 15.0 V
- CMOS low power dissipation
- High noise immunity
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Complies with JEDEC standard JESD 13-B
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

## 3. Applications

- Oscillator

## 4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
<a href="#">HEF4069UBT-Q100</a>	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	<a href="#">SOT108-1</a>
<a href="#">HEF4069UBTT-Q100</a>	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	<a href="#">SOT402-1</a>

## 5. Functional diagram

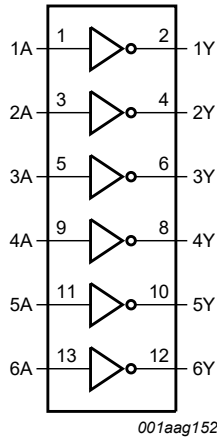


Fig. 1. Functional diagram

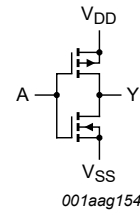


Fig. 2. Schematic diagram (one inverter)

## 6. Pinning information

### 6.1. Pinning

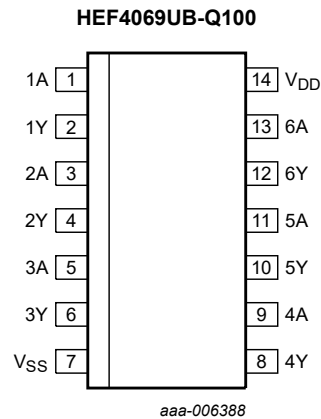


Fig. 3. Pin configuration

### 6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A, 5A, 6A	1, 3, 5, 9, 11, 13	input
1Y, 2Y, 3Y, 4Y, 5Y, 6Y	2, 4, 6, 8, 10, 12	output
V <sub>SS</sub>	7	ground (0 V)
V <sub>DD</sub>	14	supply voltage

## 7. Limiting values

**Table 3. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD}$	supply voltage		-0.5	+18	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{DD} + 0.5\text{ V}$	-	$\pm 10$	mA
$V_I$	input voltage		-0.5	$V_{DD} + 0.5$	V
$I_{OK}$	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{DD} + 0.5\text{ V}$	-	$\pm 10$	mA
$I_{I/O}$	input/output current		-	$\pm 10$	mA
$I_{DD}$	supply current		-	50	mA
$T_{stg}$	storage temperature		-65	+150	°C
$T_{amb}$	ambient temperature		-40	+125	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$ [1]	-	500	mW
$P$	power dissipation	per output	-	100	mW

[1] For SOT108-1 (SO14) package:  $P_{tot}$  derates linearly with 10.1 mW/K above 100 °C.  
For SOT402-1 (TSSOP14) package:  $P_{tot}$  derates linearly with 7.3 mW/K above 81 °C.

## 8. Recommended operating conditions

**Table 4. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD}$	supply voltage		3	-	15	V
$V_I$	input voltage		0	-	$V_{DD}$	V
$T_{amb}$	ambient temperature	in free air	-40	-	+125	°C

## 9. Static characteristics

**Table 5. Static characteristics**

$V_{SS} = 0\text{ V}$ ;  $V_I = V_{SS}$  or  $V_{DD}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	$T_{amb} = -40\text{ °C}$		$T_{amb} = +25\text{ °C}$		$T_{amb} = +85\text{ °C}$		$T_{amb} = +125\text{ °C}$		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	4	-	4	-	4	-	4	-	V
			10 V	8	-	8	-	8	-	8	-	V
			15 V	12.5	-	12.5	-	12.5	-	12.5	-	V
$V_{IL}$	LOW-level input voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	-	1	-	1	-	1	-	1	V
			10 V	-	2	-	2	-	2	-	2	V
			15 V	-	2.5	-	2.5	-	2.5	-	2.5	V
$V_{OH}$	HIGH-level output voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	4.95	-	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	14.95	-	V
$V_{OL}$	LOW-level output voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	-	0.05	V

Symbol	Parameter	Conditions	V <sub>DD</sub>	T <sub>amb</sub> = -40 °C		T <sub>amb</sub> = +25 °C		T <sub>amb</sub> = +85 °C		T <sub>amb</sub> = +125 °C		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
I <sub>OH</sub>	HIGH-level output current	V <sub>O</sub> = 2.5 V	5 V	-	-1.7	-	-1.4	-	-1.1	-	-1.1	mA
		V <sub>O</sub> = 4.6 V	5 V	-	-0.64	-	-0.5	-	-0.36	-	-0.36	mA
		V <sub>O</sub> = 9.5 V	10 V	-	-1.6	-	-1.3	-	-0.9	-	-0.9	mA
		V <sub>O</sub> = 13.5 V	15 V	-	-4.2	-	-3.4	-	-2.4	-	-2.4	mA
I <sub>OL</sub>	LOW-level output current	V <sub>O</sub> = 0.4 V	5 V	0.64	-	0.5	-	0.36	-	0.36	-	mA
		V <sub>O</sub> = 0.5 V	10 V	1.6	-	1.3	-	0.9	-	0.9	-	mA
		V <sub>O</sub> = 1.5 V	15 V	4.2	-	3.4	-	2.4	-	2.4	-	mA
I <sub>I</sub>	input leakage current		15 V	-	±0.1	-	±0.1	-	±1.0	-	±1.0	µA
I <sub>DD</sub>	supply current	all valid input combinations; I <sub>O</sub> = 0 A	5 V	-	0.25	-	0.25	-	7.5	-	7.5	µA
			10 V	-	0.5	-	0.5	-	15.0	-	15.0	µA
			15 V	-	1.0	-	1.0	-	30.0	-	30.0	µA
C <sub>I</sub>	input capacitance	digital inputs		-	-	-	7.5	-	-	-	pF	

## 10. Dynamic characteristics

**Table 6. Dynamic characteristics**

T<sub>amb</sub> = 25 °C; for waveforms see Fig. 4; for test circuit see Fig. 5.

Symbol	Parameter	Conditions	V <sub>DD</sub>	Extrapolation formula [1]	Min	Typ	Max	Unit
t <sub>PHL</sub>	HIGH to LOW propagation delay	nA to nY	5 V	18 ns + (0.55 ns/pF)C <sub>L</sub>	-	45	90	ns
			10 V	9 ns + (0.23 ns/pF)C <sub>L</sub>	-	20	40	ns
			15 V	7 ns + (0.16 ns/pF)C <sub>L</sub>	-	15	25	ns
t <sub>PLH</sub>	LOW to HIGH propagation delay	nA to nY	5 V	13 ns + (0.55 ns/pF)C <sub>L</sub>	-	40	80	ns
			10 V	9 ns + (0.23 ns/pF)C <sub>L</sub>	-	20	40	ns
			15 V	7 ns + (0.16 ns/pF)C <sub>L</sub>	-	15	30	ns
t <sub>THL</sub>	HIGH to LOW output transition time	output nY	5 V	10 ns + (1.00 ns/pF)C <sub>L</sub>	-	60	120	ns
			10 V	9 ns + (0.42 ns/pF)C <sub>L</sub>	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF)C <sub>L</sub>	-	20	40	ns
t <sub>TLH</sub>	LOW to HIGH output transition time	output nY	5 V	10 ns + (1.00 ns/pF)C <sub>L</sub>	-	60	120	ns
			10 V	9 ns + (0.42 ns/pF)C <sub>L</sub>	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF)C <sub>L</sub>	-	20	40	ns

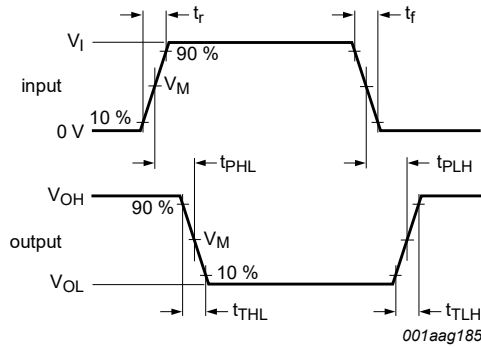
[1] The typical value of the propagation delay and output transition time can be calculated with the extrapolation formula (C<sub>L</sub> in pF).

**Table 7. Dynamic power dissipation**

V<sub>SS</sub> = 0 V; t<sub>r</sub> = t<sub>f</sub> ≤ 20 ns; T<sub>amb</sub> = 25 °C.

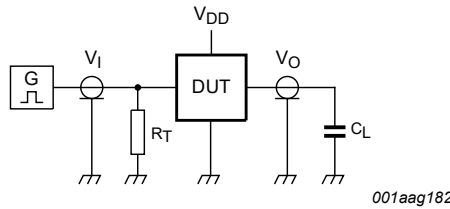
Symbol	Parameter	V <sub>DD</sub>	Typical formula	Where
P <sub>D</sub>	dynamic power dissipation	5 V	P <sub>D</sub> = 600 × f <sub>i</sub> + Σ(f <sub>o</sub> × C <sub>L</sub> ) × V <sub>DD</sub> <sup>2</sup> (µW)	f <sub>i</sub> = input frequency in MHz; f <sub>o</sub> = output frequency in MHz; C <sub>L</sub> = output load capacitance in pF; Σ(f <sub>o</sub> × C <sub>L</sub> ) = sum of the outputs; V <sub>DD</sub> = supply voltage in V.
		10 V	P <sub>D</sub> = 4000 × f <sub>i</sub> + Σ(f <sub>o</sub> × C <sub>L</sub> ) × V <sub>DD</sub> <sup>2</sup> (µW)	
		15 V	P <sub>D</sub> = 22000 × f <sub>i</sub> + Σ(f <sub>o</sub> × C <sub>L</sub> ) × V <sub>DD</sub> <sup>2</sup> (µW)	

10.1. Waveforms and test circuit



Measurement points:  $V_M = 0.5V_{DD}$ .  
 Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

Fig. 4. Propagation delay and transition times



For test data refer to [Table 8](#).  
 Definitions test circuit:  
 $C_L$  = load capacitance including jig and probe capacitance;  
 $R_T$  = termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.

Fig. 5. Test circuit for measuring switching times

Table 8. Test data

Supply voltage	Input	Load
$V_{DD}$	$V_I$	$C_L$
5 V to 15 V	$V_{SS}$ or $V_{DD}$	50 pF

10.2. Transfer characteristics

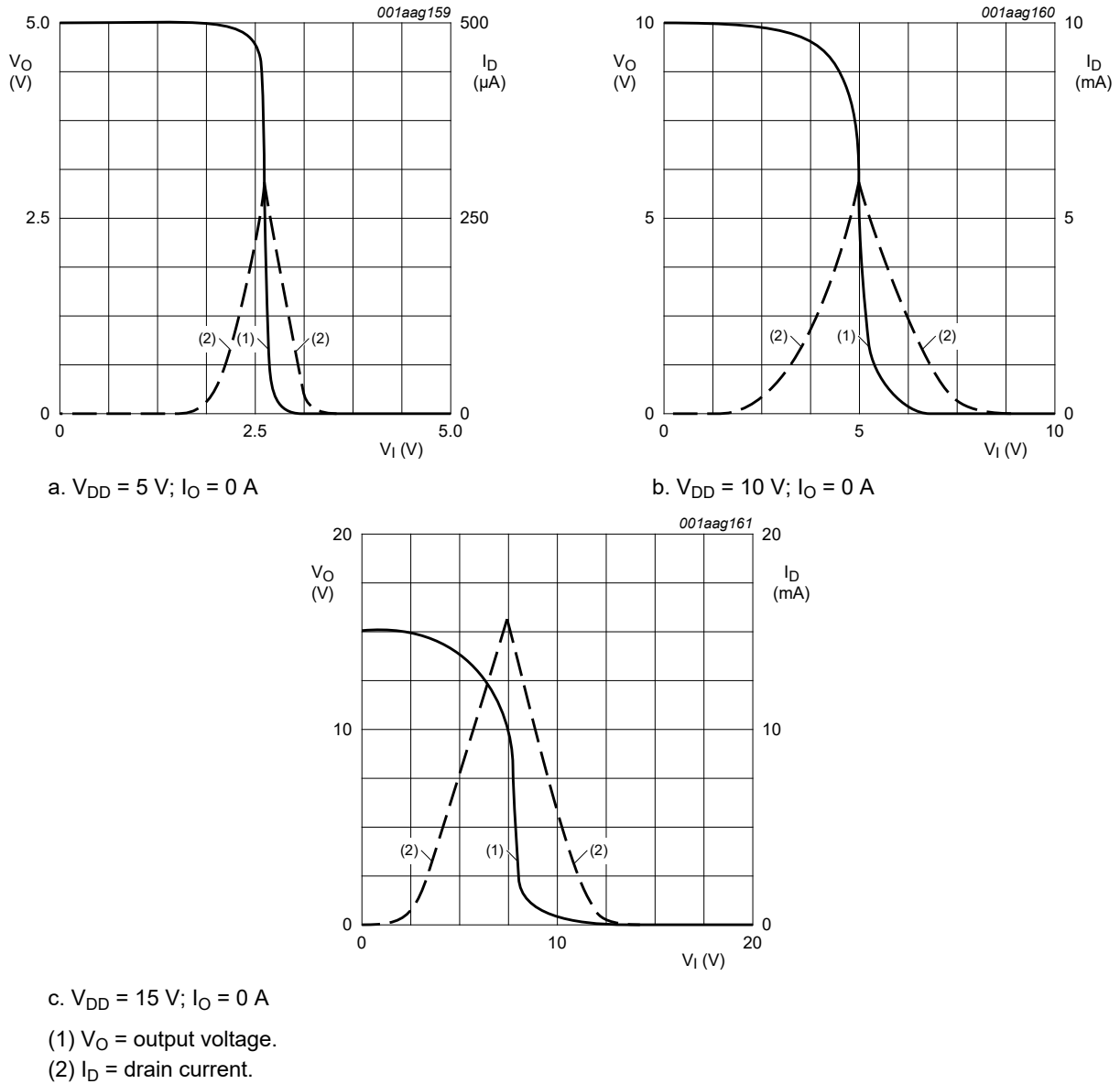


Fig. 6. Typical transfer characteristics

## 11. Application information

Some examples of applications for HEF4069UB-Q100.

Fig. 7 shows an astable relaxation oscillator using two HEF4069UB-Q100 inverters and two BAW62 diodes. The oscillation frequency is mainly determined by  $R1 \times C1$ , provided  $R1 \ll R2$  and  $R2 \times C2 \ll R1 \times C1$ .

The function of  $R2$  is to minimize the influence of the forward voltage across the protection diodes on the frequency;  $C2$  is a stray (parasitic) capacitance.

The period  $T_p$  is given by  $T_p = T_1 + T_2$ ,

where:

$$T_1 = R1C1 \ln \frac{V_{DD} + V_{ST}}{V_{ST}}$$

$$T_2 = R1C1 \ln \frac{2V_{DD} - V_{ST}}{V_{DD} - V_{ST}}$$

$V_{ST}$  = the signal threshold level of the inverter.

The period is fairly independent of  $V_{DD}$ ,  $V_{ST}$  and temperature. The duty factor, however, is influenced by  $V_{ST}$ .

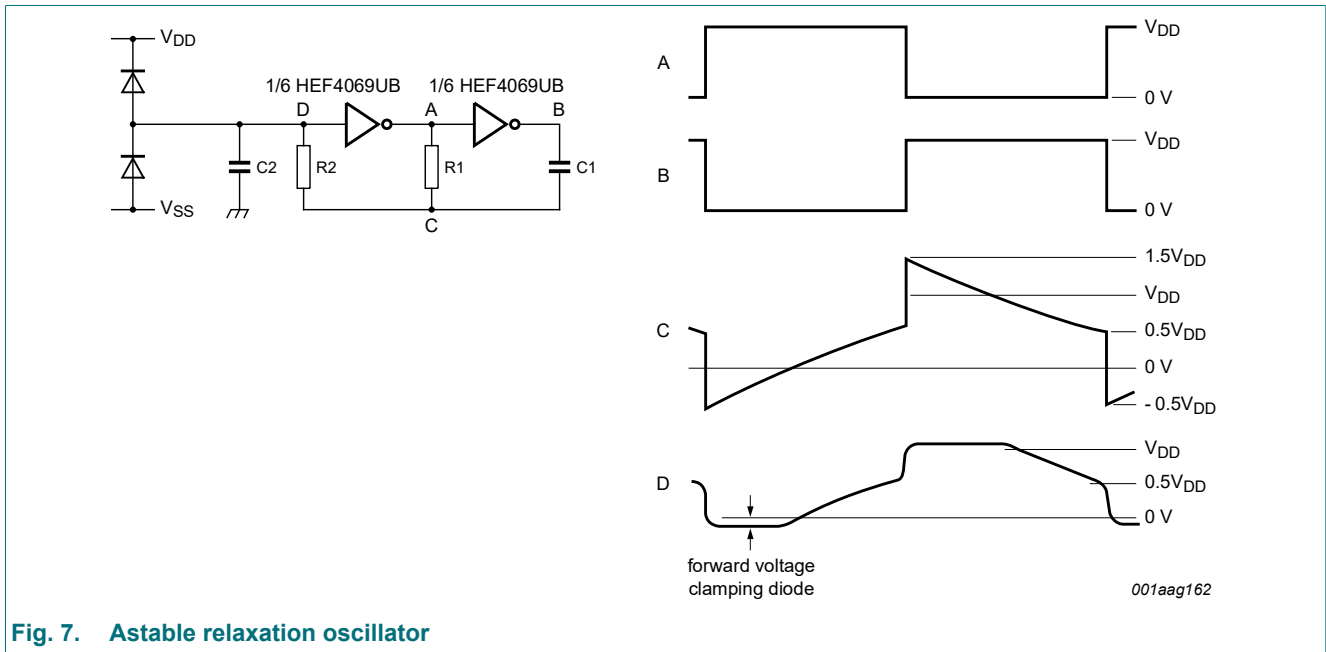


Fig. 8 shows a crystal oscillator for frequencies up to 10 MHz using two HEF4069UB-Q100 inverters. The second inverter amplifies the oscillator output voltage to a level sufficient to drive other Local Oxidation CMOS (LOCMOS) circuits.

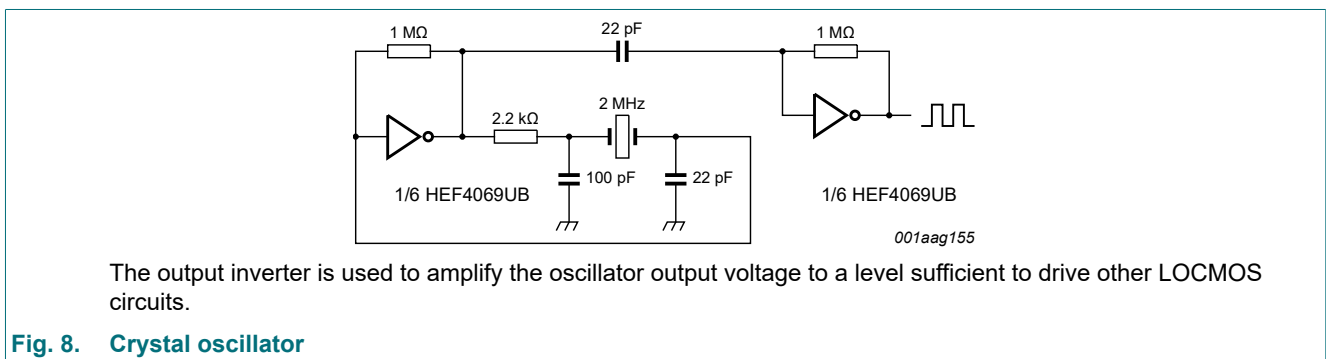


Fig. 9 and Fig. 10 show voltage gain and supply current. Fig. 11 shows the test set-up and an example of an analog amplifier using one HEF4069UB-Q100.

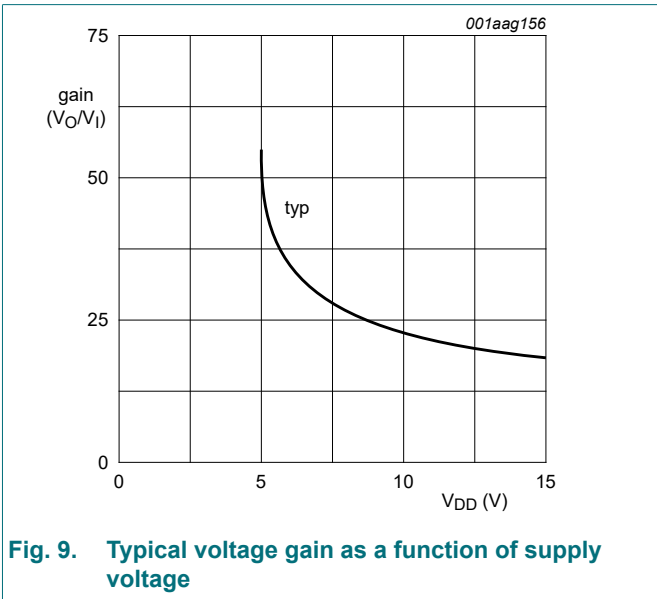


Fig. 9. Typical voltage gain as a function of supply voltage

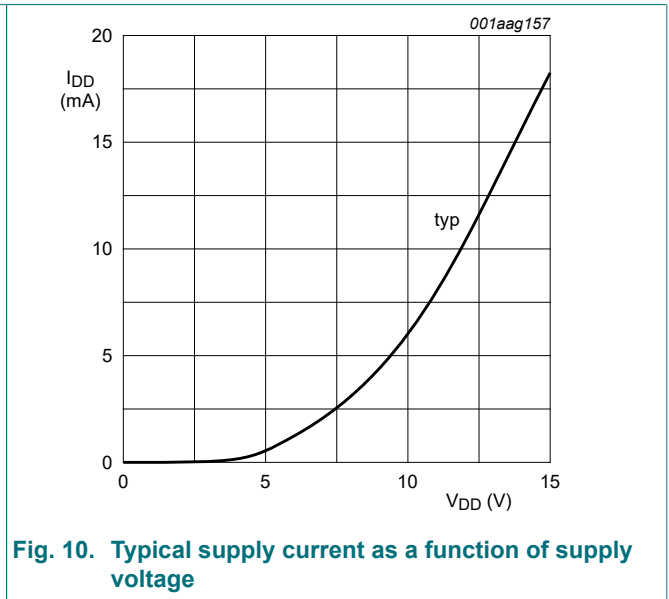


Fig. 10. Typical supply current as a function of supply voltage

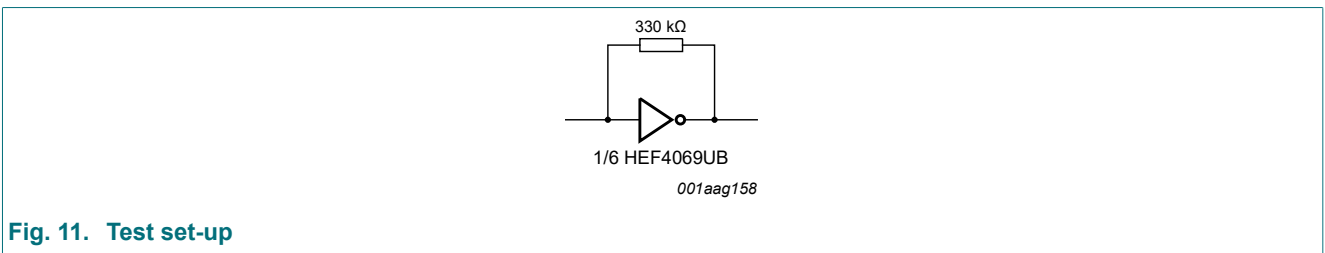


Fig. 11. Test set-up

Fig. 12 shows typical forward transconductance. Fig. 13 shows the test set-up.

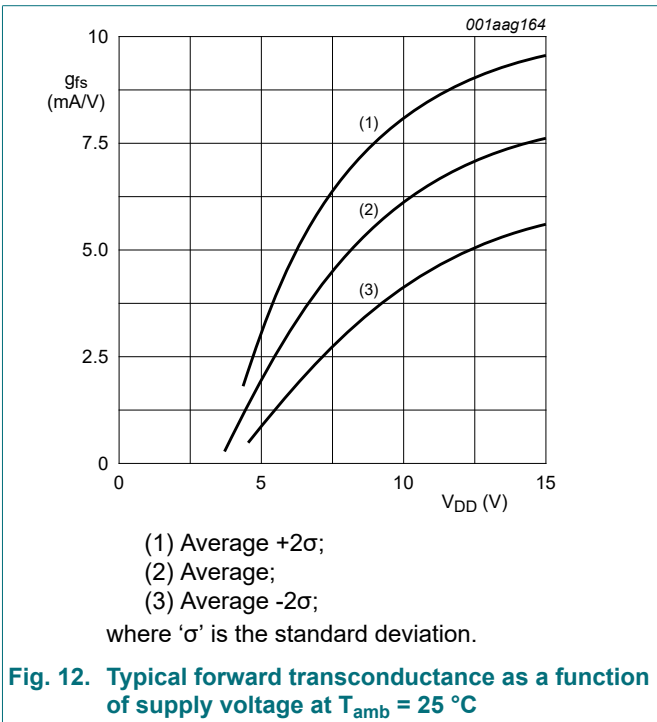


Fig. 12. Typical forward transconductance as a function of supply voltage at T<sub>amb</sub> = 25 °C

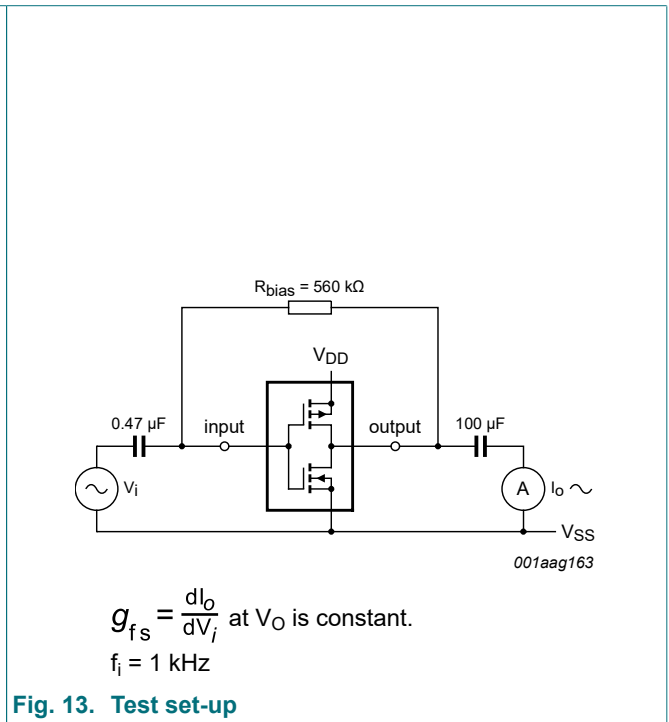


Fig. 13. Test set-up



## 12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

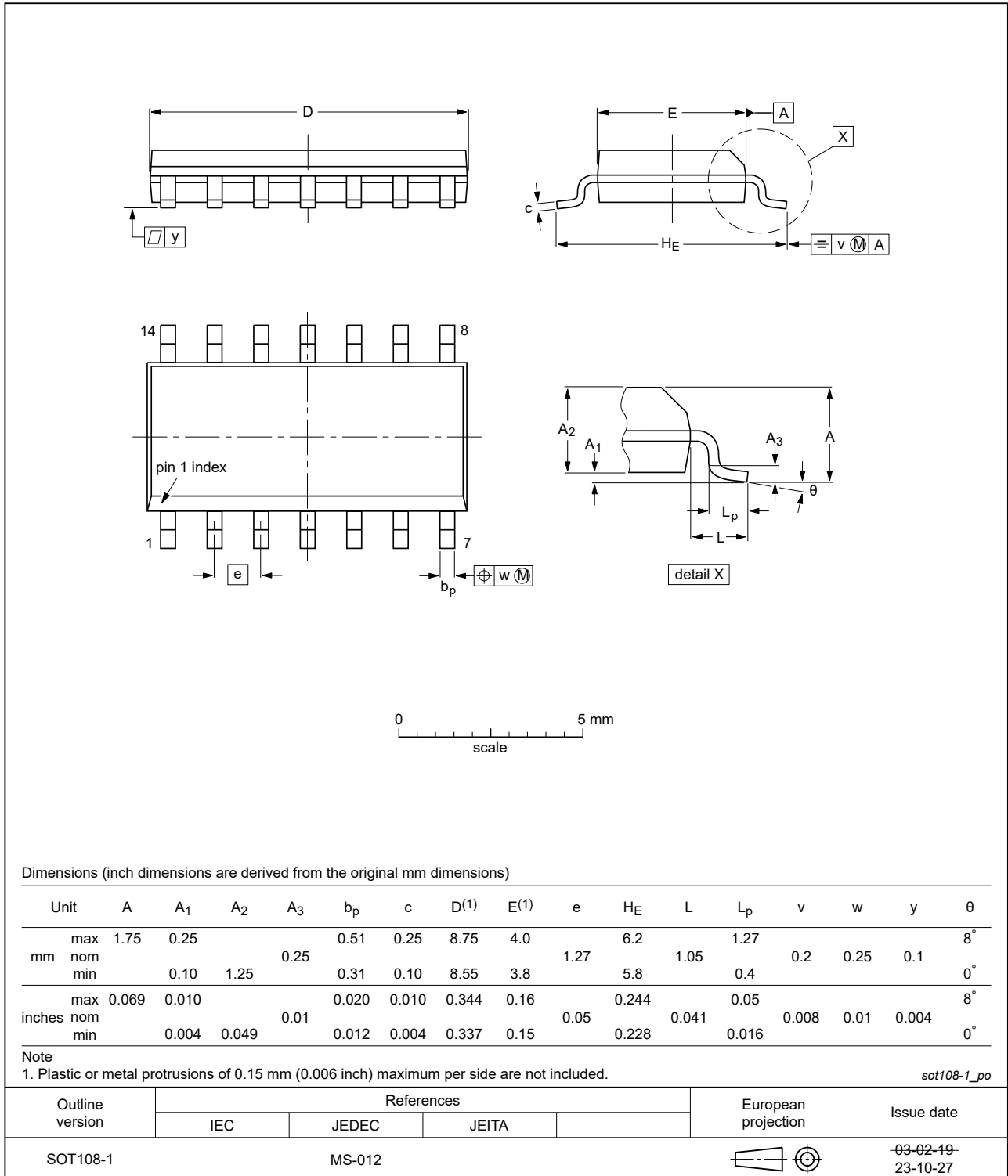


Fig. 14. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

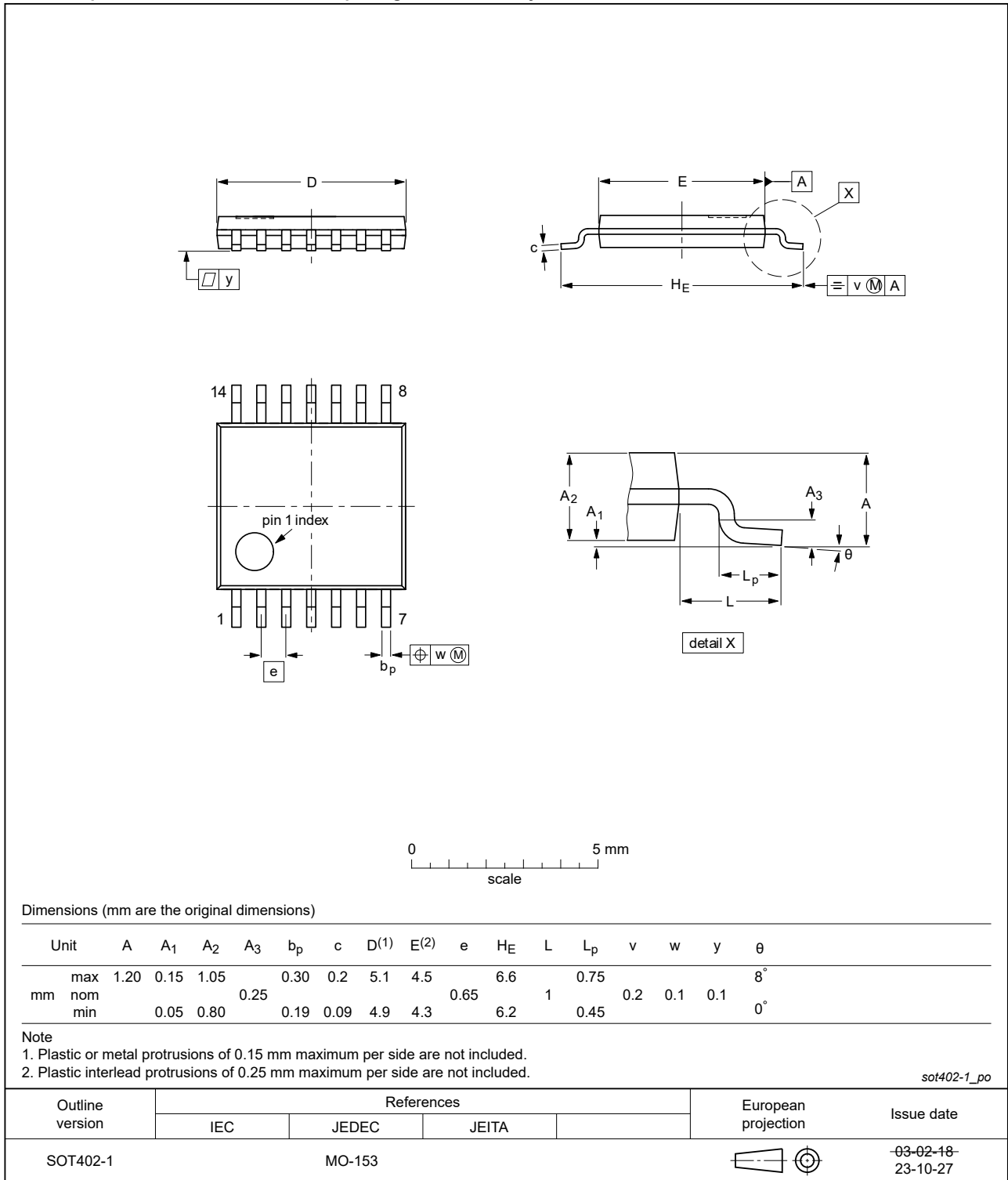


Fig. 15. Package outline SOT402-1 (TSSOP14)

## 13. Abbreviations

Table 9. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
LOCOS	Local Oxidation Complementary Metal-Oxide Semiconductor

## 14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4069UB_Q100 v.4	20240905	Product data sheet	-	HEF4069UB_Q100 v.3
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Section 2</a>: ESD specification updated according to the latest JEDEC standard.</li> <li><a href="#">Fig. 14</a>, <a href="#">Fig. 15</a>: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153</li> </ul>			
HEF4069UB_Q100 v.3	20220106	Product data sheet	-	HEF4069UB_Q100 v.2
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Section 1</a> and <a href="#">Section 2</a> updated.</li> <li><a href="#">Table 3</a>: Derating values for <math>P_{tot}</math> total power dissipation updated.</li> </ul>			
HEF4069UB_Q100 v.2	20140909	Product data sheet	-	HEF4069UB_Q100 v.1
Modifications:	<ul style="list-style-type: none"> <li>: ESD protection: MIL-STD-833 changed to MIL-STD883</li> </ul>			
HEF4069UB_Q100 v.1	20130228	Product data sheet	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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Date of release: 5 September 2024

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