

# HEF4067B

## 16-channel analog multiplexer/demultiplexer

Rev. 10 — 7 November 2023

Product data sheet

### 1. General description

The HEF4067B is a single-pole 16-throw analog switch (SP16T) suitable for use in analog or digital 16:1 multiplexer/demultiplexer applications. The switch features four digital select inputs (A0, A1, A2 and A3), sixteen independent inputs/outputs (Yn), a common input/output (Z) and a digital enable input (E). When E is HIGH, the switches are turned off. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of  $V_{DD}$ .

### 2. Features and benefits

- Wide supply voltage range from 3.0 V to 15.0 V
- CMOS low power dissipation
- High noise immunity
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Complies with JEDEC standard JESD 13-B
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-B exceeds 200 V
- Specified from -40 °C to +85 °C

### 3. Applications

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

### 4. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
<a href="#">HEF4067BT</a>	-40 °C to +85 °C	SO24	plastic small outline package; 24 leads; body width 7.5 mm	<a href="#">SOT137-1</a>
<a href="#">HEF4067BTT</a>	-40 °C to +85 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	<a href="#">SOT355-1</a>

### 5. Functional diagram

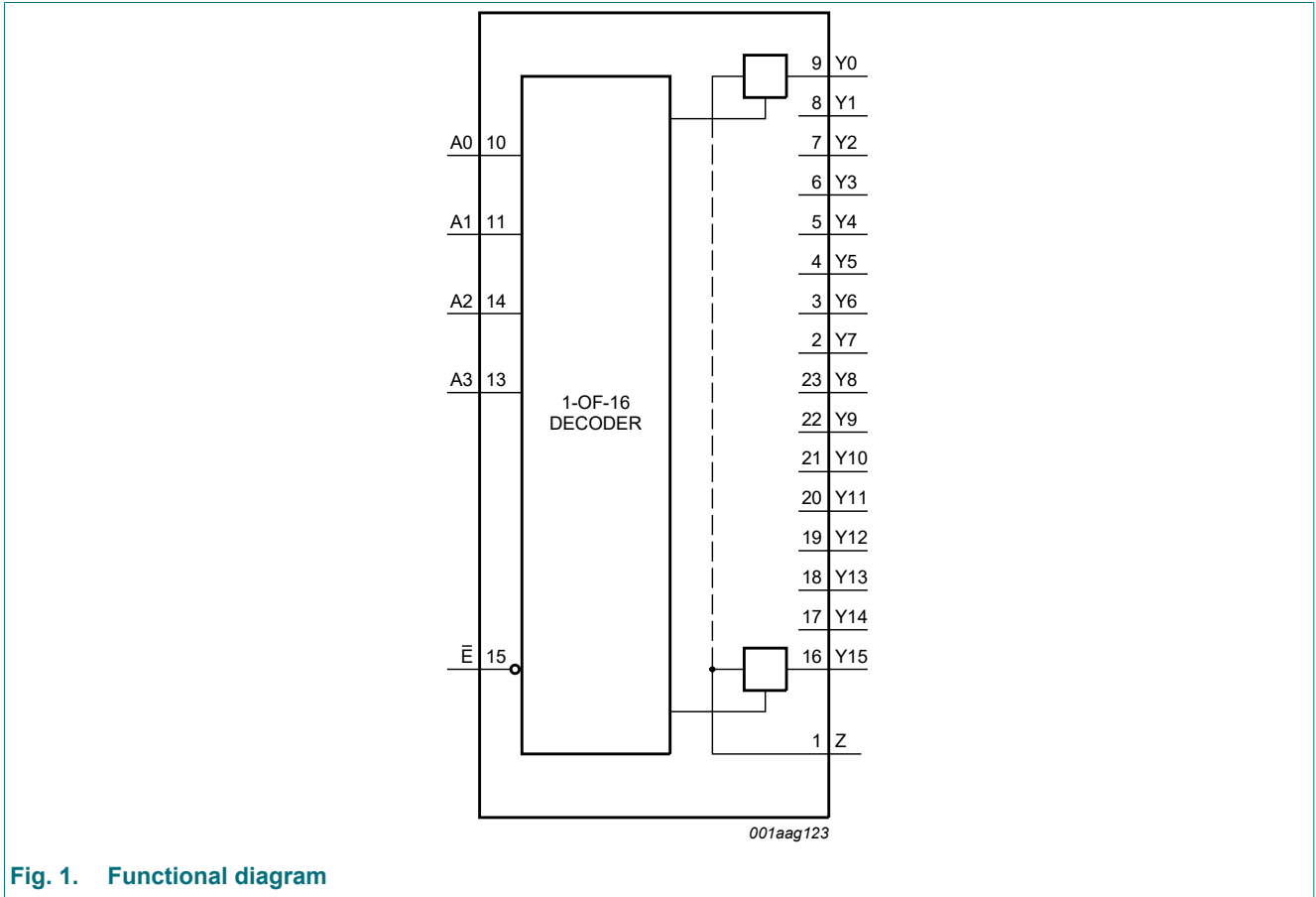


Fig. 1. Functional diagram

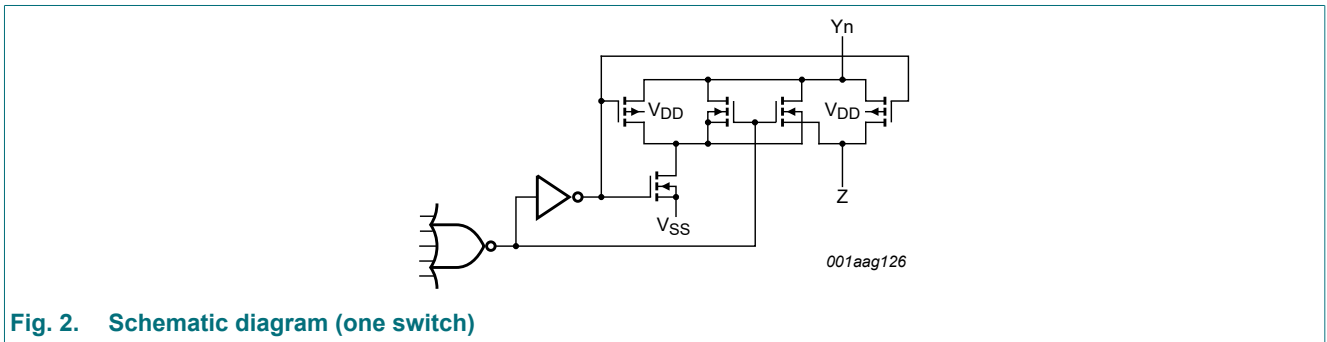


Fig. 2. Schematic diagram (one switch)

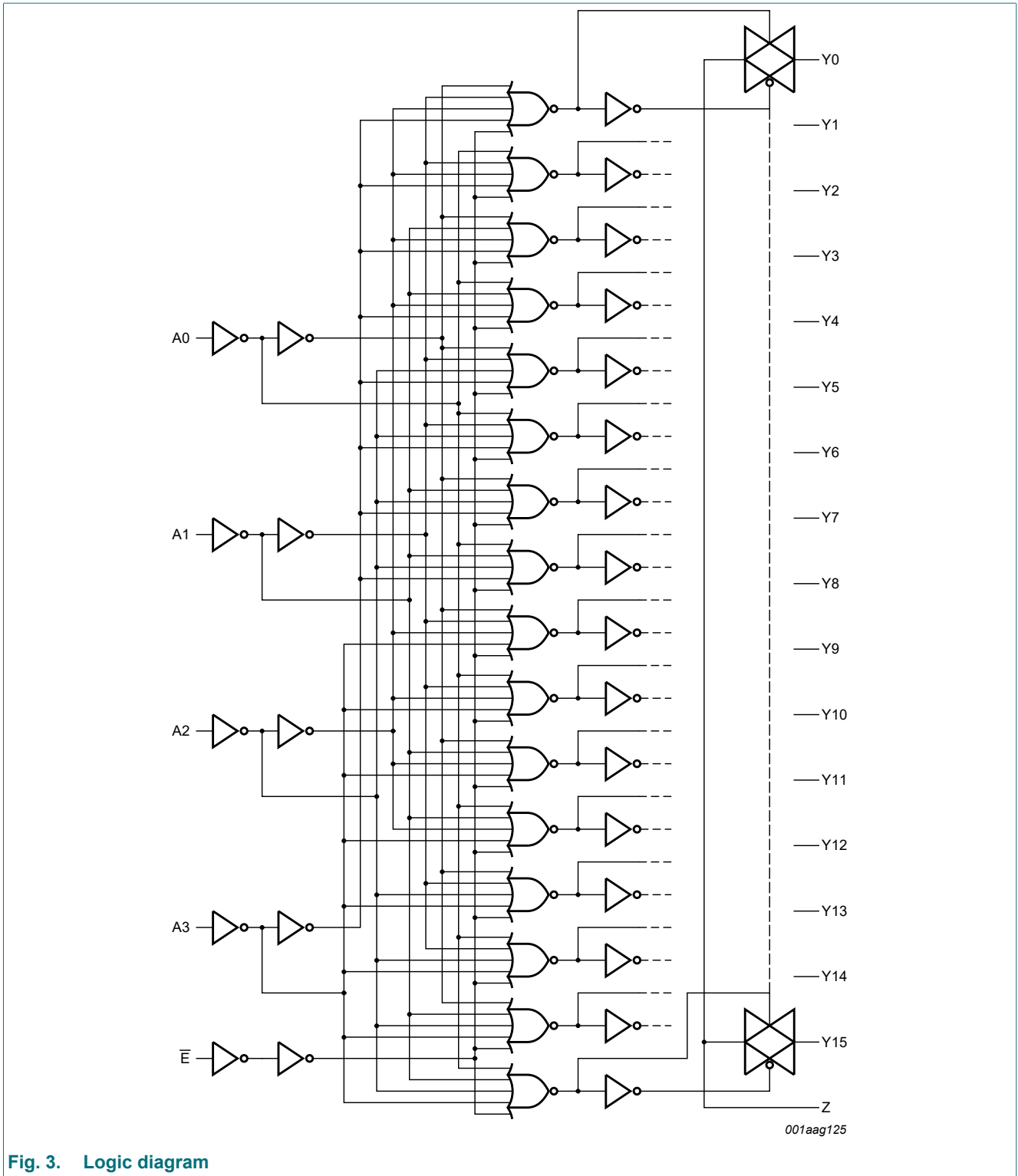
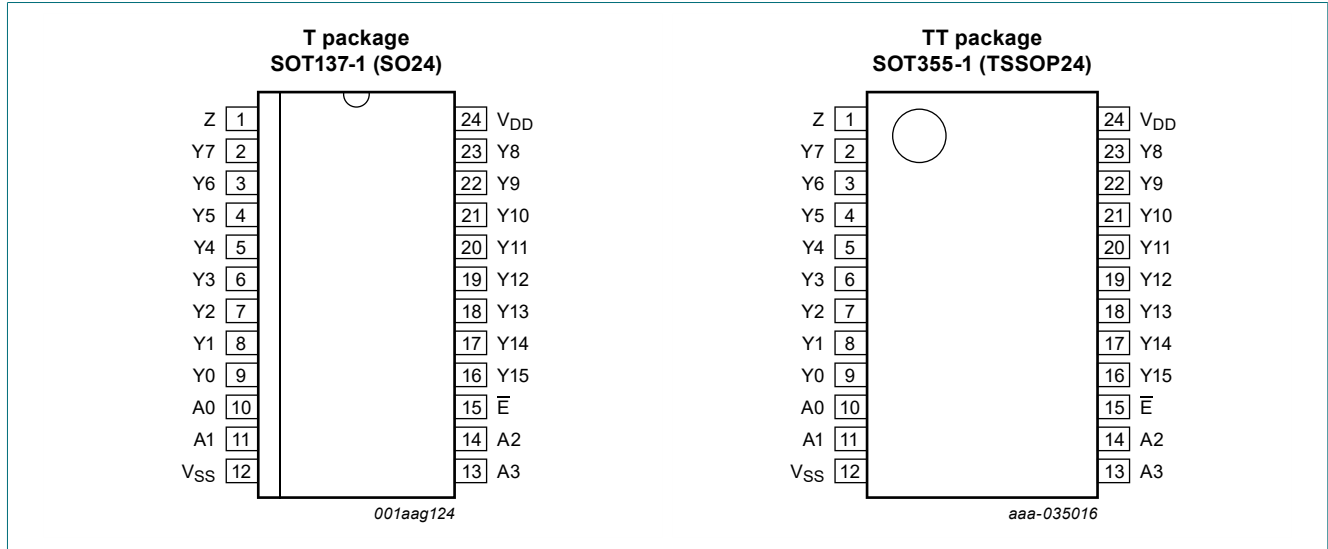


Fig. 3. Logic diagram

## 6. Pinning information

### 6.1. Pinning



### 6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
Z	1	common input/output
Y0, Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8, Y9, Y10, Y11, Y12, Y13, Y14, Y15	9, 8, 7, 6, 5, 4, 3, 2, 23, 22, 21, 20, 19, 18, 17, 16	independent input/output
A0, A1, A2, A3	10, 11, 14, 13	address input
V <sub>SS</sub>	12	ground (0 V)
$\bar{E}$	15	enable input (active LOW)
V <sub>DD</sub>	24	supply voltage

## 7. Functional description

**Table 3. Function table**

*H = HIGH voltage level; L = LOW voltage level; X = don't care.*

Control	Address				Channel ON
	A3	A2	A1	A0	
L	L	L	L	L	Y0 = Z
L	L	L	L	H	Y1 = Z
L	L	L	H	L	Y2 = Z
L	L	L	H	H	Y3 = Z
L	L	H	L	L	Y4 = Z
L	L	H	L	H	Y5 = Z
L	L	H	H	L	Y6 = Z
L	L	H	H	H	Y7 = Z
L	H	L	L	L	Y8 = Z
L	H	L	L	H	Y9 = Z
L	H	L	H	L	Y10 = Z
L	H	L	H	H	Y11 = Z
L	H	H	L	L	Y12 = Z
L	H	H	L	H	Y13 = Z
L	H	H	H	L	Y14 = Z
L	H	H	H	H	Y15 = Z
H	X	X	X	X	none

## 8. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to  $V_{SS} = 0$  V (ground).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD}$	supply voltage		-0.5	+18	V
$I_{IK}$	input clamping current	pins An and $\bar{E}$ ; $V_I < -0.5$ V or $V_I > V_{DD} + 0.5$ V	-	$\pm 10$	mA
$V_I$	input voltage		-0.5	$V_{DD} + 0.5$	V
$I_{I/O}$	input/output current	[1]	-	$\pm 10$	mA
$I_{DD}$	supply current		-	50	mA
$T_{stg}$	storage temperature		-65	+150	°C
$T_{amb}$	ambient temperature		-40	+85	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +85 °C	-	500	mW
P	power dissipation	per output	-	100	mW

- [1] To avoid drawing  $V_{DD}$  current out of terminal Z, when switch current flows into terminals Yn, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no  $V_{DD}$  current will flow out of terminals Yn, in this case there is no limit for the voltage drop across the switch, but the voltages at Y and Z may not exceed  $V_{DD}$  or  $V_{SS}$ .

## 9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD}$	supply voltage		3	-	15	V
$V_I$	input voltage		0	-	$V_{DD}$	V
$T_{amb}$	ambient temperature	in free air	-40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5\text{ V}$	-	-	3.75	$\mu\text{s/V}$
		$V_{DD} = 10\text{ V}$	-	-	0.5	$\mu\text{s/V}$
		$V_{DD} = 15\text{ V}$	-	-	0.08	$\mu\text{s/V}$

## 10. Static characteristics

Table 6. Static characteristics

$V_{SS} = 0\text{ V}$ ;  $V_I = V_{SS}$  or  $V_{DD}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	$T_{amb} = -40\text{ °C}$		$T_{amb} = +25\text{ °C}$		$T_{amb} = +85\text{ °C}$		Unit
				Min	Max	Min	Max	Min	Max	
$V_{IL}$	LOW-level input voltage	$ I_{O1}  < 1\ \mu\text{A}$								
		$V_O = 0.5\text{ V}$ or $4.5\text{ V}$	5 V	-	1	-	1	-	1	V
		$V_O = 1.0\text{ V}$ or $9.0\text{ V}$	10 V	-	2	-	2	-	2	V
		$V_O = 1.5\text{ V}$ or $13.5\text{ V}$	15 V	-	2.5	-	2.5	-	2.5	V
$V_{IH}$	HIGH-level input voltage	$ I_{O1}  < 1\ \mu\text{A}$								
		$V_O = 0.5\text{ V}$ or $4.5\text{ V}$	5 V	4	-	4	-	4	-	V
		$V_O = 1.0\text{ V}$ or $9.0\text{ V}$	10 V	8	-	8	-	8	-	V
		$V_O = 1.5\text{ V}$ or $13.5\text{ V}$	15 V	12.5	-	12.5	-	12.5	-	V
$I_I$	input leakage current	$V_I = 0\text{ V}$ or $15\text{ V}$	15 V	-	$\pm 0.3$	-	$\pm 0.3$	-	$\pm 1.0$	$\mu\text{A}$
$I_{S(OFF)}$	OFF-state leakage current	Z port; all channels OFF; see Fig. 4	15 V	-	-	-	1000	-	7500	nA
		Yn port; per channel; see Fig. 5	15 V	-	-	-	200	-	1500	nA
$I_{DD}$	supply current	all valid input combinations; $I_O = 0\text{ A}$	5 V	-	20	-	20	-	150	$\mu\text{A}$
			10 V	-	40	-	40	-	300	$\mu\text{A}$
			15 V	-	80	-	80	-	600	$\mu\text{A}$
$C_I$	input capacitance	digital inputs	15 V	-	-	-	7.5	-	-	pF

10.1. Test circuits

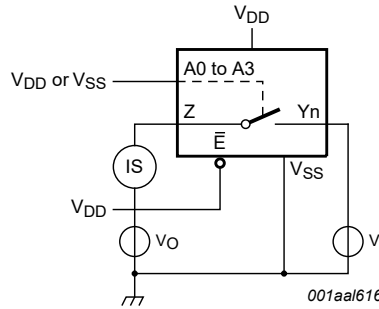


Fig. 4. Test circuit for measuring OFF-state leakage current Z port

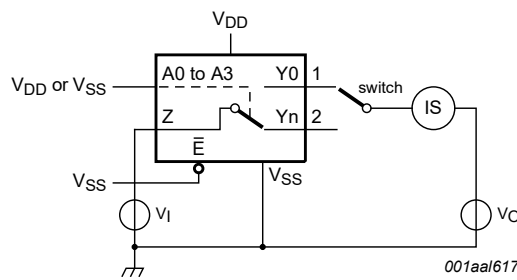


Fig. 5. Test circuit for measuring OFF-state leakage current Yn port

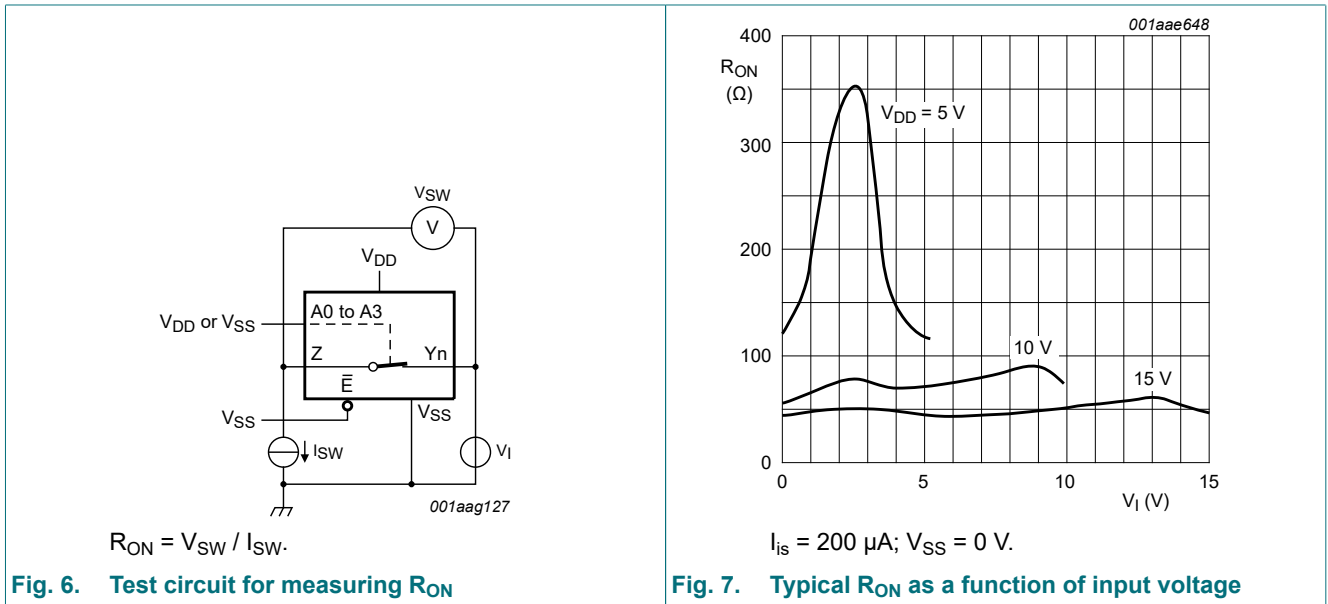
10.2. On resistance

Table 7. ON resistance

$T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $I_{SW} = 200\text{ }\mu\text{A}$ ;  $V_{SS} = 0\text{ V}$ .

Symbol	Parameter	Conditions	V <sub>DD</sub>	Typ	Max	Unit
R <sub>ON(peak)</sub>	ON resistance (peak)	V <sub>I</sub> = 0 V to V <sub>DD</sub> ; see Fig. 6 and Fig. 7	5 V	350	2500	Ω
			10 V	80	245	Ω
			15 V	60	175	Ω
R <sub>ON(rail)</sub>	ON resistance (rail)	V <sub>I</sub> = 0 V; see Fig. 6 and Fig. 7	5 V	115	340	Ω
			10 V	50	160	Ω
			15 V	40	115	Ω
		V <sub>I</sub> = V <sub>DD</sub> ; see Fig. 6 and Fig. 7	5 V	120	365	Ω
			10 V	65	200	Ω
			15 V	50	155	Ω
ΔR <sub>ON</sub>	ON resistance mismatch between channels	V <sub>I</sub> = 0 V to V <sub>DD</sub> ; see Fig. 6	5 V	25	-	Ω
			10 V	10	-	Ω
			15 V	5	-	Ω

10.2.1. On resistance waveform and test circuit



11. Dynamic characteristics

Table 8. Dynamic characteristics

$T_{amb} = 25 \text{ }^\circ\text{C}; V_{SS} = 0 \text{ V};$  for test circuit see Fig. 11.

Symbol	Parameter	Conditions	$V_{DD}$	Min	Typ	Max	Unit
$t_{PHL}$	HIGH to LOW propagation delay	$Y_n, Z$ to $Z, Y_n$ ; see Fig. 8	5 V	-	30	60	ns
			10 V	-	15	25	ns
			15 V	-	10	20	ns
		$A_n$ to $Y_n, Z$ ; see Fig. 9	5 V	-	190	380	ns
			10 V	-	70	145	ns
			15 V	-	50	100	ns
$t_{PLH}$	LOW to HIGH propagation delay	$Y_n, Z$ to $Z, Y_n$ ; see Fig. 8	5 V	-	25	50	ns
			10 V	-	10	20	ns
			15 V	-	10	20	ns
		$A_n$ to $Y_n, Z$ ; see Fig. 9	5 V	-	175	345	ns
			10 V	-	70	140	ns
			15 V	-	50	100	ns
$t_{PHZ}$	HIGH to OFF-state propagation delay	$\bar{E}$ to $Y_n, Z$ ; see Fig. 10	5 V	-	195	385	ns
			10 V	-	140	280	ns
			15 V	-	130	260	ns
$t_{PLZ}$	LOW to OFF-state propagation delay	$\bar{E}$ to $Y_n, Z$ ; see Fig. 10	5 V	-	215	435	ns
			10 V	-	180	355	ns
			15 V	-	170	340	ns
$t_{PZH}$	OFF-state to HIGH propagation delay	$\bar{E}$ to $Y_n, Z$ ; see Fig. 10	5 V	-	155	315	ns
			10 V	-	70	135	ns
			15 V	-	50	100	ns



Symbol	Parameter	Conditions	V <sub>DD</sub>	Min	Typ	Max	Unit
t <sub>PZL</sub>	OFF-state to LOW propagation delay	$\bar{E}$ to Y <sub>n</sub> , Z; see Fig. 10	5 V	-	170	340	ns
			10 V	-	70	140	ns
			15 V	-	50	100	ns

11.1. Waveforms and test circuit

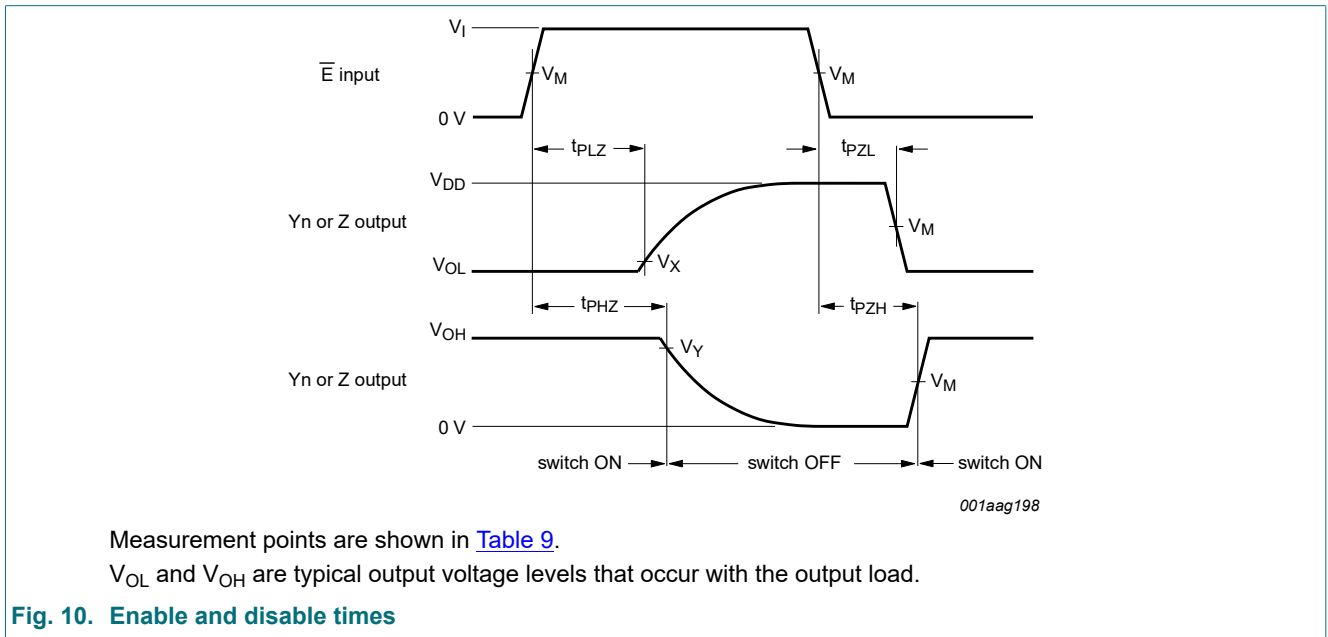
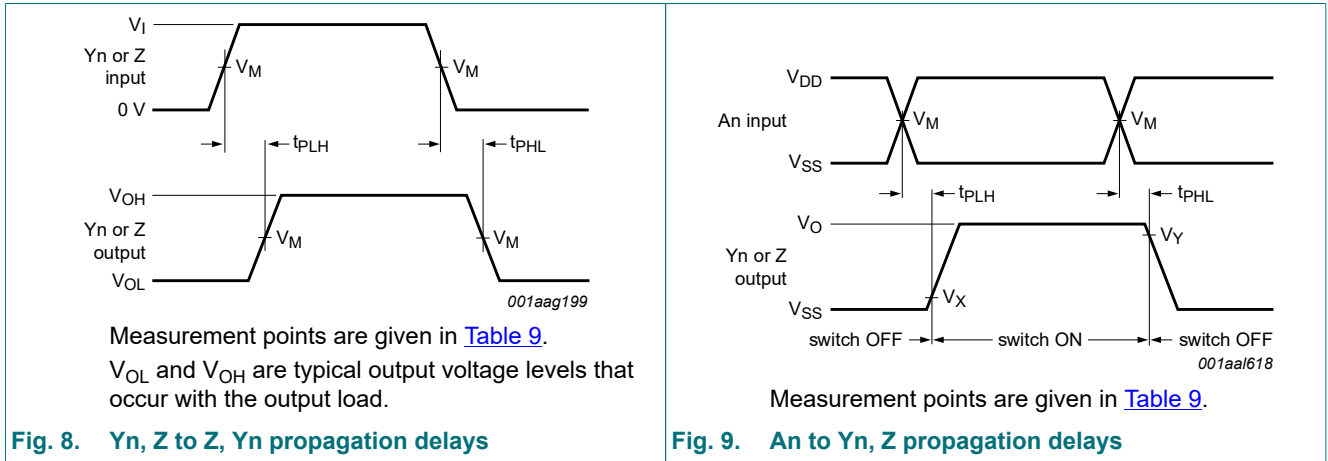


Table 9. Measurement points

Supply voltage	Input		Output		
	V <sub>M</sub>	V <sub>I</sub>	V <sub>M</sub>	V <sub>X</sub>	V <sub>Y</sub>
5 V to 15 V	0.5 × V <sub>DD</sub>	GND to V <sub>DD</sub>	0.5 × V <sub>DD</sub>	10%	90%

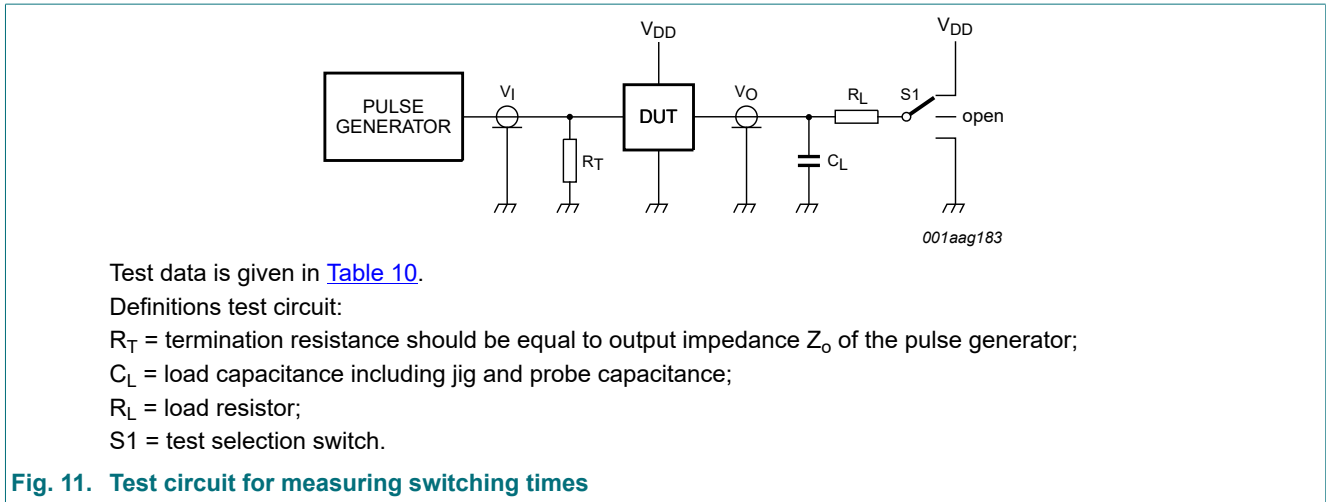


Fig. 11. Test circuit for measuring switching times

Table 10. Test data

Input				Load		S1 position				
Yn, Z	An and E	$t_r, t_f$	$V_M$	$C_L$	$R_L$	$t_{PHL}$ [1]	$t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$	other
$V_{DD}$ or $V_{SS}$	$V_{DD}$ or $V_{SS}$	$\leq 20$ ns	$0.5 \times V_{DD}$	50 pF	10 k $\Omega$	$V_{DD}$ or $V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{DD}$	$V_{SS}$

[1] For Yn to Z or Z to Yn propagation delays use  $V_{SS}$ . For An or to Yn or Z propagation delays use  $V_{DD}$ .

## 11.2. Additional dynamic parameters

Table 11. Additional dynamic characteristics

$V_{SS} = 0$  V;  $T_{amb} = 25$  °C.

Symbol	Parameter	Conditions	$V_{DD}$	Typ	Max	Unit
THD	total harmonic distortion	see <a href="#">Fig. 12</a> ; $R_L = 10$ k $\Omega$ ; $C_L = 15$ pF; channel ON; $V_I = 0.5 \times V_{DD}$ (p-p); $f_i = 1$ kHz	[1] 5 V	0.25	-	%
			10 V	0.04	-	%
			15 V	0.04	-	%
$f_{(-3dB)}$	-3 dB frequency response	see <a href="#">Fig. 13</a> ; $R_L = 1$ k $\Omega$ ; $C_L = 5$ pF; channel ON; $V_I = 0.5 \times V_{DD}$ (p-p)	[1] 5 V	13	-	MHz
			10 V	40	-	MHz
			15 V	70	-	MHz
$\alpha_{iso}$	isolation (OFF-state)	see <a href="#">Fig. 14</a> ; $f_i = 1$ MHz; $R_L = 1$ k $\Omega$ ; $C_L = 5$ pF; [1] channel OFF; $V_I = 0.5 \times V_{DD}$ (p-p)	10 V	-50	-	dB
$V_{ct}$	crosstalk voltage	digital inputs to switch; see <a href="#">Fig. 15</a> ; $R_L = 10$ k $\Omega$ ; $C_L = 15$ pF; $\bar{E}$ or An = $V_{DD}$ (square-wave)	10 V	50	-	mV
Xtalk	crosstalk	between switches; see <a href="#">Fig. 16</a> ; $f_i = 1$ MHz; [1] $R_L = 1$ k $\Omega$ ; $V_I = 0.5 \times V_{DD}$ (p-p)	10 V	-50	-	dB

[1]  $f_i$  is biased at  $0.5 \times V_{DD}$ ;  $V_I = 0.5 \times V_{DD}$  (p-p).

Table 12. Dynamic power dissipation  $P_D$

$P_D$  can be calculated from the formulas shown;  $V_{SS} = 0$  V;  $t_r = t_f \leq 20$  ns;  $T_{amb} = 25$  °C.

Symbol	Parameter	$V_{DD}$	Typical formula for $P_D$ ( $\mu$ W)	where:
$P_D$	dynamic power dissipation	5 V	$P_D = 1000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	$f_i$ = input frequency in MHz; $f_o$ = output frequency in MHz; $C_L$ = output load capacitance in pF; $V_{DD}$ = supply voltage in V; $\Sigma(C_L \times f_o)$ = sum of the outputs.
		10 V	$P_D = 5500 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	
		15 V	$P_D = 15000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	

11.2.1. Test circuits

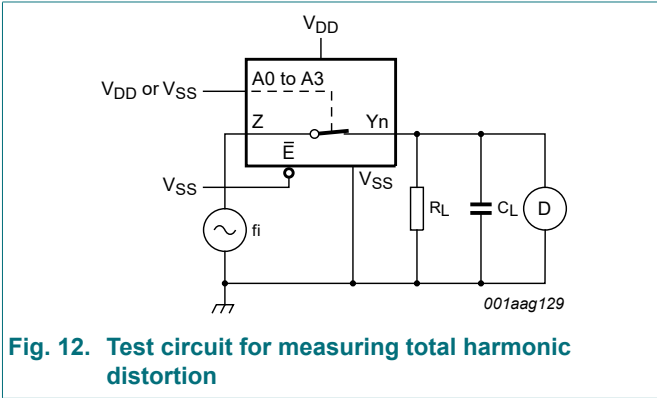


Fig. 12. Test circuit for measuring total harmonic distortion

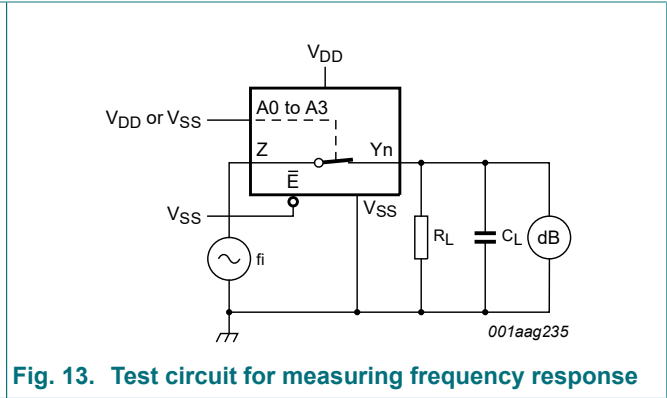


Fig. 13. Test circuit for measuring frequency response

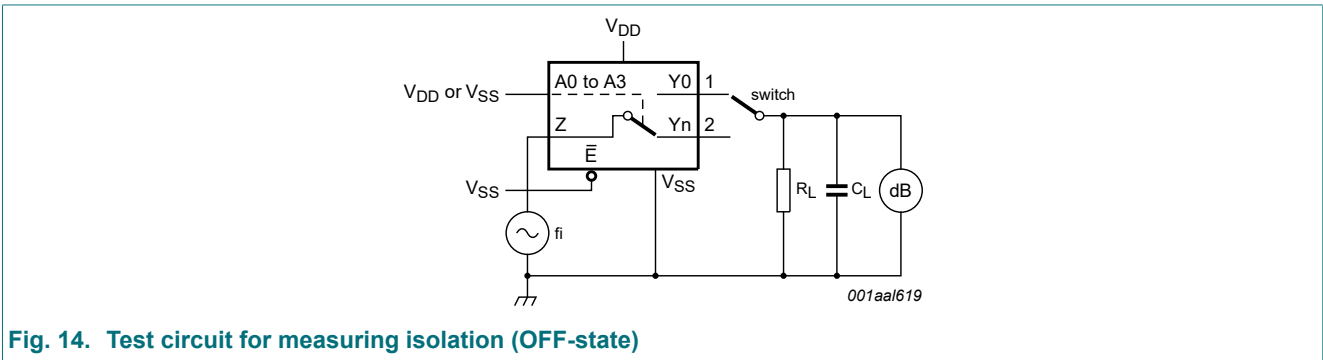


Fig. 14. Test circuit for measuring isolation (OFF-state)

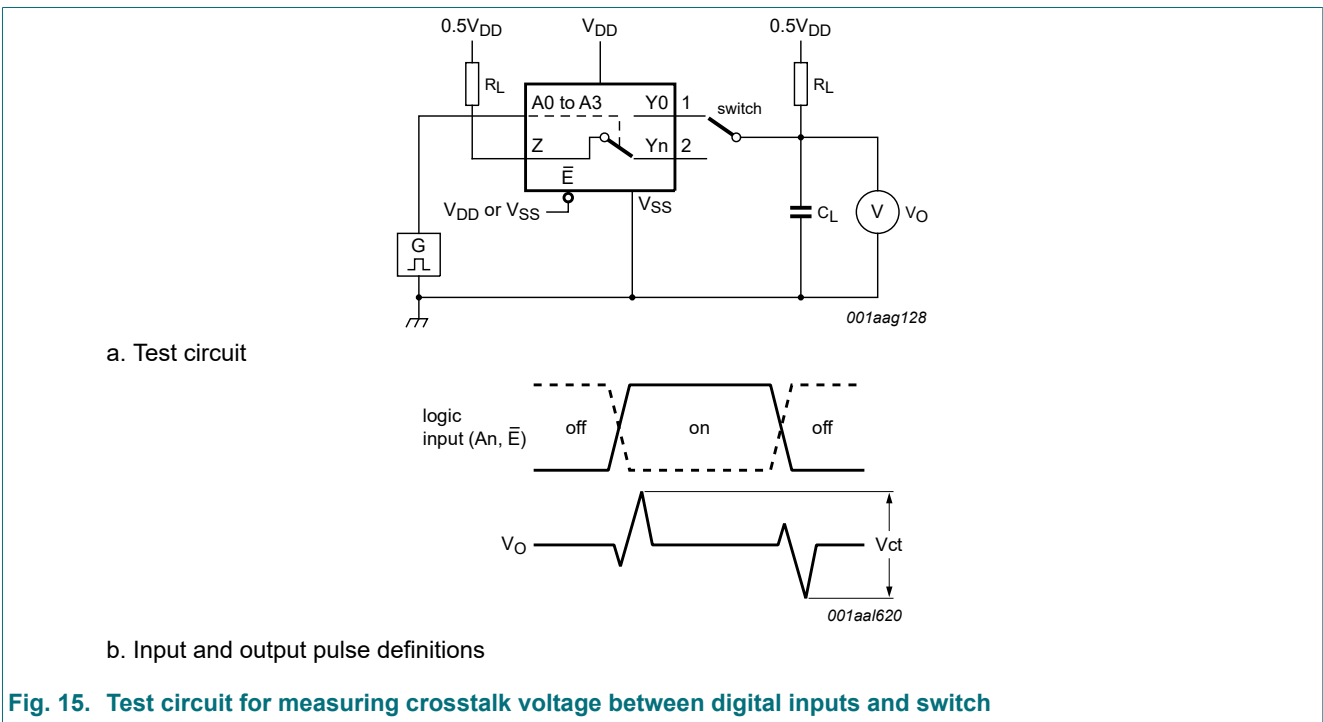


Fig. 15. Test circuit for measuring crosstalk voltage between digital inputs and switch

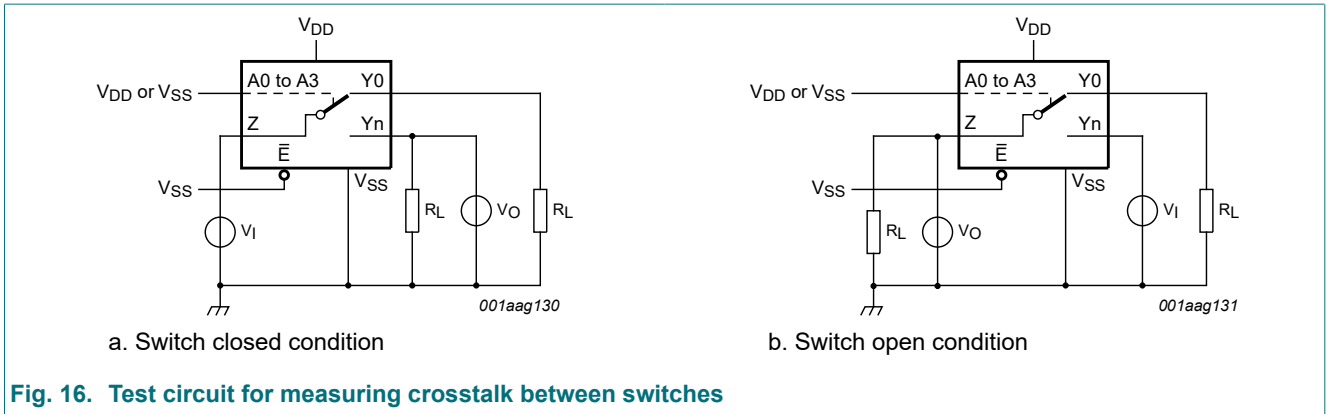


Fig. 16. Test circuit for measuring crosstalk between switches

12. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1

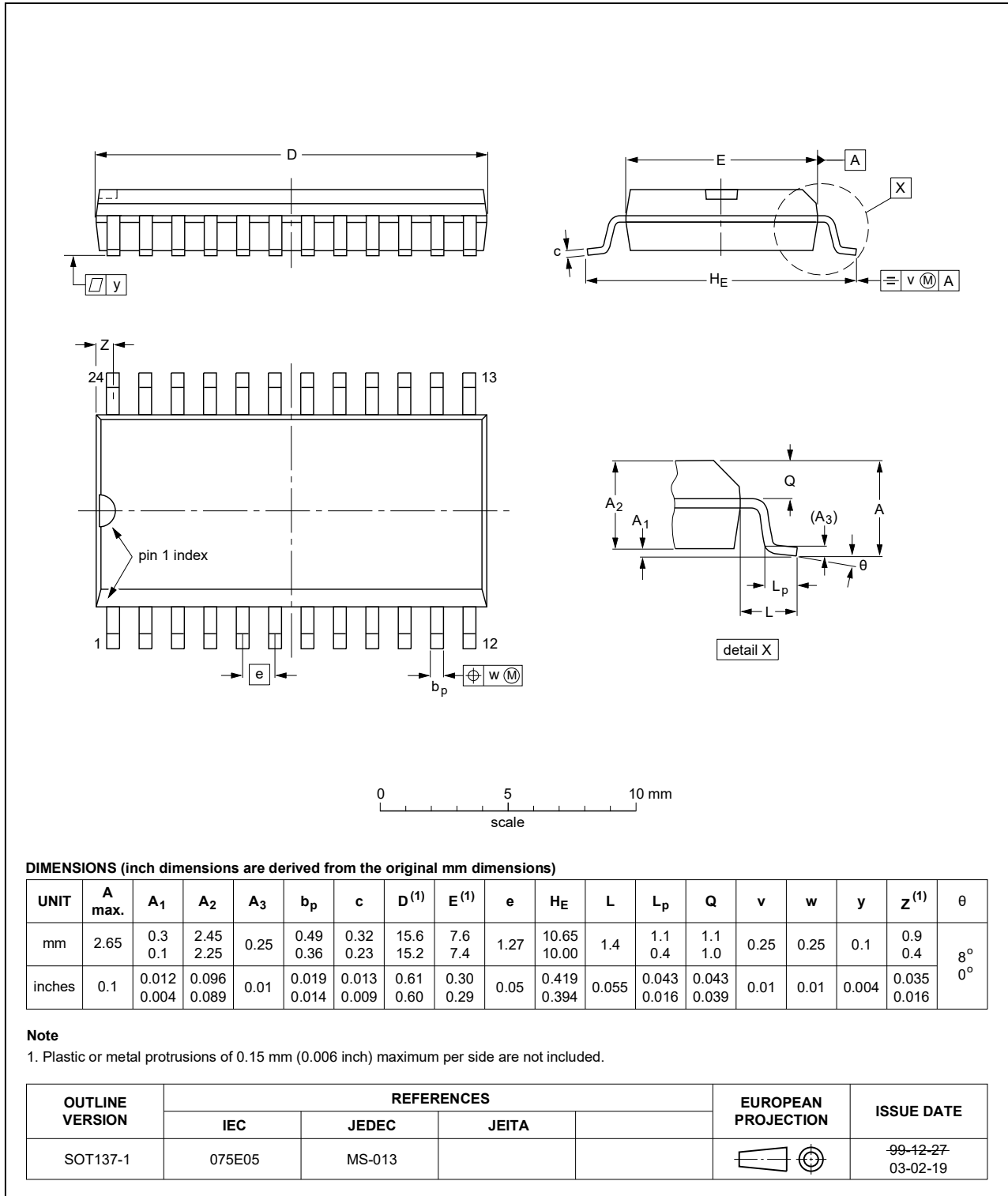


Fig. 17. Package outline SOT137-1 (SO24)

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1

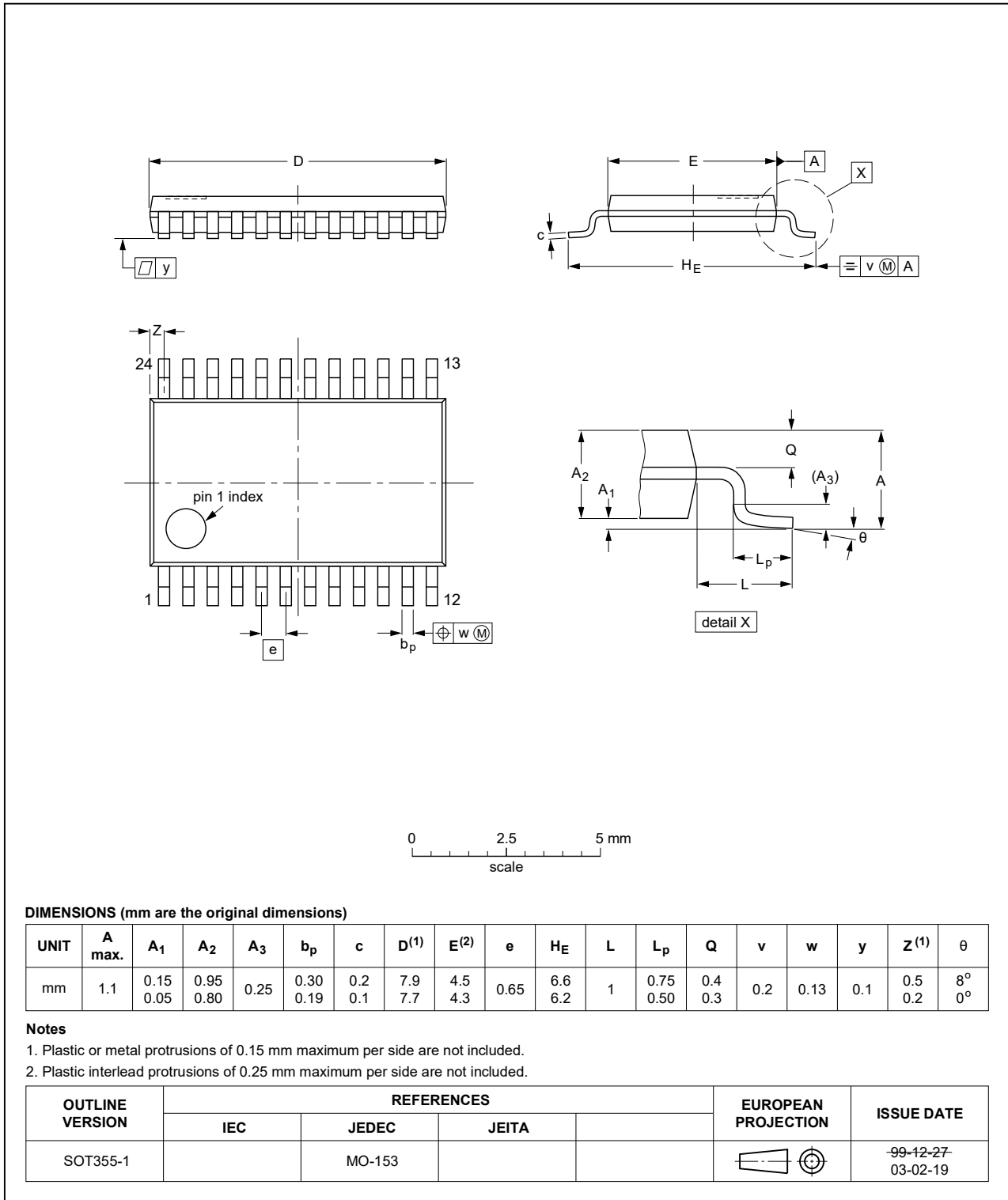


Fig. 18. Package outline SOT355-1 (TSSOP24)

## 13. Abbreviations

Table 13. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

## 14. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4067B v.10	20231107	Product data sheet	-	HEF4067B v.9
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Table 6</a>: <math>I_{S(OFF)}</math> parameter added for +85 °C, <math>I_{OZ}</math> specification removed.</li> <li>• Type number HEF4067BTT (SOT355-1/TSSOP24) added.</li> </ul>			
HEF4067B v.9	20220106	Product data sheet	-	HEF4067B v.8
Modifications:	<ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> <li>• <a href="#">Section 1</a> and <a href="#">Section 2</a> updated.</li> </ul>			
HEF4067B v.8	20160418	Product data sheet	-	HEF4067B v.7
Modifications:	<ul style="list-style-type: none"> <li>• Type number HEF4067BP (SOT101-1) removed.</li> <li>• <a href="#">Table 8</a>: Typo corrected in conditions row for <math>T_{PZH}</math> and <math>T_{PZL}</math>.</li> </ul>			
HEF4067B v.7	20140911	Product data sheet	-	HEF4067B v.6
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Fig. 15</a>: Test circuit modified</li> </ul>			
HEF4067B v.6	20111116	Product data sheet	-	HEF4067B v.5
Modifications:	<ul style="list-style-type: none"> <li>• Legal pages updated.</li> <li>• Changes in <a href="#">Section 1</a>, <a href="#">Section 2</a>, and <a href="#">Section 3</a>.</li> </ul>			
HEF4067B v.5	20100325	Product data sheet	-	HEF4067B v.4
HEF4067B v.4	20100308	Product data sheet	-	HEF4067B_CNV v.3
HEF4067B_CNV v.3	19950101	Product specification	-	HEF4067B_CNV v.2
HEF4067B_CNV v.2	19950101	Product specification	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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## Contents

<b>1. General description</b> .....	<b>1</b>
<b>2. Features and benefits</b> .....	<b>1</b>
<b>3. Applications</b> .....	<b>1</b>
<b>4. Ordering information</b> .....	<b>1</b>
<b>5. Functional diagram</b> .....	<b>2</b>
<b>6. Pinning information</b> .....	<b>4</b>
6.1. Pinning.....	4
6.2. Pin description.....	4
<b>7. Functional description</b> .....	<b>5</b>
<b>8. Limiting values</b> .....	<b>5</b>
<b>9. Recommended operating conditions</b> .....	<b>6</b>
<b>10. Static characteristics</b> .....	<b>6</b>
10.1. Test circuits.....	7
10.2. On resistance.....	7
10.2.1. On resistance waveform and test circuit.....	8
<b>11. Dynamic characteristics</b> .....	<b>8</b>
11.1. Waveforms and test circuit.....	9
11.2. Additional dynamic parameters.....	10
11.2.1. Test circuits.....	11
<b>12. Package outline</b> .....	<b>13</b>
<b>13. Abbreviations</b> .....	<b>15</b>
<b>14. Revision history</b> .....	<b>15</b>
<b>15. Legal information</b> .....	<b>16</b>

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