



GANB012-040CBA

40 V, 12 mOhm bi-directional Gallium Nitride (GaN) FET in a 1.2 mm x 1.7 mm Wafer Level Chip-Scale Package (WLCSP)

12 March 2025

Product data sheet

1. General description

The GANB012-040CBA is a 40 V, 12 mΩ bi-directional Gallium Nitride (GaN) High Electron-Mobility-Transistor (HEMT) in a Wafer Level Chip-Scale (WLCSP) package. It is a normally-off e-mode device offering superior performance.

2. Features and benefits

- Enhancement mode - normally-off power switch
- Bi-directional device
- Ultra high switching speed capability
- Ultra-low on-state resistance
- RoHS, Pb-free, REACH-compliant
- High efficiency and high power density
- Wafer Level Chip-Scale Package (WLCSP) 1.2 mm x 1.7 mm

3. Applications

- High-side load switch
- OVP protection in smart phone USB port
- Power switch circuits
- Stand-by power system

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DD}	drain-drain voltage	$-40\text{ °C} \leq T_j \leq 125\text{ °C}$	[1]	-	-	40	V
I_D	drain current	$V_{GD} = 5\text{ V}; T_{mb} = 25\text{ °C}$	[2][3]	-	-	10	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}; \text{Fig. 1}$		-	-	11	W
T_j	junction temperature			-40	-	125	°C
Static characteristics							
R_{DDon}	drain-drain on-state resistance	$V_{GD2} = 5\text{ V}; V; I_{D1} = 10\text{ A}; T_j = 25\text{ °C}; \text{Fig. 9; Fig. 10; Fig. 11}$	[1]	-	9	12	mΩ
		$V_{GD2} = 5\text{ V}; V; I_{D1} = 10\text{ A}; T_j = 125\text{ °C}; \text{Fig. 9; Fig. 12}$	[1]	-	16.5	-	mΩ

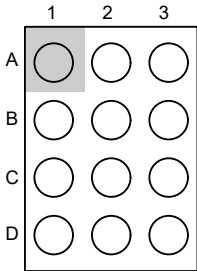
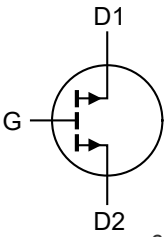
40 V, 12 mOhm bi-directional Gallium Nitride (GaN) FET in a 1.2 mm x 1.7 mm Wafer Level Chip-Scale Package (WLCSP)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	$I_D = 10\text{ A}$; $V_{DS} = 20\text{ V}$; $V_{GS} = 5\text{ V}$; $T_j = 25\text{ °C}$; Fig. 13 ; Fig. 14	[2]	-	7.2	-	nC

- [1] Parameters are understood to apply for either polarity of bias. For example, V_{DD} is the same whether D1 is the source and D2 is the drain or vice versa.
- [2] D1 and D2 are symetrical with respect to the gate, G. Either can take the function of source or drain. For datasheet parameters, the source is defined as the terminal, D1 or D2, which has lower potential in the test circuit. The drain is the terminal with the higher potential.
- [3] Limited by solder ball

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
B2-B3, D1-D3	D1	drain1	 Transparent top view WLCSP12_SOT8088	 <i>aaa-037587</i>
A1-A3, C2-C3	D2	drain2		
B1, C1	G	gate		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
GANB012-040CBA	WLCSP12_SOT8088	WLCSP12, 1.2 mm x 1.7 mm	WLCSP12_SOT8088

7. Marking

Table 4. Marking codes

Type number	Marking code
GANB012-040CBA	012ACBA

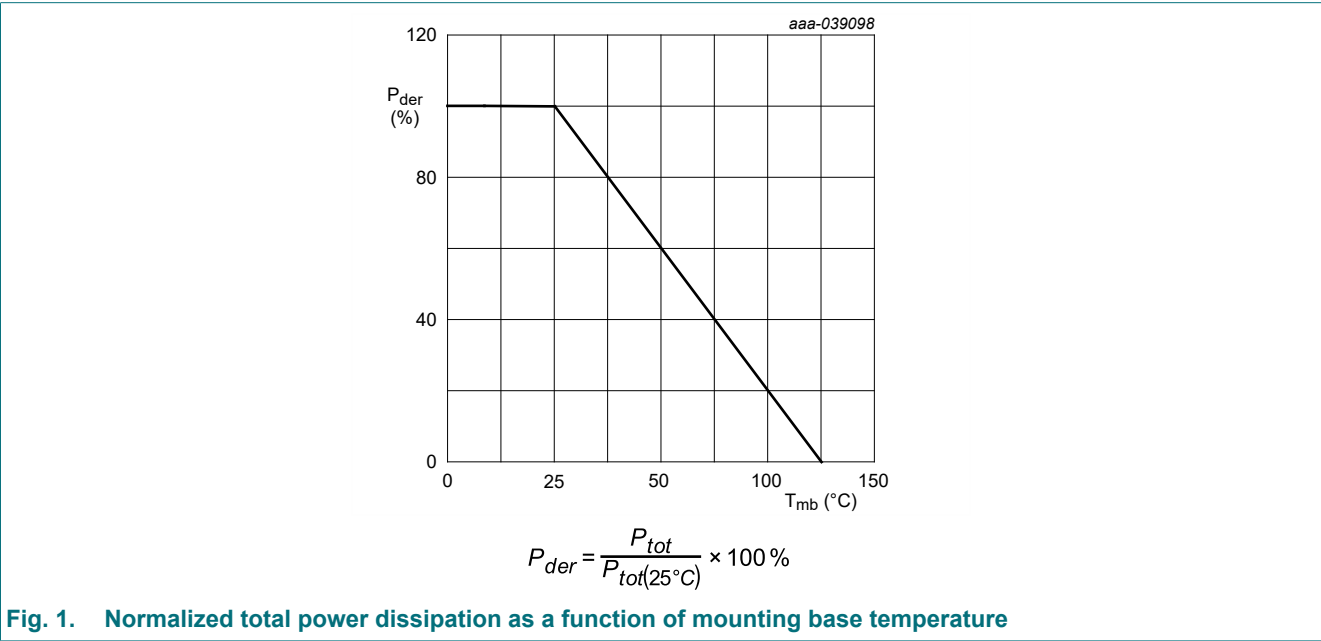
8. Limiting values

Table 5. Limiting values

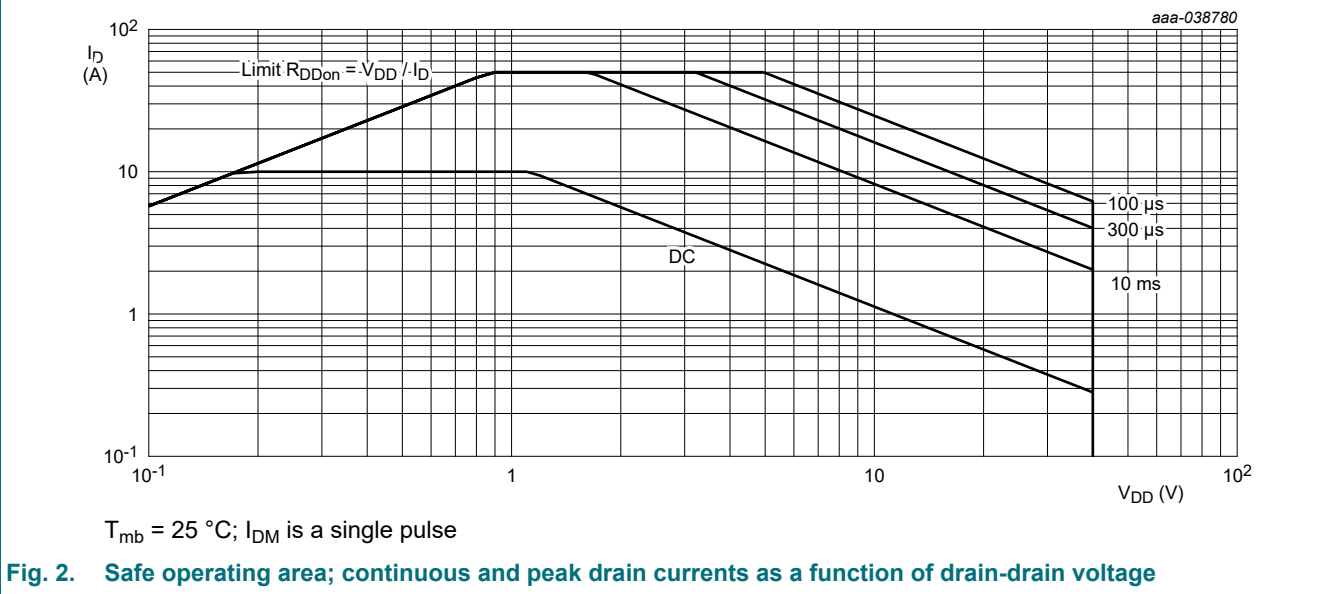
In accordance with the Absolute Maximum Rating System (IEC 60134). $T_j = 25\text{ °C}$ unless otherwise stated.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	drain-drain voltage	$-40\text{ °C} \leq T_j \leq 125\text{ °C}$	[1]	-	40	V
V_{DG}	drain-gate voltage		[1]	-	40	V
V_{GD}	gate-drain voltage		[1]	-	6	V
I_D	drain current	$V_{GD} = 5\text{ V}; T_{mb} = 25\text{ °C}$	[2] [3]	-	10	A
I_{DM}	peak drain current	pulsed; $t_p \leq 300\text{ }\mu\text{s}; T_{mb} = 25\text{ °C}$; Fig. 2	[2] [3]	-	50	A
$P_{(tot)}$	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	11	W
T_{stg}	storage temperature			-40	150	°C
T_j	junction temperature			-40	125	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C

- [1] Parameters are understood to apply for either polarity of bias. For example, V_{DD} is the same whether D1 is the source and D2 is the drain or vice versa.
- [2] D1 and D2 are symetrical with respect to the gate, G. Either can take the function of source or drain. For datasheet parameters, the source is defined as the terminal, D1 or D2, which has lower potential in the test circuit. The drain is the terminal with the higher potential.
- [3] Limited by solder ball.



40 V, 12 mOhm bi-directional Gallium Nitride (GaN) FET in a 1.2 mm x 1.7 mm Wafer Level Chip-Scale Package (WLCSP)

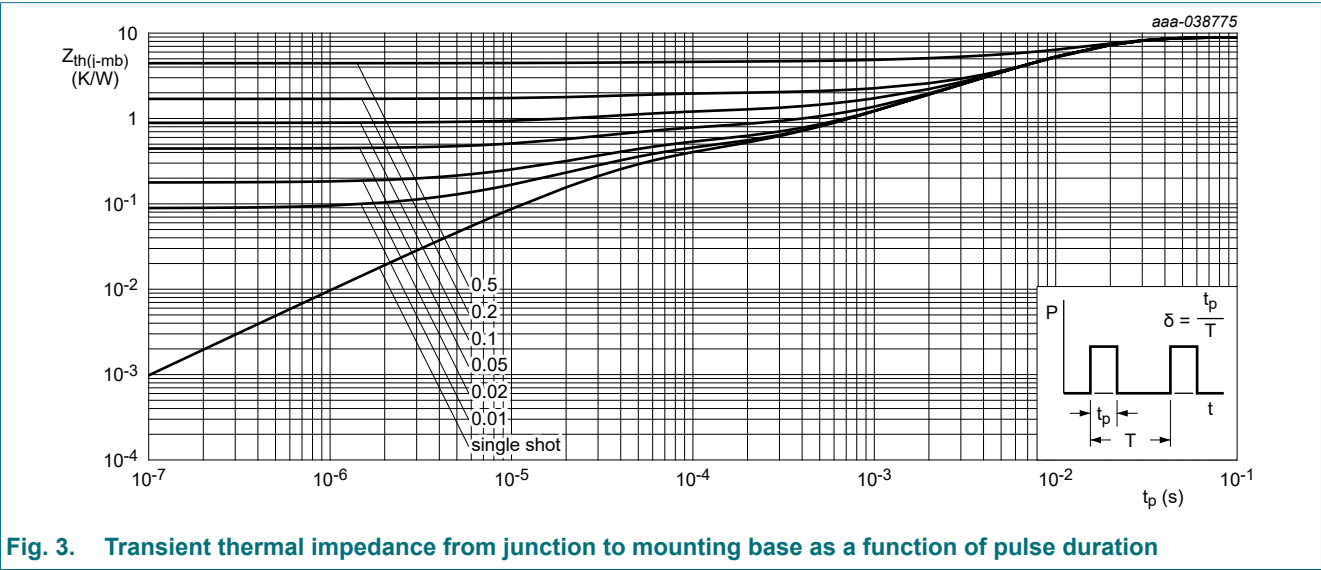


9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-c)}$	thermal resistance from junction to case		[1]	-	-	1.4	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 3		-	-	8.88	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		[2]	-	-	67.35	K/W

- [1] Thermal junction to top side of package.
[2] $R_{th(j-a)}$ is determined with the device mounted on one square inch of copper pad single layer 2 oz copper on FR4 board.



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
BV_{DDs}	drain-drain breakdown voltage	$I_{D1D2} = 500 \mu A$; $V_{D2} = V_G = 0 V$; $T_j = 25^\circ C$	[1]	40	-	-	V
$V_{GD(th)}$	gate-drain threshold voltage	$I_D = 1 mA$; $V_{D1} = 0 V$; $V_{D2} = V_G$; $T_j = 25^\circ C$; Fig. 8	[1]	0.8	1.35	2.4	V
		$I_D = 1 mA$; $V_{D1} = 0 V$; $V_{D2} = V_G$; $T_j = 125^\circ C$; Fig. 8		-	1.1	-	V
I_{DDs}	drain-drain leakage current	$V_{DD} = 40 V$; $V_{GD} = 0 V$; $T_j = 25^\circ C$	[1]	-	0.1	20	μA
I_{GDS}	gate-drain leakage current	$V_{GD} = 5 V$; $V_{DD} = 0 V$; $T_j = 25^\circ C$	[1]	-	0.5	5	μA
		$V_{GD} = -5 V$; $V_{DD} = 0 V$; $T_j = 25^\circ C$	[2]	-30	-	-	μA
		$V_{GD} = 6 V$; $V_{DD} = 0 V$; $T_j = 25^\circ C$		-	5	30	μA
		$V_{GD} = -6 V$; $V_{DD} = 0 V$; $T_j = 25^\circ C$		-40	-	-	μA
		$V_{GD} = 5 V$; $V_{DD} = 0 V$; $T_j = 85^\circ C$	[1]	-	0.5	5	μA
		$V_{GD} = -5 V$; $V_{DD} = 0 V$; $T_j = 85^\circ C$		-30	-	-	μA
		$V_{GD} = 6 V$; $V_{DD} = 0 V$; $T_j = 85^\circ C$		-	5	30	μA
		$V_{GD} = -6 V$; $V_{DD} = 0 V$; $T_j = 85^\circ C$		-40	-	-	μA
R_{DDon}	drain-drain on-state resistance	$V_{GD2} = 5 V$; $I_{D1} = 10 A$; $T_j = 25^\circ C$; Fig. 9 ; Fig. 10 ; Fig. 11	[1]	-	9	12	m Ω
		$V_{GD2} = 5 V$; $I_{D1} = 10 A$; $T_j = 125^\circ C$; Fig. 9 ; Fig. 12		-	16.5	-	m Ω
R_G	gate resistance	$f = 1 MHz$; $T_j = 25^\circ C$	[1]	-	3	-	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	$V_{DS} = 20 V$; $V_{GS} = 5 V$; $I_D = 10 A$; $T_j = 25^\circ C$; Fig. 13 ; Fig. 14	[3]	-	7.2	-	nC
Q_{GS}	gate-source charge			-	0.9	-	nC
Q_{GD}	gate-drain charge			-	3.9	-	nC
C_{iss}	input capacitance	$V_{DS} = 20 V$; $V_{GS} = 0 V$; $f = 1 MHz$; $T_j = 25^\circ C$; Fig. 15	[3]	-	405	-	pF
C_{oss}	output capacitance			-	174	-	pF
C_{rss}	reverse transfer capacitance			-	104	-	pF
Q_{oss}	output charge	$V_{DS} = 20 V$; $V_{GS} = 0 V$; $T_j = 25^\circ C$; Fig. 7	[3][4]	-	5.6	-	nC

- [1] Parameters are understood to apply for either polarity of bias. For example, V_{DD} is the same whether D1 is the source and D2 is the drain or vice versa.
- [2] Specification is validated during qualification at 25°C only
- [3] D1 and D2 are symmetrical with respect to the gate, G. Either can take the function of source or drain. For datasheet parameters, the source is defined as the terminal, D1 or D2, which has lower potential in the test circuit. The drain is the terminal with the higher potential.
- [4] Q_r is not specified separately from Q_{oss} for e-mode GaN FETs, since $Q_r = Q_{oss} + Q_D$, and $Q_D = 0$. (Q_D is charge associated with diffusion of minority carriers. Since there is no body diode, no minority carriers in excess of Q_{oss} have to be transferred for e-mode GaN FETs.)

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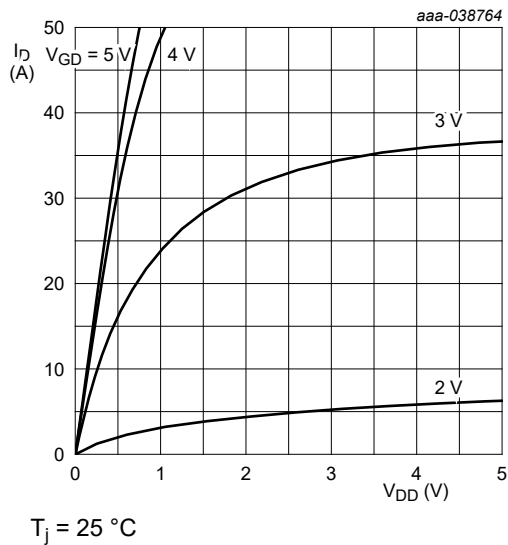


Fig. 4. Output characteristics; drain current as a function of drain-drain voltage; typical values

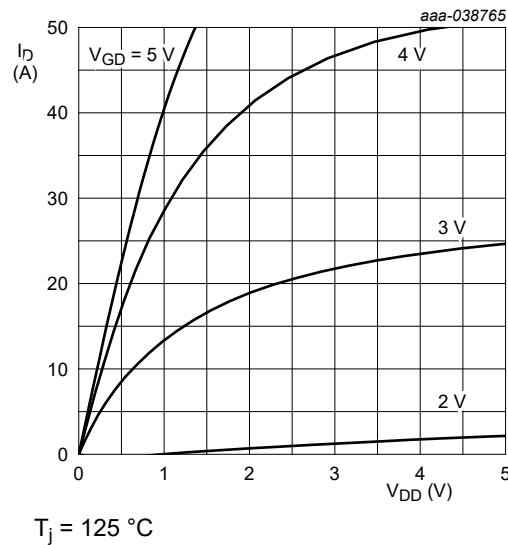


Fig. 5. Output characteristics; drain current as a function of drain-drain voltage; typical values

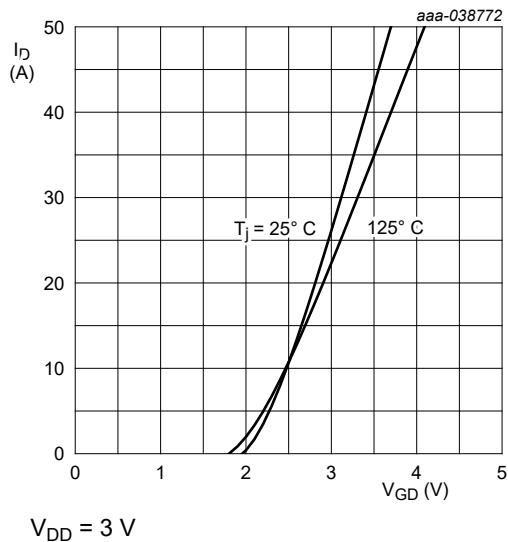


Fig. 6. Transfer characteristics; drain current as a function of gate-drain voltage; typical values

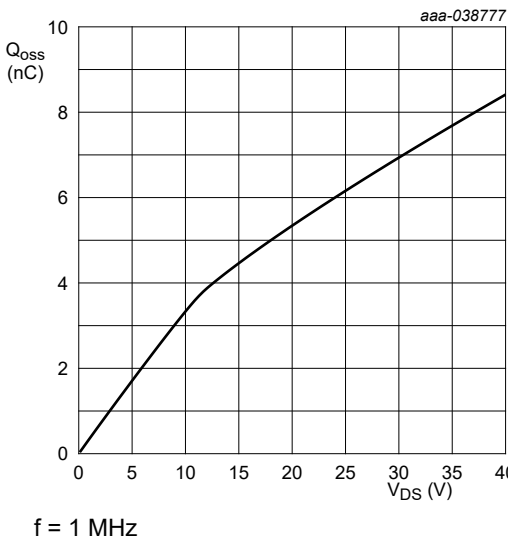
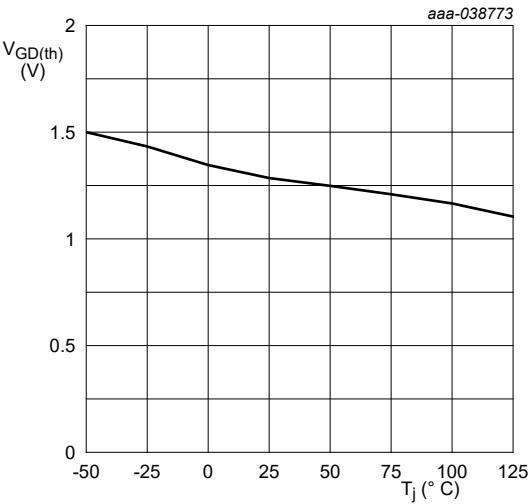


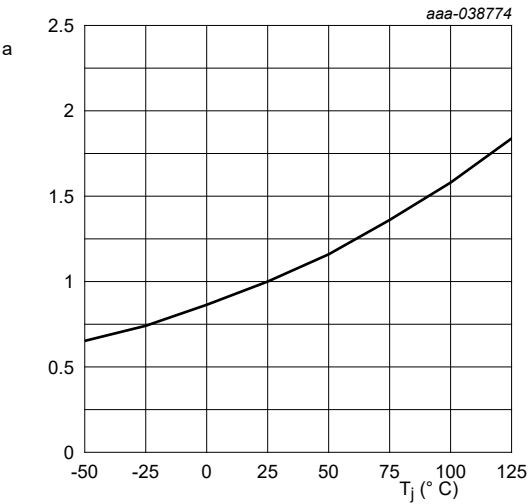
Fig. 7. Output charge as a function of drain-source voltage; typical values

40 V, 12 mOhm bi-directional Gallium Nitride (GaN) FET in a 1.2 mm x 1.7 mm Wafer Level Chip-Scale Package (WLCSP)



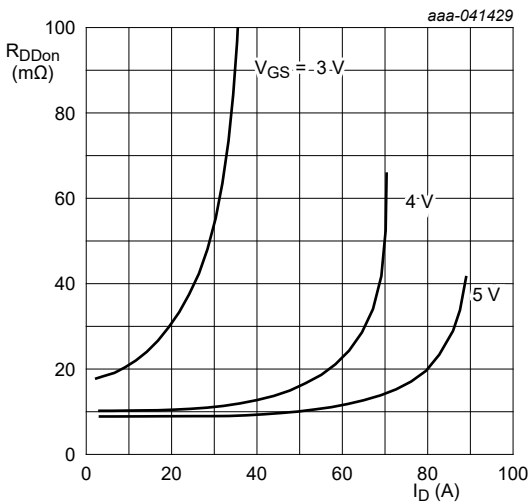
$I_D = 1 \text{ mA}$; $V_{DD} = V_{GD}$

Fig. 8. Gate-drain threshold voltage as a function of junction temperature; typical values



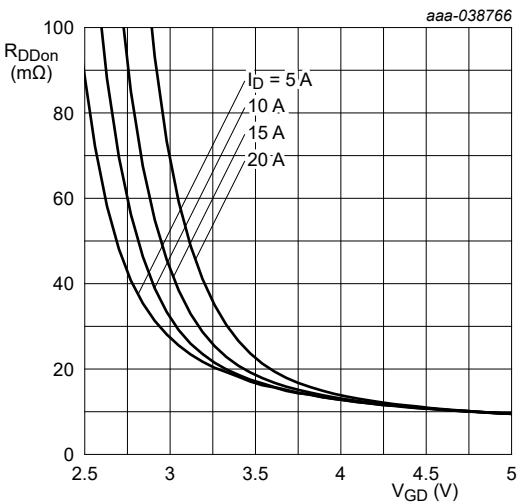
$$a = \frac{R_{DDon}}{R_{DDon}(25^\circ\text{C})}$$

Fig. 9. Normalized drain-drain on-state resistance factor as a function of junction temperature; typical values



$T_j = 25^\circ\text{C}$

Fig. 10. Drain-drain on-state resistance as a function of drain current; typical values



$T_j = 25^\circ\text{C}$

Fig. 11. Drain-drain on-state resistance as a function of gate-drain voltage; typical values

40 V, 12 mOhm bi-directional Gallium Nitride (GaN) FET in a 1.2 mm x 1.7 mm Wafer Level Chip-Scale Package (WLCSP)

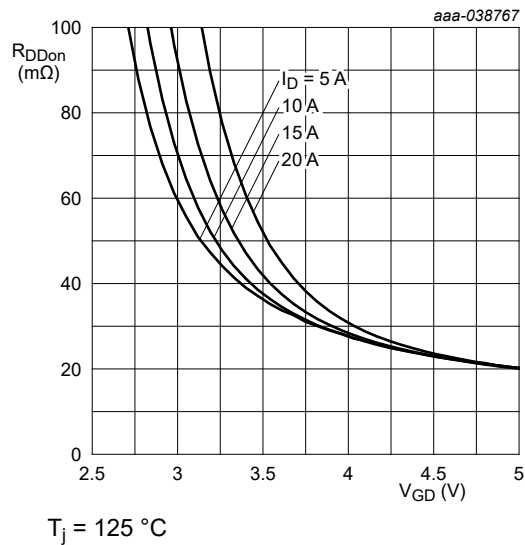


Fig. 12. Drain-drain on-state resistance as a function of gate-drain voltage; typical values

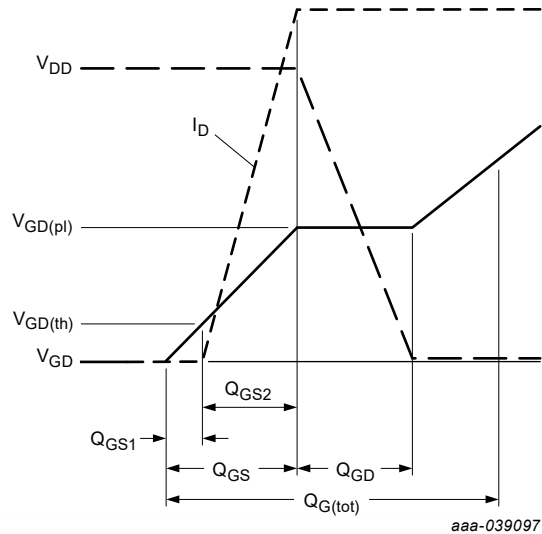


Fig. 13. Gate charge waveform definitions

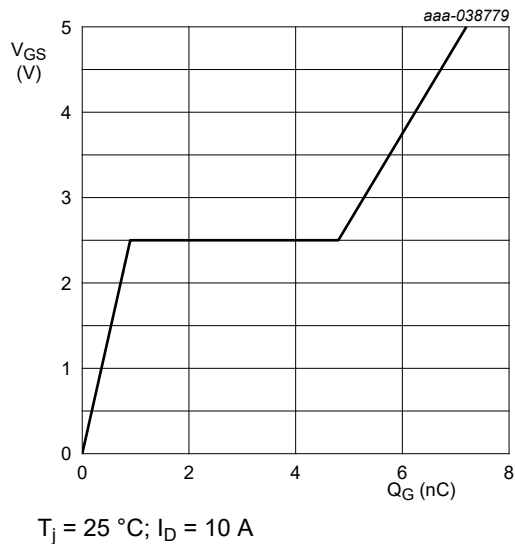


Fig. 14. Gate-source voltage as a function of gate charge; typical values

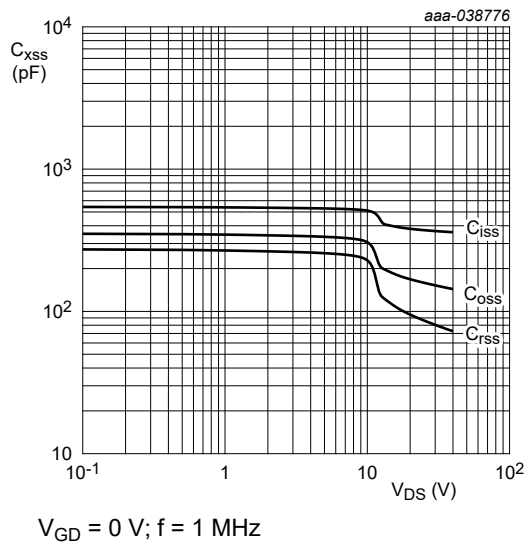


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

40 V, 12 mOhm bi-directional Gallium Nitride (GaN) FET in a 1.2 mm x 1.7 mm Wafer Level Chip-Scale Package (WLCSP)

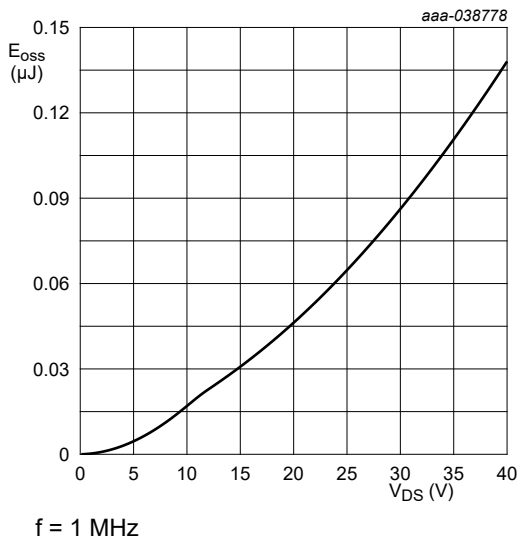


Fig. 16. C_{oss} stored energy as a function of drain-source voltage; typical values

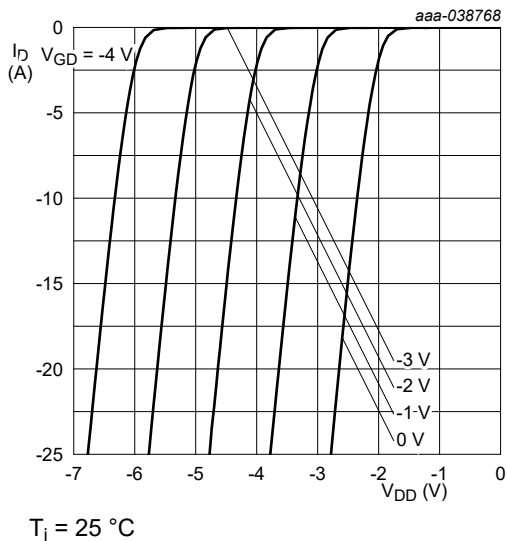


Fig. 17. Reverse drain current as a function of drain-drain voltage; typical values

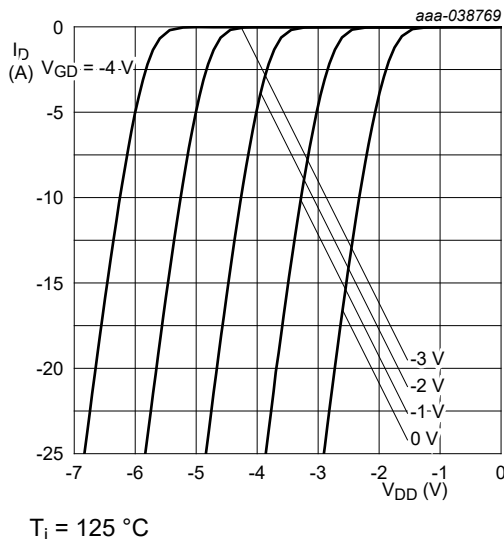


Fig. 18. Reverse drain current as a function of drain-drain voltage; typical values

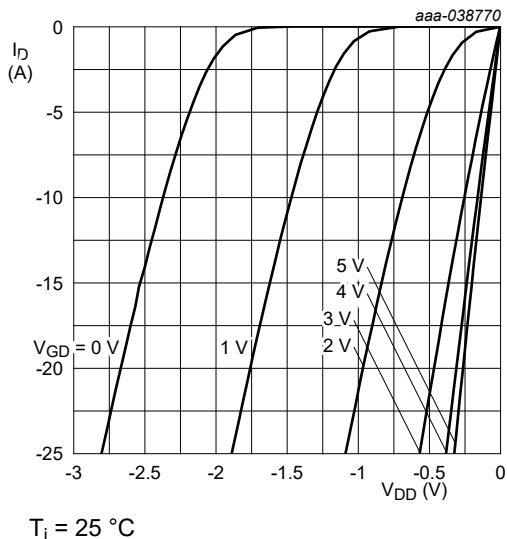
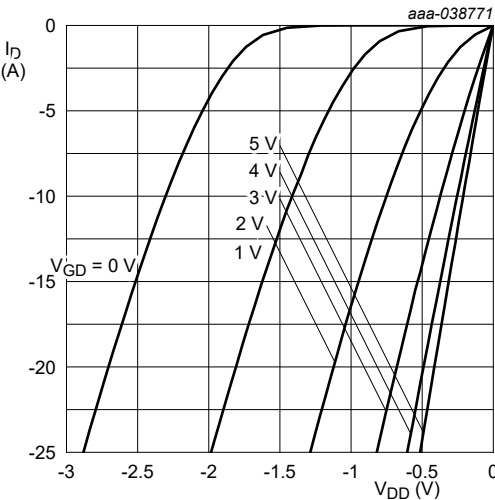


Fig. 19. Reverse drain current as a function of drain-drain voltage; typical values

40 V, 12 mOhm bi-directional Gallium Nitride (GaN) FET in a 1.2 mm x 1.7 mm Wafer Level Chip-Scale Package (WLCSP)



$T_j = 125\text{ }^{\circ}\text{C}$

Fig. 20. Reverse drain current as a function of drain-drain voltage; typical values

11. Package outline

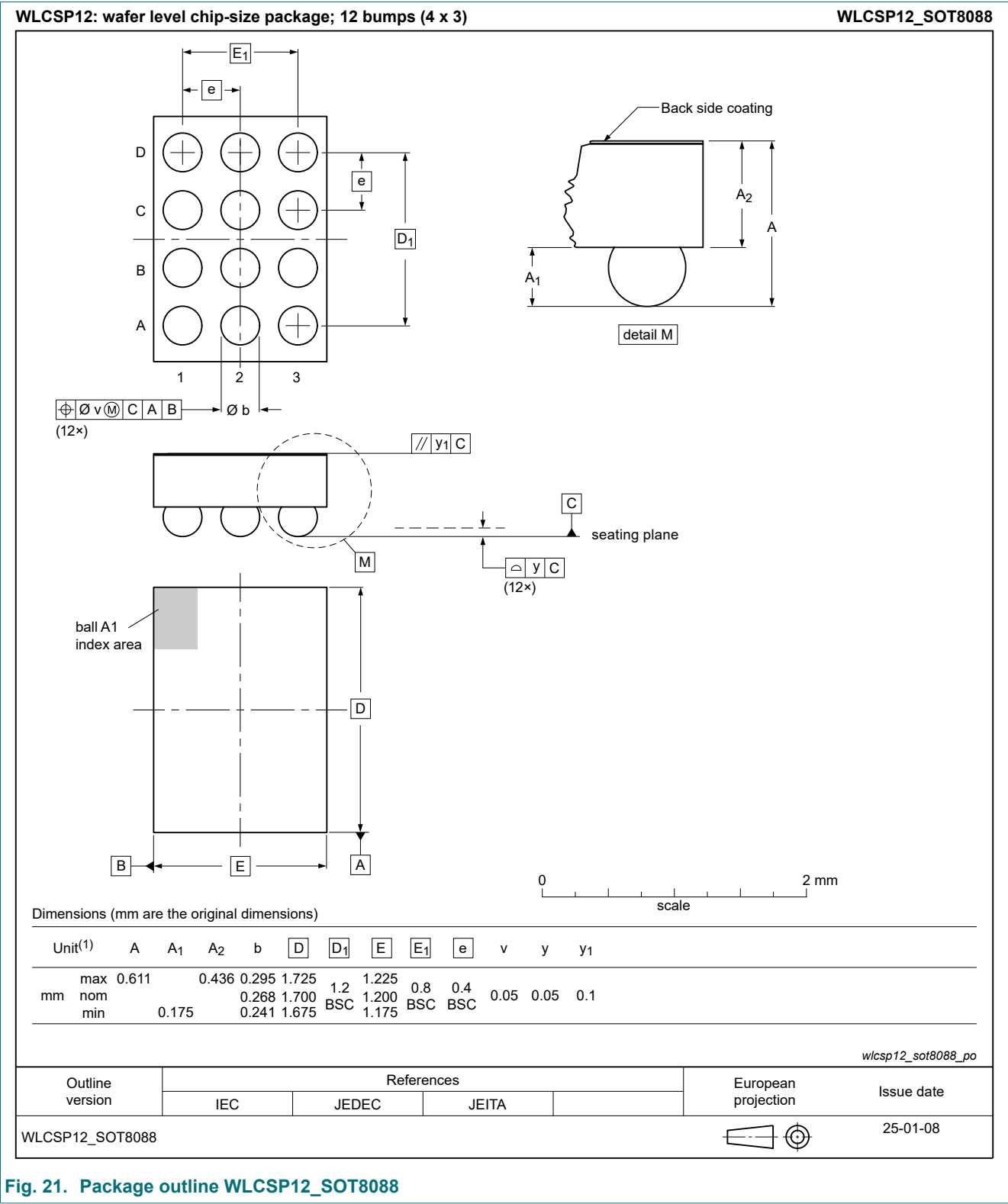
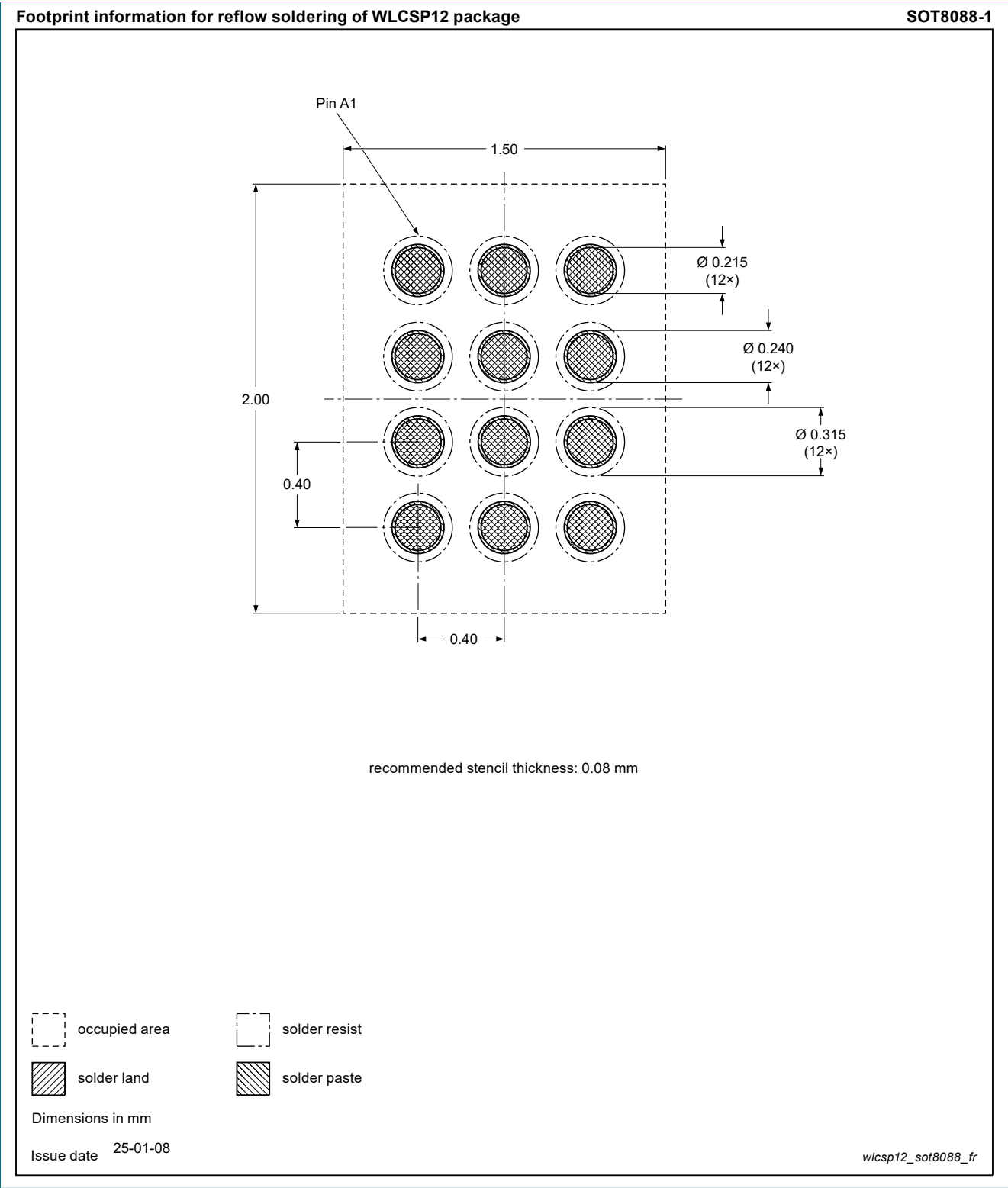


Fig. 21. Package outline WLCSP12_SOT8088

12. Soldering



40 V, 12 mOhm bi-directional Gallium Nitride (GaN) FET in a 1.2 mm x 1.7 mm Wafer Level Chip-Scale Package (WL CSP)

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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