1. General description

Single, logic level, N-channel MOSFET in LFPAK56 using Application specific (ASFET) Enhanced SOA technology. This product has been designed and qualified to AEC-Q101 for use in linear mode in airbag applications.

2. Features and benefits

- Fully automotive qualified to AEC-Q101 at 175 °C
- Enhanced SOA technology for improved linear mode performance
- LFPAK copper clip package technology:
  - High robustness and current handling capability
  - Gull wing leads for easy AOI inspection and exceptional board level reliability

3. Applications

- 12 V automotive systems
- Airbag squib voltage regulator MOSFET

4. Quick reference data

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DS}$</td>
<td>drain-source voltage</td>
<td>$25 \degree C \leq T_j \leq 175 \degree C$</td>
<td>-</td>
<td>-</td>
<td>60</td>
<td>V</td>
</tr>
<tr>
<td>$I_D$</td>
<td>drain current</td>
<td>$V_{GS} = 10 , V$; $T_{mb} = 25 \degree C$; [Fig. 2]</td>
<td>-</td>
<td>-</td>
<td>110</td>
<td>A</td>
</tr>
<tr>
<td>$P_{tot}$</td>
<td>total power dissipation</td>
<td>$T_{mb} = 25 \degree C$; [Fig. 1]</td>
<td>-</td>
<td>-</td>
<td>194</td>
<td>W</td>
</tr>
</tbody>
</table>

**Static characteristics**

- $R_{DSon}$ | drain-source on-state resistance | $V_{GS} = 10 \, V$; $I_D = 25 \, A$; $T_j = 25 \degree C$; [Fig. 13] | 3.1 | 4.4 | 5.6 | mΩ |

**Dynamic characteristics**

- $Q_{GD}$ | gate-drain charge | $I_D = 25 \, A$; $V_{DS} = 48 \, V$; $V_{GS} = 4.5 \, V$; $T_j = 25 \degree C$; [Fig. 15; Fig. 16] | - | 18.2 | 36.4 | nC |

[1] 110 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
5. Pinning information

Table 2. Pinning information

<table>
<thead>
<tr>
<th>Pin</th>
<th>Symbol</th>
<th>Description</th>
<th>Simplified outline</th>
<th>Graphic symbol</th>
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<tbody>
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<td>1</td>
<td>S</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>S</td>
<td>source</td>
<td></td>
<td></td>
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<tr>
<td>3</td>
<td>S</td>
<td>source</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>G</td>
<td>gate</td>
<td></td>
<td></td>
</tr>
<tr>
<td>mb</td>
<td>D</td>
<td>mounting base; connected to drain</td>
<td>LFPAK56; Power-SO8 (SOT669)</td>
<td></td>
</tr>
</tbody>
</table>

6. Ordering information

Table 3. Ordering information

<table>
<thead>
<tr>
<th>Type number</th>
<th>Package</th>
<th>Description</th>
<th>Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>BUK9Y8R8-60EL</td>
<td>LFPAK56; Power-SO8</td>
<td>plastic, single-ended surface-mounted package; 4 terminals</td>
<td>SOT669</td>
</tr>
</tbody>
</table>

7. Marking

Table 4. Marking codes

<table>
<thead>
<tr>
<th>Type number</th>
<th>Marking code</th>
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</thead>
<tbody>
<tr>
<td>BUK9Y8R8-60EL</td>
<td>98E860L</td>
</tr>
</tbody>
</table>

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). $T_j = 25$ °C unless otherwise stated.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DS}$</td>
<td>drain-source voltage</td>
<td>$25 \degree C \leq T_j \leq 175 \degree C$</td>
<td>-</td>
<td>60</td>
<td>V</td>
</tr>
<tr>
<td>$V_{GS}$</td>
<td>gate-source voltage</td>
<td>DC; $T_j \leq 175 \degree C$</td>
<td>-10</td>
<td>10</td>
<td>V</td>
</tr>
<tr>
<td>$P_{tot}$</td>
<td>total power dissipation</td>
<td>$T_{mb} = 25 \degree C$; Fig. 1</td>
<td>-</td>
<td>194</td>
<td>W</td>
</tr>
<tr>
<td>$I_D$</td>
<td>drain current</td>
<td>$V_{GS} = 10 V$; $T_{mb} = 25 \degree C$; Fig. 2; $V_{GS} = 10 V$; $T_{mb} = 100 \degree C$; Fig. 2</td>
<td>[1] -</td>
<td>110</td>
<td>A</td>
</tr>
<tr>
<td>$I_{DM}$</td>
<td>peak drain current</td>
<td>pulsed; $t_p \leq 10 \mu s$; $T_{mb} = 25 \degree C$; Fig. 3; Fig. 4</td>
<td>-</td>
<td>493</td>
<td>A</td>
</tr>
<tr>
<td>$T_{stg}$</td>
<td>storage temperature</td>
<td></td>
<td>-55</td>
<td>175</td>
<td>°C</td>
</tr>
<tr>
<td>$T_j$</td>
<td>junction temperature</td>
<td></td>
<td>-55</td>
<td>175</td>
<td>°C</td>
</tr>
</tbody>
</table>

Source-drain diode

- $I_S$: source current; $T_{mb} = 25 \degree C$; $I_S = 110$ A
- $I_{SM}$: peak source current; pulsed; $t_p \leq 10 \mu s$; $T_{mb} = 25 \degree C$; $I_{SM} = 493$ A

Avalanche ruggedness

- $E_{DS(AlS)}$: non-repetitive drain-source avalanche energy; $E_{DS(AlS)} = 62.3$ A; $V_{sup} \leq 60$ V; $R_{GS} = 50$ Ω; $V_{GS} = 10$ V; $T_{j(init)} = 25 \degree C$; unclamped; $t_p = 76$ μs; Fig. 5 | [2] [3] - 195 | mJ   |
Single N-channel 60 V, 5.6 mOhm logic level MOSFET in LFPAK56 using Enhanced SOA technology

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{AS}$</td>
<td>non-repetitive avalanche current</td>
<td>$V_{sup} \leq 60$ V; $V_{GS} = 10$ V; $T_{j(init)} = 25$ °C; $R_{GS} = 50$ Ω; Fig. 5</td>
<td>[2] [3]</td>
<td>62.3</td>
<td>A</td>
</tr>
</tbody>
</table>

[1] 110 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

[2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.


[4] Protected by 100% test.

Fig. 1. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\%$$

Fig. 2. Continuous drain current as a function of mounting base temperature

$V_{GS} \geq 10$ V

(1) 110 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25$ °C; $I_{DM}$ is a single pulse
Nexperia

Single N-channel 60 V, 5.6 mOhm logic level MOSFET in LFPAK56 using Enhanced SOA technology

\[ T_{mb} = 125 \, ^{\circ}C; \, I_{DM} \text{ is a single pulse} \]

Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

\[ (1) \, T_{j\text{(init)}} = 25 \, ^{\circ}C; \, (2) \, T_{j\text{(init)}} = 150 \, ^{\circ}C; \, (3) \, \text{Repetitive Avalanche} \]

Fig. 5. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{th(j-mb)} )</td>
<td>thermal resistance from junction to mounting base</td>
<td>Fig. 6</td>
<td>-</td>
<td>0.69</td>
<td>0.77</td>
<td>K/W</td>
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</table>
Fig. 6. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{(BR)DSS}$</td>
<td>drain-source breakdown voltage</td>
<td>$I_D = 250 \mu A; V_{GS} = 0 \text{ V}; T_J = 25 \degree C$</td>
<td>60</td>
<td>66</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_D = 250 \mu A; V_{GS} = 0 \text{ V}; T_J = -40 \degree C$</td>
<td>-</td>
<td>62.2</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_D = 250 \mu A; V_{GS} = 0 \text{ V}; T_J = -55 \degree C$</td>
<td>54</td>
<td>61.2</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>$V_{GS(th)}$</td>
<td>gate-source threshold voltage</td>
<td>$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_J = 25 \degree C$; Fig. 11; Fig. 12</td>
<td>1.4</td>
<td>1.8</td>
<td>2.1</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_J = -55 \degree C$; Fig. 12</td>
<td>-</td>
<td>-</td>
<td>2.45</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_J = 175 \degree C$; Fig. 12</td>
<td>0.5</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>$I_{DSS}$</td>
<td>drain leakage current</td>
<td>$V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; T_J = 25 \degree C$</td>
<td>-</td>
<td>0.023</td>
<td>1</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; T_J = 175 \degree C$</td>
<td>-</td>
<td>68</td>
<td>500</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{GSS}$</td>
<td>gate leakage current</td>
<td>$V_{GS} = 10 \text{ V}; V_{DS} = 0 \text{ V}; T_J = 25 \degree C$</td>
<td>-</td>
<td>2</td>
<td>100</td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_J = 25 \degree C$</td>
<td>-</td>
<td>2</td>
<td>100</td>
<td>nA</td>
</tr>
<tr>
<td>$R_{DS(on)}$</td>
<td>drain-source on-state resistance</td>
<td>$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_J = 25 \degree C$; Fig. 13</td>
<td>3.1</td>
<td>4.4</td>
<td>5.6</td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_J = 105 \degree C$; Fig. 14</td>
<td>4.7</td>
<td>7</td>
<td>9</td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_J = 125 \degree C$; Fig. 14</td>
<td>5.2</td>
<td>7.7</td>
<td>10</td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_J = 175 \degree C$; Fig. 14</td>
<td>6.4</td>
<td>9.7</td>
<td>12.7</td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_J = 25 \degree C$; Fig. 13</td>
<td>4.5</td>
<td>6.5</td>
<td>8.6</td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
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<td>$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_J = 105 \degree C$; Fig. 14</td>
<td>4.5</td>
<td>6.5</td>
<td>8.6</td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_J = 125 \degree C$; Fig. 14</td>
<td>6.7</td>
<td>10</td>
<td>13.7</td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_J = 125 \degree C$; Fig. 14</td>
<td>7.3</td>
<td>11</td>
<td>15.2</td>
<td>mΩ</td>
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<tr>
<td></td>
<td></td>
<td>$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_J = 175 \degree C$; Fig. 14</td>
<td>9</td>
<td>13.5</td>
<td>19.1</td>
<td>mΩ</td>
</tr>
</tbody>
</table>
Symbol | Parameter | Conditions | Min | Typ | Max | Unit
---|---|---|---|---|---|---
$R_G$ | gate resistance | $f = 1$ MHz; $T_j = 25$ °C | - | 2.24 | - | Ω

**Dynamic characteristics**

$Q_{G(tot)}$ | total gate charge | $I_D = 25$ A; $V_{DS} = 48$ V; $V_{GS} = 4.5$ V; $T_j = 25$ °C; [Fig. 15; Fig. 16] | - | 43 | 60 | nC
$Q_{GS}$ | gate-source charge | $I_D = 25$ A; $V_{DS} = 48$ V; $V_{GS} = 10$ V; $T_j = 25$ °C; [Fig. 15; Fig. 16] | - | 88 | 123 | nC
$Q_{GD}$ | gate-drain charge | $T_j = 25$ °C; [Fig. 15; Fig. 16] | - | 12 | 18 | nC
$C_{iss}$ | input capacitance | $V_{DS} = 25$ V; $V_{GS} = 0$ V; $f = 1$ MHz; | - | 4782 | 6695 | pF
$C_{oss}$ | output capacitance | $T_j = 25$ °C; [Fig. 17] | - | 412 | 494 | pF
$C_{rss}$ | reverse transfer capacitance | - | 224 | 307 | pF
$t_{d(on)}$ | turn-on delay time | $V_{DS} = 48$ V; $R_G = 1.92$ Ω; $V_{GS} = 5$ V; $R_G(\text{ext}) = 5$ Ω; $T_j = 25$ °C | - | 22 | - | ns
$t_r$ | rise time | - | 55 | - | ns
$t_{d(off)}$ | turn-off delay time | - | 56 | - | ns
$t_f$ | fall time | - | 42 | - | ns
$g_{fs}$ | transfer conductance | $V_{DS} = 8$ V; $I_D = 25$ A; $T_j = 25$ °C; [Fig. 9] | - | 80 | - | S

**Source-drain diode**

$V_{SD}$ | source-drain voltage | $I_S = 25$ A; $V_{GS} = 0$ V; $T_j = 25$ °C; [Fig. 18] | - | 0.81 | 1 | V
$t_{rr}$ | reverse recovery time | $I_S = 25$ A; $dI_S/dt = -100$ A/µs; $V_{GS} = 0$ V; $V_{DS} = 30$ V; $T_j = 25$ °C; [Fig. 19] | - | 30 | - | ns
$Q_r$ | recovered charge | [1] | - | 33 | - | nC

[1] includes capacitive recovery

---

Fig. 7. **Output characteristics; drain current as a function of drain-source voltage; typical values**

Fig. 8. **Drain-source on-state resistance as a function of gate-source voltage; typical values**
Single N-channel 60 V, 5.6 mOhm logic level MOSFET in LFPAK56 using Enhanced SOA technology

Fig. 9. Forward transconductance as a function of drain current; typical values

\( T_j = 25 \, ^\circ C; \, V_{DS} = 8 \, V \)

Fig. 10. Transfer characteristics; drain current as a function of gate-source voltage; typical values

\( V_{DS} = 8 \, V \)

Fig. 11. Sub-threshold drain current as a function of gate-source voltage

\( T_j = 25 \, ^\circ C; \, V_{DS} = 5 \, V \)

Fig. 12. Gate-source threshold voltage as a function of junction temperature

\( I_D = 1 \, mA; \, V_{DS} = V_{GS} \)
Single N-channel 60 V, 5.6 mOhm logic level MOSFET in LFPAK56 using Enhanced SOA technology

Fig. 13. Drain-source on-state resistance as a function of drain current; typical values

Fig. 14. Normalized drain-source on-state resistance factor as a function of junction temperature

Fig. 15. Gate-source voltage as a function of gate charge; typical values

Fig. 16. Gate charge waveform definitions
**Fig. 17.** Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

\( V_{GS} = 0 \text{ V}; \ f = 1 \text{ MHz} \)

**Fig. 18.** Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

\( V_{GS} = 0 \text{ V} \)

**Fig. 19.** Reverse recovery timing definition
11. Package outline

Plastic single-ended surface-mounted package (LFPAK56; Power-SO8; 4 leads) SOT669

Fig. 20. Package outline LFPAK56; Power-SO8 (SOT669)
12. Legal information

## Data sheet status

<table>
<thead>
<tr>
<th>Document status</th>
<th>Product status</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>[1][2]</td>
<td>[3]</td>
<td></td>
</tr>
</tbody>
</table>

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**Product data sheet** 8 April 2022

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This document contains data from the preliminary specification.

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This document contains the product specification.
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