1. General description

Single, logic level, N-channel MOSFET in LFPAK56 using Application specific (ASFET) Enhanced SOA technology. This product has been designed and qualified to AEC-Q101 for use in linear mode in airbag applications.

2. Features and benefits

- Fully automotive qualified to AEC-Q101 at 175 °C
- Enhanced SOA technology for improved linear mode performance
- LFPAK copper clip package technology:
  - High robustness and current handling capability
  - Gull wing leads for easy AOI inspection and exceptional board level reliability

3. Applications

- 12 V automotive systems
- Airbag squib voltage regulator MOSFET

4. Quick reference data

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
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</thead>
<tbody>
<tr>
<td>V$_{DS}$</td>
<td>drain-source voltage</td>
<td>25 °C ≤ T$_j$ ≤ 175 °C</td>
<td>-</td>
<td>-</td>
<td>60</td>
<td>V</td>
</tr>
<tr>
<td>I$_D$</td>
<td>drain current</td>
<td>V$<em>{GS}$ = 10 V; T$</em>{mb}$ = 25 °C; Fig. 2</td>
<td>[1]</td>
<td>-</td>
<td>125</td>
<td>A</td>
</tr>
<tr>
<td>P$_{tot}$</td>
<td>total power dissipation</td>
<td>T$_{mb}$ = 25 °C; Fig. 1</td>
<td>-</td>
<td>-</td>
<td>238.4</td>
<td>W</td>
</tr>
</tbody>
</table>

**Static characteristics**

- $R_{Dson}$: drain-source on-state resistance
  - $V_{GS} = 10$ V; $I_D = 25$ A; $T_j = 25$ °C; Fig. 13
  - 2.5 | 3.6 | 4.5 | mΩ

**Dynamic characteristics**

- $Q_{GD}$: gate-drain charge
  - $I_D = 25$ A; $V_{DS} = 48$ V; $V_{GS} = 4.5$ V; $T_j = 25$ °C; Fig. 15; Fig. 16
  - - | 22 | 44 | nC

[1] 125 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
5. Pinning information

Table 2. Pinning information

<table>
<thead>
<tr>
<th>Pin</th>
<th>Symbol</th>
<th>Description</th>
<th>Simplified outline</th>
<th>Graphic symbol</th>
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<tr>
<td>1</td>
<td>S</td>
<td>source</td>
<td></td>
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<td>2</td>
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<td>S</td>
<td>source</td>
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<tr>
<td>4</td>
<td>G</td>
<td>gate</td>
<td></td>
<td></td>
</tr>
<tr>
<td>mb</td>
<td>D</td>
<td>mounting base; connected to drain</td>
<td><img src="image" alt="Simplified outline" /></td>
<td><img src="image" alt="Graphic symbol" /></td>
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</table>

6. Ordering information

Table 3. Ordering information

<table>
<thead>
<tr>
<th>Type number</th>
<th>Package</th>
<th>Description</th>
<th>Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>BUK9Y7R0-60EL</td>
<td>LFPAK56; Power-SO8</td>
<td>plastic, single-ended surface-mounted package; 4 terminals</td>
<td>SOT669</td>
</tr>
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</table>

7. Marking

Table 4. Marking codes

<table>
<thead>
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<th>Type number</th>
<th>Marking code</th>
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</thead>
<tbody>
<tr>
<td>BUK9Y7R0-60EL</td>
<td>97E060L</td>
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</table>

8. Limiting values

Table 5. Limiting values

*In accordance with the Absolute Maximum Rating System (IEC 60134). Tj = 25 °C unless otherwise stated.*

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDS</td>
<td>drain-source voltage</td>
<td>25 °C ≤ Tj ≤ 175 °C</td>
<td>-</td>
<td>60</td>
<td>V</td>
</tr>
<tr>
<td>VGS</td>
<td>gate-source voltage</td>
<td>DC; Tj ≤ 175 °C</td>
<td>-10</td>
<td>10</td>
<td>V</td>
</tr>
<tr>
<td>Ptot</td>
<td>total power dissipation</td>
<td>Tmb = 25 °C; Fig. 1</td>
<td>-</td>
<td>238.4</td>
<td>W</td>
</tr>
<tr>
<td>ID</td>
<td>drain current</td>
<td>VGS = 10 V; Tmb = 25 °C; Fig. 2</td>
<td>-1</td>
<td>125</td>
<td>A</td>
</tr>
<tr>
<td>IDM</td>
<td>peak drain current</td>
<td>pulsed; tp ≤ 10 µs; Tmb = 25 °C; Fig. 3; Fig. 4</td>
<td>-</td>
<td>612</td>
<td>A</td>
</tr>
<tr>
<td>Tstg</td>
<td>storage temperature</td>
<td></td>
<td>-55</td>
<td>175</td>
<td>°C</td>
</tr>
<tr>
<td>Tj</td>
<td>junction temperature</td>
<td></td>
<td>-55</td>
<td>175</td>
<td>°C</td>
</tr>
</tbody>
</table>

**Source-drain diode**

| I_S    | source current                         | Tmb = 25 °C                                    | -    | 125  | A    |
| I_SM   | peak source current                    | pulsed; tp ≤ 10 µs; Tmb = 25 °C                | -    | 612  | A    |

**Avalanche ruggedness**

| E_D(AL)S | non-repetitive drain-source avalanche energy | I_D = 73 A; V_sup ≤ 60 V; R_GS = 50 Ω; VGS = 10 V; T_j(init) = 25 °C; unclamped; t_p = 87 µs; Fig. 5 | [2] [3] | 261  | mJ   |
Nexperia

BUK9Y7R0-60EL

Single N-channel 60 V, 4.5 mOhm logic level MOSFET in LFPAK56 using Enhanced SOA technology

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>I(_{AS})</td>
<td>non-repetitive avalanche current</td>
<td>(V_{\text{sup}} \leq 60 \text{ V}; \ V_{\text{GS}} = 10 \text{ V}; \ T_{j\text{(init)}} = 25 ^\circ \text{C}; \</td>
<td>R_{GS} = 50 \Omega; ) Fig. 5</td>
<td>[2] [3]</td>
<td>73</td>
</tr>
</tbody>
</table>

[1] 125 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

[2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.


[4] Protected by 100% test.

---

Fig. 1. Normalized total power dissipation as a function of mounting base temperature

\[
P_{\text{der}} = \frac{P_{\text{tot}}}{P_{\text{tot}(25^\circ \text{C})}} \times 100 \%
\]

---

Fig. 2. Continuous drain current as a function of mounting base temperature

\(V_{\text{GS}} \geq 10 \text{ V}\)

(1) 125 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

---

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

\(T_{\text{mb}} = 25 ^\circ \text{C}; \ I_{\text{DM}} \) is a single pulse
T_{mb} = 125 °C; I_{DM} is a single pulse

Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

(1) T_{j (init)} = 25 °C; (2) T_{j (init)} = 150 °C; (3) Repetitive Avalanche

Fig. 5. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>R_{th(j-mb)}</td>
<td>thermal resistance from junction to mounting base</td>
<td>Fig. 6</td>
<td>-</td>
<td>0.56</td>
<td>0.63</td>
<td>K/W</td>
</tr>
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</table>
Fig. 6. Transient thermal impedance from junction to mounting base as a function of pulse duration

### 10. Characteristics

#### Table 7. Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
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</thead>
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<tr>
<td>$V_{(br)DSS}$</td>
<td>drain-source breakdown voltage</td>
<td>$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 ^\circ C$</td>
<td>60</td>
<td>66</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -40 ^\circ C$</td>
<td>-</td>
<td>62</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 ^\circ C$</td>
<td>54</td>
<td>61.7</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>$V_{GS(th)}$</td>
<td>gate-source threshold voltage</td>
<td>$I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 ^\circ C$; Fig. 11; Fig. 12</td>
<td>1.4</td>
<td>1.75</td>
<td>2.1</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_D = 1 mA; V_{DS}=V_{GS}; T_j = -55 ^\circ C$; Fig. 12</td>
<td>-</td>
<td>-</td>
<td>2.45</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_D = 1 mA; V_{DS}=V_{GS}; T_j = 175 ^\circ C$; Fig. 12</td>
<td>0.5</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>$I_{DSS}$</td>
<td>drain leakage current</td>
<td>$V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 ^\circ C$</td>
<td>-</td>
<td>0.032</td>
<td>1</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DS} = 60 V; V_{GS} = 0 V; T_j = 175 ^\circ C$</td>
<td>-</td>
<td>91</td>
<td>500</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{GSS}$</td>
<td>gate leakage current</td>
<td>$V_{GS} = 10 V; V_{DS} = 0 V; T_j = 25 ^\circ C$</td>
<td>-</td>
<td>2</td>
<td>100</td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25 ^\circ C$</td>
<td>-</td>
<td>2</td>
<td>100</td>
<td>nA</td>
</tr>
<tr>
<td>$R_{DSon}$</td>
<td>drain-source on-state resistance</td>
<td>$V_{GS} = 10 V; I_D = 25 A; T_j = 25 ^\circ C$; Fig. 13</td>
<td>2.5</td>
<td>3.6</td>
<td>4.5</td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{GS} = 10 V; I_D = 25 A; T_j = 105 ^\circ C$; Fig. 14</td>
<td>3.8</td>
<td>5.7</td>
<td>7.3</td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{GS} = 10 V; I_D = 25 A; T_j = 125 ^\circ C$; Fig. 14</td>
<td>4.2</td>
<td>6.3</td>
<td>8.1</td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{GS} = 10 V; I_D = 25 A; T_j = 175 ^\circ C$; Fig. 14</td>
<td>5.2</td>
<td>7.8</td>
<td>10.3</td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 ^\circ C$; Fig. 13</td>
<td>3.6</td>
<td>5.2</td>
<td>7</td>
<td>mΩ</td>
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<tr>
<td></td>
<td></td>
<td>$V_{GS} = 4.5 V; I_D = 25 A; T_j = 105 ^\circ C$; Fig. 14</td>
<td>5.4</td>
<td>8</td>
<td>11</td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{GS} = 4.5 V; I_D = 25 A; T_j = 125 ^\circ C$; Fig. 14</td>
<td>5.9</td>
<td>8.8</td>
<td>12.2</td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{GS} = 4.5 V; I_D = 25 A; T_j = 175 ^\circ C$; Fig. 14</td>
<td>7.2</td>
<td>10.9</td>
<td>15.4</td>
<td>mΩ</td>
</tr>
</tbody>
</table>
## Nexperia

BUK9Y7R0-60EL

Single N-channel 60 V, 4.5 mOhm logic level MOSFET in LFPAK56 using Enhanced SOA technology

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>(R_G)</td>
<td>gate resistance</td>
<td>(f = 1) MHz; (T_j = 25) °C</td>
<td>-</td>
<td>2.39</td>
<td>-</td>
<td>Ω</td>
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### Dynamic characteristics

<table>
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<tr>
<th>Symbol</th>
<th>Parameter Description</th>
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<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
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<tbody>
<tr>
<td>(Q_{G(tot)})</td>
<td>total gate charge</td>
<td>(I_D = 25) A; (V_{DS} = 48) V; (V_{GS} = 4.5) V; (T_j = 25) °C; [Fig. 15; Fig. 16]</td>
<td>-</td>
<td>53</td>
<td>74</td>
<td>nC</td>
</tr>
<tr>
<td>(Q_{GS})</td>
<td>gate-source charge</td>
<td>(I_D = 25) A; (V_{DS} = 48) V; (V_{GS} = 10) V; (T_j = 25) °C; [Fig. 15; Fig. 16]</td>
<td>-</td>
<td>109</td>
<td>152</td>
<td>nC</td>
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<tr>
<td>(Q_{GD})</td>
<td>gate-drain charge</td>
<td>(V_{DS} = 25) V; (V_{GS} = 0) V; (f = 1) MHz; [Fig. 15; Fig. 16]</td>
<td>-</td>
<td>14</td>
<td>22</td>
<td>nC</td>
</tr>
<tr>
<td>(C_{iss})</td>
<td>input capacitance</td>
<td>(V_{DS} = 25) V; (V_{GS} = 0) V; (f = 1) MHz; [Fig. 17]</td>
<td>-</td>
<td>5948</td>
<td>8327</td>
<td>pF</td>
</tr>
<tr>
<td>(C_{oss})</td>
<td>output capacitance</td>
<td>(T_j = 25) °C; [Fig. 17]</td>
<td>-</td>
<td>517</td>
<td>620</td>
<td>pF</td>
</tr>
<tr>
<td>(C_{rss})</td>
<td>reverse transfer capacitance</td>
<td>-</td>
<td>280</td>
<td>383</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>(t_{d(on)})</td>
<td>turn-on delay time</td>
<td>(V_{DS} = 48) V; (R_G = 1.92) Ω; (V_{GS} = 5) V; (R_{G(ext)} = 5) Ω; (T_j = 25) °C</td>
<td>-</td>
<td>27</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{r})</td>
<td>rise time</td>
<td>(R_{G(ext)} = 5) Ω; (T_j = 25) °C</td>
<td>-</td>
<td>67</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{d(off)})</td>
<td>turn-off delay time</td>
<td>(V_{DS} = 48) V; (V_{GS} = 0) V; (dI_S/dt = -100) A/µs; (V_{DS} = 30) V; (T_j = 25) °C; [Fig. 19]</td>
<td>-</td>
<td>53</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>(t_f)</td>
<td>fall time</td>
<td>(V_{DS} = 48) V; (V_{GS} = 0) V; (dI_S/dt = -100) A/µs; (V_{DS} = 30) V; (T_j = 25) °C; [Fig. 19]</td>
<td>-</td>
<td>72</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>(g_{fs})</td>
<td>transfer conductance</td>
<td>(V_{DS} = 8) V; (I_D = 25) A; (T_j = 25) °C; [Fig. 9]</td>
<td>-</td>
<td>90</td>
<td>-</td>
<td>S</td>
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</table>

### Source-drain diode

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{SD})</td>
<td>source-drain voltage</td>
<td>(I_S = 25) A; (V_{GS} = 0) V; (T_j = 25) °C; [Fig. 18]</td>
<td>-</td>
<td>0.81</td>
<td>1</td>
<td>V</td>
</tr>
<tr>
<td>(t_{rr})</td>
<td>reverse recovery time</td>
<td>(I_S = 25) A; (dI_S/dt = -100) A/µs; (V_{GS} = 0) V; (V_{DS} = 30) V; (T_j = 25) °C; [Fig. 19]</td>
<td>-</td>
<td>32</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>(Q_r)</td>
<td>recovered charge</td>
<td>(V_{DS} = 30) V; (T_j = 25) °C; [Fig. 19]</td>
<td>[1]</td>
<td>38.5</td>
<td>-</td>
<td>nC</td>
</tr>
</tbody>
</table>

[1] includes capacitive recovery

### Figures

- **Fig. 7.** Output characteristics; drain current as a function of drain-source voltage; typical values
- **Fig. 8.** Drain-source on-state resistance as a function of gate-source voltage; typical values
Single N-channel 60 V, 4.5 mOhm logic level MOSFET in LFPAK56 using Enhanced SOA technology

Fig. 9. Forward transconductance as a function of drain current; typical values

\[ g_m = \frac{I_D}{V_{DS}} \]

\[ T_j = 25 \, ^\circ C; \, V_{DS} = 8 \, V \]

Fig. 10. Transfer characteristics; drain current as a function of gate-source voltage; typical values

\[ I_D = \frac{V_{GS} - V_{TH}}{R_{GS}} \]

\[ V_{DS} = 8 \, V \]

Fig. 11. Sub-threshold drain current as a function of gate-source voltage

\[ I_D = 10^{-6} \, A \]

\[ V_{GS} = 5 \, V \]

Fig. 12. Gate-source threshold voltage as a function of junction temperature

\[ V_{TH} = \frac{I_D}{n \cdot V_{GS}} \]

\[ T_j = 25 \, ^\circ C; \, V_{DS} = 5 \, V \]

\[ I_D = 1 \, mA \]

\[ V_{GS} = V_{DS} \]
**Fig. 13.** Drain-source on-state resistance as a function of drain current; typical values

\[ R_{DSon} = \begin{cases} 2.6 \text{ mΩ} & \text{at } 2.6 \text{ V} \\ 2.8 \text{ mΩ} & \text{at } 2.8 \text{ V} \\ 3 \text{ mΩ} & \text{at } 3 \text{ V} \end{cases} \]

\[ V_{GS} = 10 \text{ V} \]

\[ T_j = 25 ^\circ C \]

**Fig. 14.** Normalized drain-source on-state resistance factor as a function of junction temperature

\[ a = \frac{R_{DSon}}{R_{DSon}(25^\circ C)} \]

**Fig. 15.** Gate-source voltage as a function of gate charge; typical values

\[ V_{GS} = 10 \text{ V} \]

\[ V_{GS} = 48 \text{ V} \]

\[ V_{GS} = 14 \text{ V} \]

\[ T_j = 25 ^\circ C; \ ID = 25 \text{ A} \]

**Fig. 16.** Gate charge waveform definitions

- \( V_{DS} \)
- \( V_{GS(pl)} \)
- \( V_{GS(th)} \)
- \( V_{GS} \)
- \( Q_{GS1} \)
- \( Q_{GS2} \)
- \( Q_{GD} \)
- \( Q_{G(tot)} \)
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Single N-channel 60 V, 4.5 mOhm logic level MOSFET in LFPAK56 using Enhanced SOA technology

V_{GS} = 0 V; f = 1 MHz

**Fig. 17.** Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

V_{GS} = 0 V

**Fig. 18.** Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

**Fig. 19.** Reverse recovery timing definition
11. Package outline

Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads

Figure 20. Package outline LFPAK56; Power-SO8 (SOT669)
12. Legal information

Data sheet status

<table>
<thead>
<tr>
<th>Document status</th>
<th>Product status</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Objective [short] data sheet</td>
<td>Development</td>
<td>This document contains data from the objective specification for product development.</td>
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