1. General description

Automotive qualified N-channel MOSFET using the latest Trench 9 low ohmic superjunction technology, housed in a robust LFPAK56 package. This product has been fully designed and qualified to meet AEC-Q101 requirements delivering high performance and endurance.

2. Features and benefits

- Fully automotive qualified to AEC-Q101:
  - 175 °C rating suitable for thermally demanding environments
- Trench 9 Superjunction technology:
  - Reduced cell pitch enables enhanced power density and efficiency with lower $R_{DSon}$ in same footprint
  - Improved SOA and avalanche capability compared to standard TrenchMOS
  - Tight $V_{GS(th)}$ limits enable easy paralleling of MOSFETs
- LFPAK Gull Wing leads:
  - High Board Level Reliability absorbing mechanical stress during thermal cycling, unlike traditional QFN packages
  - Visual (AOI) soldering inspection, no need for expensive x-ray equipment
  - Easy solder wetting for good mechanical solder joint
- LFPAK copper clip technology:
  - Improved reliability, with reduced $R_{th}$ and $R_{DSon}$
  - Increases maximum current capability and improved current spreading

3. Applications

- 12 V automotive systems
- Motors, lamps and solenoid control
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

4. Quick reference data

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DS}$</td>
<td>drain-source voltage</td>
<td>$25 , ^\circ C \leq T_j \leq 175 , ^\circ C$</td>
<td>-</td>
<td>-</td>
<td>40</td>
<td>V</td>
</tr>
<tr>
<td>$I_D$</td>
<td>drain current</td>
<td>$V_{GS} = 10 , V; T_{mb} = 25 , ^\circ C; \text{Fig. 2}$</td>
<td>70</td>
<td>A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$P_{tot}$</td>
<td>total power dissipation</td>
<td>$T_{mb} = 25 , ^\circ C; \text{Fig. 1}$</td>
<td>64</td>
<td>W</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Static characteristics

- $R_{DSon}$: $V_{GS} = 10 \, V; I_D = 20 \, A; T_j = 25 \, ^\circ C; \text{Fig. 11}$ | 3.9 | 5.6 | 6.5 | mΩ |
Dynamic characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$Q_{GD}$</td>
<td>gate-drain charge</td>
<td>$I_D = 20 \text{ A}; V_{DS} = 20 \text{ V}; V_{GS} = 4.5 \text{ V};$ $\text{Fig. 13; Fig. 14}$</td>
<td>2.2</td>
<td>4.5</td>
<td></td>
<td>nC</td>
</tr>
</tbody>
</table>

Source-drain diode

| $Q_r$ | recovered charge          | $I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A/µs}; V_{DS} = 0 \text{ V}; V_{DS} = 20 \text{ V};$ $\text{Fig. 17}$ | 9.9 |     |     | nC   |
| $S$   | softness factor           | $I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A/µs}; V_{GS} = 0 \text{ V}; V_{DS} = 20 \text{ V}; T_j = 25 \text{ °C};$ $\text{Fig. 17}$ | 0.75 |     |     |      |

[1] 70A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

5. Pinning information

Table 2. Pinning information

<table>
<thead>
<tr>
<th>Pin</th>
<th>Symbol</th>
<th>Description</th>
<th>Simplified outline</th>
<th>Graphic symbol</th>
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<tbody>
<tr>
<td>1</td>
<td>S</td>
<td>source</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>S</td>
<td>source</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>S</td>
<td>source</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>G</td>
<td>gate</td>
<td></td>
<td></td>
</tr>
<tr>
<td>mb</td>
<td>D</td>
<td>mounting base; connected to drain</td>
<td>LFPAK56; Power-SO8 (SOT669)</td>
<td></td>
</tr>
</tbody>
</table>

6. Ordering information

Table 3. Ordering information

<table>
<thead>
<tr>
<th>Type number</th>
<th>Package</th>
<th>Name</th>
<th>Description</th>
<th>Version</th>
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<tbody>
<tr>
<td>BUK9Y6R5-40H</td>
<td>LFPAK56; Power-SO8</td>
<td>plastic, single-ended surface-mounted package; 4 terminals</td>
<td>SOT669</td>
<td></td>
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7. Marking

Table 4. Marking codes

<table>
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<th>Type number</th>
<th>Marking code</th>
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<tr>
<td>BUK9Y6R5-40H</td>
<td>96H540</td>
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</table>
8. Limiting values

Table 5. Limiting values

*In accordance with the Absolute Maximum Rating System (IEC 60134). \( T_j = 25 \, ^\circ\text{C} \) unless otherwise stated.*

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{DS} )</td>
<td>drain-source voltage</td>
<td>( 25 , ^\circ\text{C} \leq T_j \leq 175 , ^\circ\text{C} )</td>
<td>-</td>
<td>40</td>
<td>V</td>
</tr>
<tr>
<td>( V_{GS} )</td>
<td>gate-source voltage</td>
<td></td>
<td>-20</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>( P_{tot} )</td>
<td>total power dissipation</td>
<td>( T_{mb} = 25 , ^\circ\text{C}; \text{Fig. 1} )</td>
<td>-</td>
<td>64</td>
<td>W</td>
</tr>
<tr>
<td>( I_D )</td>
<td>drain current</td>
<td>( V_{GS} = 10 , V; T_{mb} = 25 , ^\circ\text{C}; \text{Fig. 2} )</td>
<td>[1]</td>
<td>70</td>
<td>A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{GS} = 10 , V; T_{mb} = 100 , ^\circ\text{C} )</td>
<td></td>
<td>50</td>
<td>A</td>
</tr>
<tr>
<td>( I_{DM} )</td>
<td>peak drain current</td>
<td>pulsed; ( t_p \leq 10 , \mu\text{s}; T_{mb} = 25 , ^\circ\text{C}; \text{Fig. 3} )</td>
<td>-</td>
<td>284</td>
<td>A</td>
</tr>
<tr>
<td>( T_{stg} )</td>
<td>storage temperature</td>
<td></td>
<td>-55</td>
<td>175</td>
<td>°C</td>
</tr>
<tr>
<td>( T_j )</td>
<td>junction temperature</td>
<td></td>
<td>-55</td>
<td>175</td>
<td>°C</td>
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</table>

**Source-drain diode**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_S )</td>
<td>source current</td>
<td>( T_{mb} = 25 , ^\circ\text{C} )</td>
<td>-</td>
<td>64</td>
<td>A</td>
</tr>
<tr>
<td>( I_{SM} )</td>
<td>peak source current</td>
<td>pulsed; ( t_p \leq 10 , \mu\text{s}; T_{mb} = 25 , ^\circ\text{C} )</td>
<td>-</td>
<td>284</td>
<td>A</td>
</tr>
</tbody>
</table>

**Avalanche ruggedness**

\[ E_{DS(AL)S} \]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_D )</td>
<td>drain current</td>
<td>( 70 , A; V_{sup} \leq 40 , V; R_{GS} = 50 , \Omega; V_{GS} = 10 , V; T_{j(init)} = 25 , ^\circ\text{C}; ) unclamped; ( \text{Fig. 4} )</td>
<td>[2] [3]</td>
<td>19.3</td>
<td>mJ</td>
</tr>
</tbody>
</table>

[1] 70A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

[2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.


---

**Fig. 1.** Normalized total power dissipation as a function of mounting base temperature

\[
P_{der} = \left( \frac{P_{tot}}{P_{tot}(25\,^\circ\text{C})} \right) \times 100 \%
\]

**Fig. 2.** Continuous drain current as a function of mounting base temperature

\[ V_{GS} \geq 10 \, V \]

(1) 70A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
$T_{mb} = 25 \, ^\circ C; \, I_{DM}$ is a single pulse

**Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

(1) $T_{j\,(init)} = 25 \, ^\circ C$; (2) $T_{j\,(init)} = 150 \, ^\circ C$; (3) Repetitive Avalanche

**Fig. 4. Avalanche rating; avalanche current as a function of avalanche time**
9. Thermal characteristics

Table 6. Thermal characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{\text{th(j-mb)}}$</td>
<td>thermal resistance from junction to mounting base</td>
<td>Fig. 5</td>
<td>-</td>
<td>2.17</td>
<td>2.35</td>
<td>K/W</td>
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</table>

Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{\text{BRDSS}}$</td>
<td>drain-source breakdown voltage</td>
<td>$I_D = 250 \mu A; V_{GS} = 0 \text{ V}; T_J = 25 , ^\circ \text{C}$</td>
<td>40</td>
<td>43</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_D = 250 \mu A; V_{GS} = 0 \text{ V}; T_J = -40 , ^\circ \text{C}$</td>
<td>-</td>
<td>40.5</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_D = 250 \mu A; V_{GS} = 0 \text{ V}; T_J = -55 , ^\circ \text{C}$</td>
<td>36</td>
<td>40</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>$V_{\text{GS(th)}}$</td>
<td>gate-source threshold voltage</td>
<td>$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_J = 25 , ^\circ \text{C}; Fig. 9; Fig. 10 $</td>
<td>1.45</td>
<td>1.77</td>
<td>2.15</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_J = -55 , ^\circ \text{C}; Fig. 10 $</td>
<td>-</td>
<td>-</td>
<td>2.6</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_J = 175 , ^\circ \text{C}; Fig. 10 $</td>
<td>0.7</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>$I_{\text{DSS}}$</td>
<td>drain leakage current</td>
<td>$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_J = 25 , ^\circ \text{C}$</td>
<td>-</td>
<td>0.01</td>
<td>5</td>
<td>$\mu \text{A}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DS} = 16 \text{ V}; V_{GS} = 0 \text{ V}; T_J = 125 , ^\circ \text{C}$</td>
<td>-</td>
<td>0.32</td>
<td>10</td>
<td>$\mu \text{A}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_J = 175 , ^\circ \text{C}$</td>
<td>-</td>
<td>44</td>
<td>500</td>
<td>$\mu \text{A}$</td>
</tr>
<tr>
<td>$I_{\text{GSS}}$</td>
<td>gate leakage current</td>
<td>$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_J = 25 , ^\circ \text{C}$</td>
<td>-</td>
<td>2</td>
<td>100</td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_J = 25 , ^\circ \text{C}$</td>
<td>-</td>
<td>2</td>
<td>100</td>
<td>nA</td>
</tr>
</tbody>
</table>
### Nexperia

**BUK9Y6R5-40H**

N-channel 40 V, 6.5 mΩ logic level MOSFET in LFPAK56

---

**Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit**  
--- | --- | --- | --- | --- | --- | ---  
$R_{D\text{Son}}$ | drain-source on-state resistance | $V_{GS} = 10 \text{ V}; I_D = 20 \text{ A}; T_J = 25 \degree \text{C}$; Fig. 11 | 3.9 | 5.6 | 6.5 | mΩ  
 | | $V_{GS} = 10 \text{ V}; I_D = 20 \text{ A}; T_J = 105 \degree \text{C}$; Fig. 12 | 5.3 | 8.1 | 9.8 | mΩ  
 | | $V_{GS} = 10 \text{ V}; I_D = 20 \text{ A}; T_J = 125 \degree \text{C}$; Fig. 12 | 5.9 | 8.8 | 10.5 | mΩ  
 | | $V_{GS} = 10 \text{ V}; I_D = 20 \text{ A}; T_J = 175 \degree \text{C}$; Fig. 12 | 7.1 | 10.6 | 12.6 | mΩ  
 | | $V_{GS} = 4.5 \text{ V}; I_D = 15 \text{ A}; T_J = 25 \degree \text{C}$; Fig. 11 | 5 | 7.1 | 8.6 | mΩ  
 | | $V_{GS} = 4.5 \text{ V}; I_D = 15 \text{ A}; T_J = 105 \degree \text{C}$; Fig. 12 | 6.9 | 10.1 | 12.9 | mΩ  
 | | $V_{GS} = 4.5 \text{ V}; I_D = 15 \text{ A}; T_J = 125 \degree \text{C}$; Fig. 12 | 7.6 | 11 | 13.9 | mΩ  
 | | $V_{GS} = 4.5 \text{ V}; I_D = 15 \text{ A}; T_J = 175 \degree \text{C}$; Fig. 12 | 9.2 | 13.1 | 16.7 | mΩ  
$R_G$ | gate resistance | $f = 1 \text{ MHz}; T_J = 25 \degree \text{C}$ | 0.3 | 0.7 | 1.8 | Ω  

**Dynamic characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit  
--- | --- | --- | --- | --- | --- | ---  
$Q_{G(\text{tot})}$ | total gate charge | $I_D = 20 \text{ A}; V_{DS} = 20 \text{ V}; V_{GS} = 10 \text{ V}$; Fig. 13; Fig. 14 | - | 21 | 29 | nC  
 | | $I_D = 20 \text{ A}; V_{DS} = 20 \text{ V}; V_{GS} = 4.5 \text{ V}$; Fig. 13; Fig. 14 | - | 9.5 | 13.3 | nC  
$Q_{GS}$ | gate-source charge | $V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$; Fig. 13; Fig. 14 | - | 4.1 | 6.2 | nC  
$Q_{GD}$ | gate-drain charge | $V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$; Fig. 13; Fig. 14 | - | 2.2 | 4.5 | nC  
$C_{iss}$ | output capacitance | $V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$; $T_J = 25 \degree \text{C}$; Fig. 15 | - | 1454 | 2036 | pF  
$C_{oss}$ | reverse transfer capacitance | $V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$; $T_J = 25 \degree \text{C}$; Fig. 15 | - | 383 | 536 | pF  
$C_{rss}$ | reverse transfer capacitance | $V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$; $T_J = 25 \degree \text{C}$; Fig. 15 | - | 54 | 119 | pF  
$t_{d(on)}$ | turn-on delay time | $V_{DS} = 20 \text{ V}; R_L = 1 \text{ Ω}; V_{GS} = 4.5 \text{ V}$; $R_{G(\text{ext})} = 5 \text{ Ω}$ | - | 10 | - | ns  
$t_r$ | rise time | - | 12 | - | ns  
$t_{d(\text{off})}$ | turn-off delay time | - | 10 | - | ns  
$t_f$ | fall time | - | 6.3 | - | ns  

**Source-drain diode**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit  
--- | --- | --- | --- | --- | --- | ---  
$V_{SD}$ | source-drain voltage | $I_S = 20 \text{ A}; V_{GS} = 0 \text{ V}; T_J = 25 \degree \text{C}$; Fig. 16 | - | 0.83 | 1 | V  
$t_r$ | reverse recovery time | $I_S = 20 \text{ A}; \text{d}I_S/\text{d}t = -100 \text{ A/µs}; V_{GS} = 0 \text{ V}$; $V_{DS} = 20 \text{ V}$; Fig. 17 | - | 19 | - | ns  
$Q_r$ | recovered charge | $I_S = 20 \text{ A}; \text{d}I_S/\text{d}t = -100 \text{ A/µs}; V_{GS} = 0 \text{ V}$; $V_{DS} = 20 \text{ V}$; $T_J = 25 \degree \text{C}$; Fig. 17 | - | 9.9 | - | nC  
$S$ | softness factor | $I_S = 20 \text{ A}; \text{d}I_S/\text{d}t = -500 \text{ A/µs}; V_{GS} = 0 \text{ V}$; $V_{DS} = 20 \text{ V}$; $T_J = 25 \degree \text{C}$; Fig. 17 | - | 0.75 | - |  
 | | $I_S = 20 \text{ A}; \text{d}I_S/\text{d}t = -500 \text{ A/µs}; V_{GS} = 0 \text{ V}$; $V_{DS} = 20 \text{ V}$; $T_J = 25 \degree \text{C}$; Fig. 17 | - | 0.62 | - |
Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

Fig. 9. Sub-threshold drain current as a function of gate-source voltage
**Nexperia**

**BUK9Y6R5-40H**

N-channel 40 V, 6.5 mΩ logic level MOSFET in LFPAK56

---

**Fig. 10.** Gate-source threshold voltage as a function of junction temperature

- **Typ**
- **Max**
- **Min**

\[ V_{GS(th)} = V_{GS} \]

**I_D = 1 mA ; V_{DS} = V_{GS}**

**T_j = 25 °C**

**Fig. 11.** Drain-source on-state resistance as a function of drain current; typical values

- **R_{DS(on)}**

\[ R_{DS(on)} = \begin{cases} 2.8 \text{ V} & V_{GS} = 10 \text{ V} \\ 3 \text{ V} & V_{GS} = 10 \text{ V} \\ 3.5 \text{ V} & V_{GS} = 10 \text{ V} \\ 4.5 \text{ V} & V_{GS} = 10 \text{ V} \end{cases} \]

**T_j = 25 °C**

**Fig. 12.** Normalized drain-source on-state resistance factor as a function of junction temperature

\[ a = \frac{R_{DS(on)}}{R_{DS(on)}(25°C)} \]

**Fig. 13.** Gate-source voltage as a function of gate charge; typical values

- **V_{GS}**

\[ V_{GS} = \begin{cases} 10 \text{ V} & V_{DS} = 14 \text{ V} \\ 20 \text{ V} & V_{DS} = 14 \text{ V} \end{cases} \]

**T_j = 25 °C ; I_D = 20 A**

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Fig. 14. Gate charge waveform definitions

Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

Fig. 17. Reverse recovery timing definition
11. Package outline

Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads

SOT669

Dimensions (mm are the original dimensions)

<table>
<thead>
<tr>
<th>Unit(1)</th>
<th>A</th>
<th>A1</th>
<th>A2</th>
<th>A3</th>
<th>b</th>
<th>b2</th>
<th>b3</th>
<th>b4</th>
<th>c</th>
<th>c2</th>
<th>D1(1)</th>
<th>D2(1)</th>
<th>E1(1)</th>
<th>E1(1)</th>
<th>e</th>
<th>H</th>
<th>L</th>
<th>L1</th>
<th>L2</th>
<th>w</th>
<th>y</th>
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</thead>
<tbody>
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<td>max</td>
<td>1.20</td>
<td>0.15</td>
<td>1.10</td>
<td>0.50</td>
<td>4.41</td>
<td>2.2</td>
<td>0.9</td>
<td>0.25</td>
<td>0.30</td>
<td>4.10</td>
<td>4.20</td>
<td>5.0</td>
<td>3.3</td>
<td>1.27</td>
<td>6.2</td>
<td>0.85</td>
<td>1.3</td>
<td>1.3</td>
<td>0.25</td>
<td>0.1</td>
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</tr>
<tr>
<td>nom</td>
<td>1.01</td>
<td>0.00</td>
<td>0.95</td>
<td>0.25</td>
<td>3.62</td>
<td>2.0</td>
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Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

Fig. 18. Package outline LFPAK56; Power-SO8 (SOT669)
12. Soldering

Footprint information for reflow soldering

Fig. 19. Reflow soldering footprint for LFPAK56; Power-SO8 (SOT669)
Wave soldering footprint information for LFPAK56 package

Fig. 20. Wave soldering footprint for LFPAK56; Power-SO8 (SOT669)
## 13. Legal information

### Data sheet status

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**Objective [short] data sheet** Development This document contains data from the objective specification for product development.

**Preliminary [short] data sheet** Qualification This document contains data from the preliminary specification.

**Product [short] data sheet** Production This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term "short data sheet" is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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Date of release: 1 May 2020