



# BUK9Y2R8-40H

N-channel 40 V, 2.8 mΩ logic level MOSFET in LFPAK56

10 January 2025

Product data sheet

## 1. General description

Automotive qualified N-channel MOSFET using the latest Trench 9 low ohmic superjunction technology, housed in a robust LFPAK56 package. This product has been fully designed and qualified to meet AEC-Q101 requirements delivering high performance and endurance.

## 2. Features and benefits

- Fully automotive qualified to AEC-Q101:
  - 175 °C rating suitable for thermally demanding environments
- Trench 9 Superjunction technology:
  - Reduced cell pitch enables enhanced power density and efficiency with lower  $R_{DSon}$  in same footprint
  - Improved SOA and avalanche capability compared to standard TrenchMOS
  - Tight  $V_{GS(th)}$  limits enable easy paralleling of MOSFETs
- LFPAK Gull Wing leads:
  - High Board Level Reliability absorbing mechanical stress during thermal cycling, unlike traditional QFN packages
  - Visual (AOI) soldering inspection, no need for expensive x-ray equipment
  - Easy solder wetting for good mechanical solder joint
- LFPAK copper clip technology:
  - Improved reliability, with reduced  $R_{th}$  and  $R_{DSon}$
  - Increases maximum current capability and improved current spreading

## 3. Applications

- 12 V automotive systems
- Motors, lamps and solenoid control
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

## 4. Quick reference data

Table 1. Quick reference data

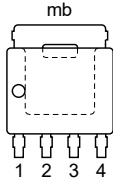
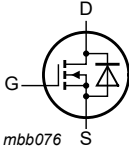
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	40	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}$	[1]	-	120	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}; \text{Fig. 1}$	-	-	172	W
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C}; \text{Fig. 10}$	1.68	2.4	2.8	mΩ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$I_D = 25\text{ A}$ ; $V_{DS} = 20\text{ V}$ ; $V_{GS} = 4.5\text{ V}$ ; <a href="#">Fig. 11</a> ; <a href="#">Fig. 12</a>	-	4.7	9	nC
<b>Source-drain diode</b>						
$Q_r$	recovered charge	$I_S = 25\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ;	-	20.4	-	nC
S	softness factor	$V_{DS} = 20\text{ V}$ ; $T_j = 25\text{ °C}$	-	0.83	-	

[1] 120A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p><b>LPAK56; Power-SO8 (SOT669)</b></p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
<a href="#">BUK9Y2R8-40H</a>	LPAK56; Power-SO8	plastic, single-ended surface-mounted package; 4 terminals	<a href="#">SOT669</a>

## 7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9Y2R8-40H	92H840

## 8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).  $T_j = 25\text{ °C}$  unless otherwise stated.

Symbol	Parameter	Conditions	Min	Max	Unit	
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	40	V	
$V_{GS}$	gate-source voltage		[1]	-20	20	V
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>	-	172	W	
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$	[2]	-	120	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 2</a>	-	600	A	
$T_{stg}$	storage temperature		-55	175	°C	

Symbol	Parameter	Conditions	Min	Max	Unit
$T_j$	junction temperature		-55	175	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25\text{ °C}$	-	120	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$	-	600	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 120\text{ A}$ ; $V_{sup} \leq 40\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; unclamped; <a href="#">Fig. 3</a>	[3] [4]	50	mJ

- [1] Refer to application note AN90001 for further information.
- [2] 120A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [3] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [4] Refer to application note AN10273 for further information.

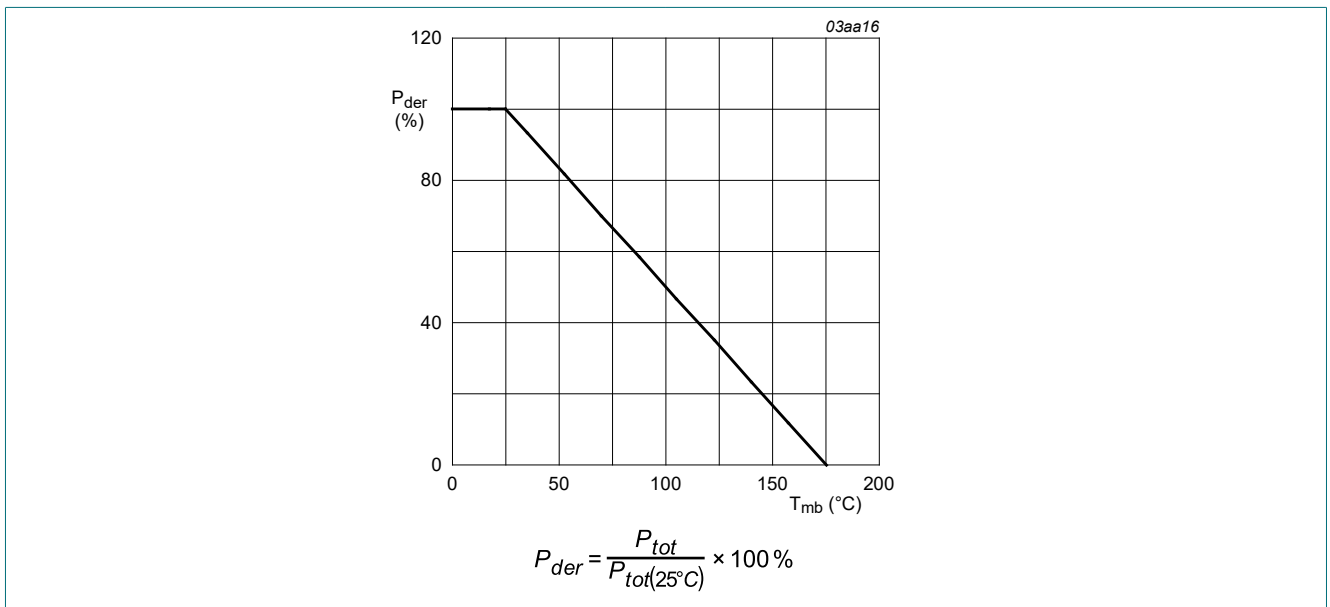


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

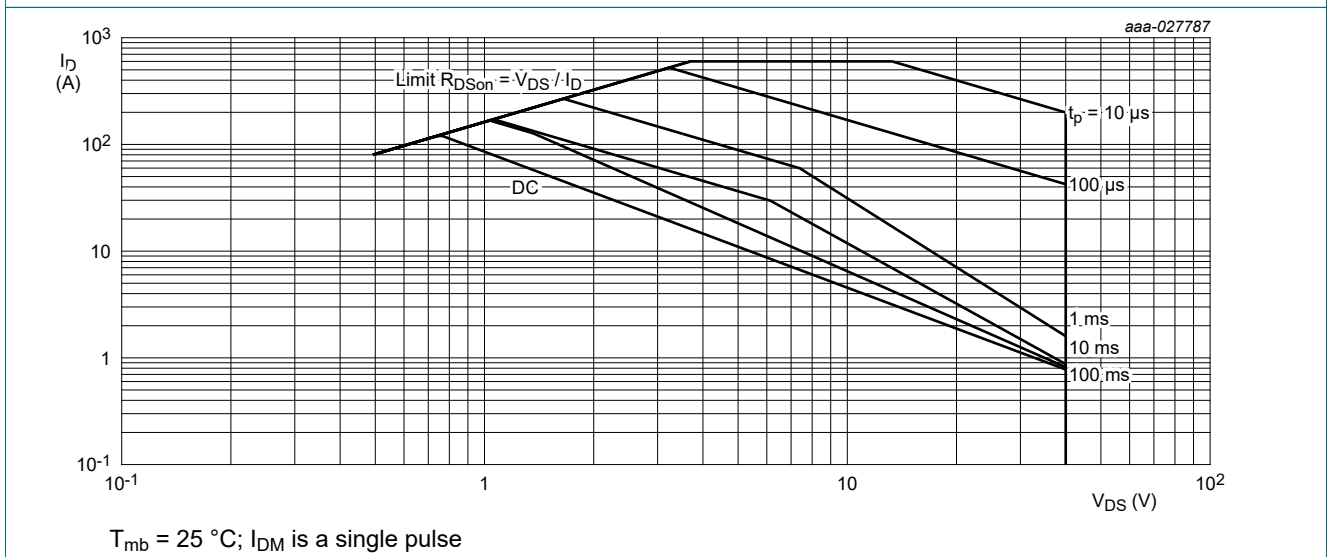
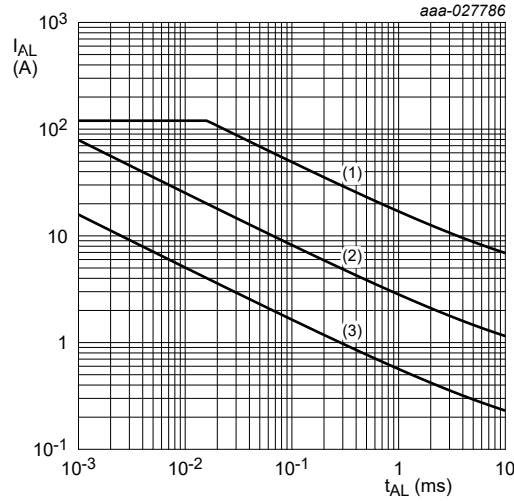


Fig. 2. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



(1)  $T_{j (init)} = 25^\circ\text{C}$ ; (2)  $T_{j (init)} = 150^\circ\text{C}$ ; (3) Repetitive Avalanche

Fig. 3. Avalanche rating; avalanche current as a function of avalanche time

### 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	0.77	0.87	K/W

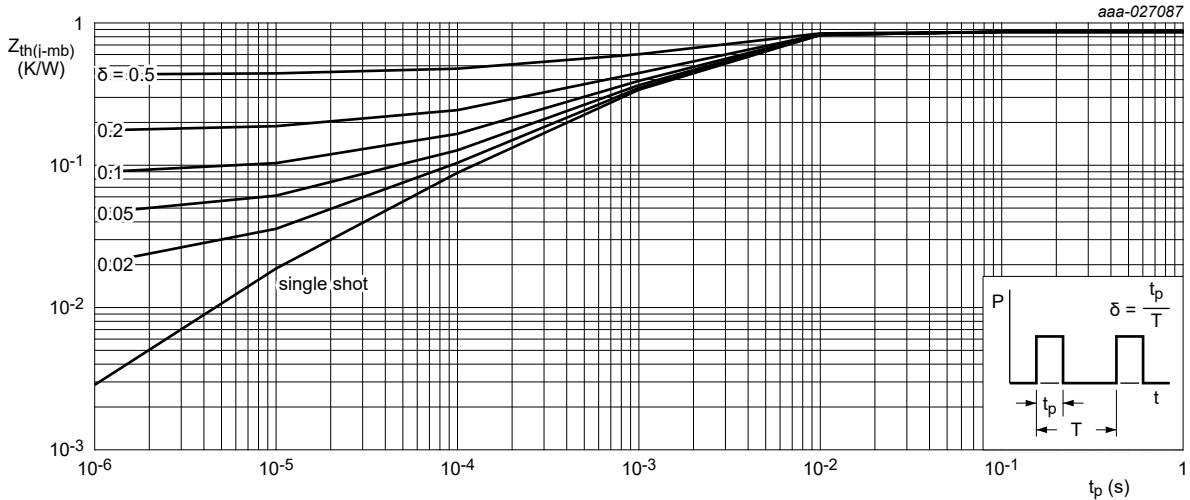


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	40	43	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -40 \text{ }^\circ C$	-	40.5	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	36	40	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ C; \text{ Fig. 8}; \text{ Fig. 9}$	1.35	1.66	2.05	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 175 \text{ }^\circ C; \text{ Fig. 9}$	0.6	-	-	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ C; \text{ Fig. 9}$	-	-	2.5	V
$I_{DSS}$	drain leakage current	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.06	5	$\mu A$
		$V_{DS} = 16 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ C$	-	0.8	10	$\mu A$
		$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ C$	-	108	500	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C; \text{ Fig. 10}$	1.68	2.4	2.8	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 105 \text{ }^\circ C$	2.5	3.6	4.4	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 125 \text{ }^\circ C$	2.7	4	5	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ C$	3.5	4.9	6.2	mΩ
		$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C; \text{ Fig. 10}$	2.1	3	3.9	mΩ
		$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 105 \text{ }^\circ C$	3.1	4.5	6.1	mΩ
		$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 125 \text{ }^\circ C$	3.4	4.9	6.8	mΩ
		$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ C$	4.4	6	8.6	mΩ
$R_G$	gate resistance	$f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$	0.32	0.8	2	Ω
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 20 \text{ V}; V_{GS} = 10 \text{ V}; \text{ Fig. 11}; \text{ Fig. 12}$	-	44	62	nC
		$I_D = 25 \text{ A}; V_{DS} = 20 \text{ V}; V_{GS} = 4.5 \text{ V}; \text{ Fig. 11}; \text{ Fig. 12}$	-	20	28	nC
$Q_{GS}$	gate-source charge		-	8	12.2	nC
$Q_{GD}$	gate-drain charge		-	4.7	9	nC
$C_{iss}$	input capacitance	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C; \text{ Fig. 13}$	-	3101	4341	pF
$C_{oss}$	output capacitance		-	709	992	pF
$C_{riss}$	reverse transfer capacitance		-	112	246	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 20 \text{ V}; R_L = 0.8 \text{ } \Omega; V_{GS} = 4.5 \text{ V}; R_{G(ext)} = 5 \text{ } \Omega$	-	18.9	-	ns
$t_r$	rise time		-	21.6	-	ns
$t_{d(off)}$	turn-off delay time		-	22.5	-	ns
$t_f$	fall time		-	13.2	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C; \text{ Fig. 14}$	-	0.81	1.2	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{rr}$	reverse recovery time	$I_S = 25 \text{ A}; dI_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V}; V_{DS} = 20 \text{ V}; T_J = 25 \text{ }^\circ\text{C}$	-	28.1	-	ns
$Q_r$	recovered charge		-	20.4	-	nC
S	softness factor		$I_S = 25 \text{ A}; dI_S/dt = -500 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V}; V_{DS} = 20 \text{ V}; T_J = 25 \text{ }^\circ\text{C}$	-	0.66	-

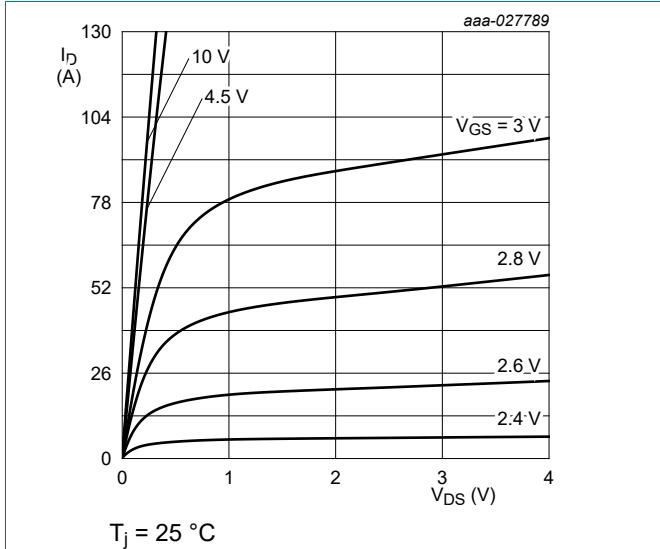


Fig. 5. Output characteristics; drain current as a function of drain-source voltage; typical values

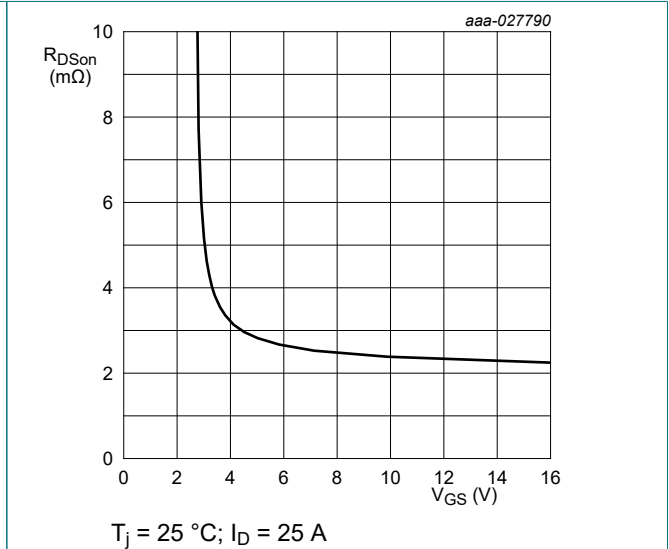


Fig. 6. Drain-source on-state resistance as a function of gate-source voltage; typical values

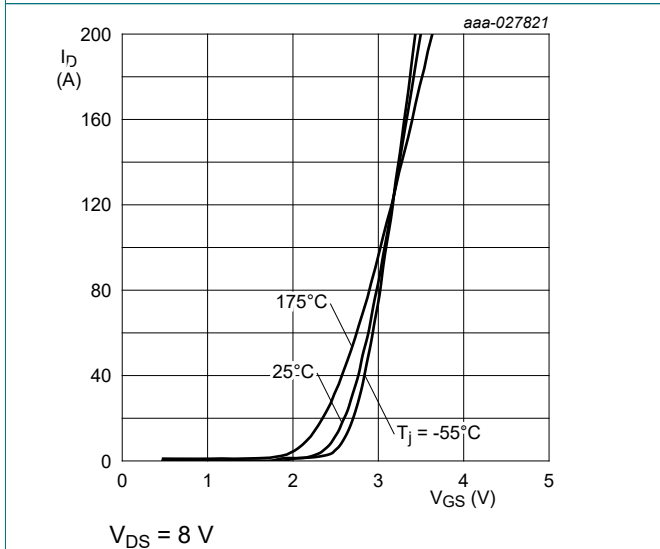


Fig. 7. Transfer characteristics; drain current as a function of gate-source voltage; typical values

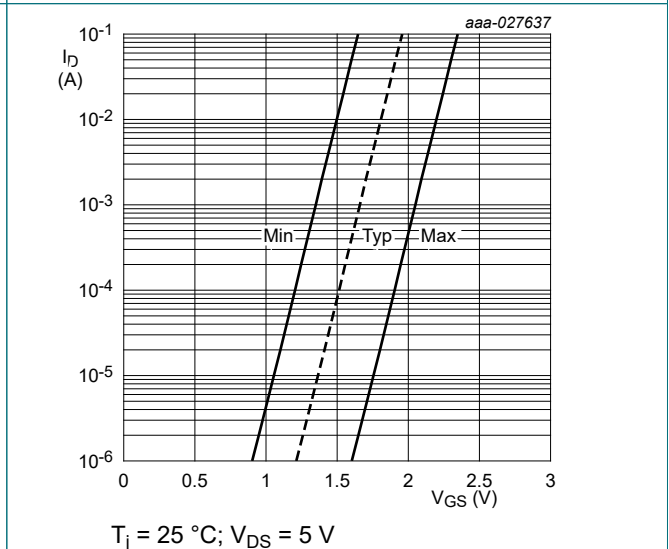


Fig. 8. Sub-threshold drain current as a function of gate-source voltage

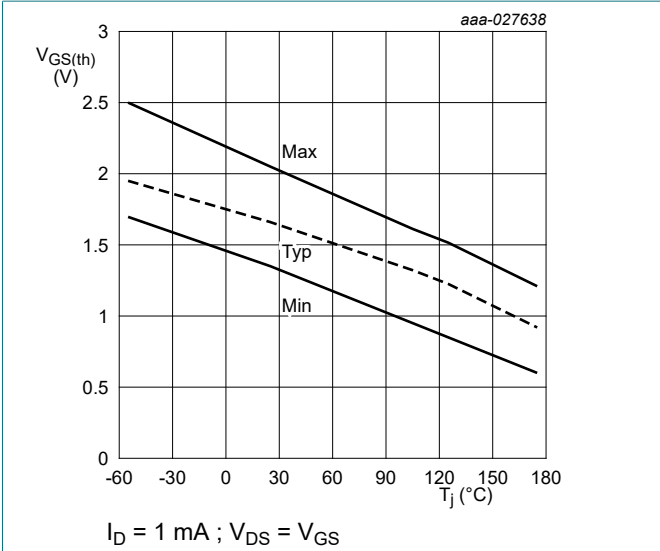


Fig. 9. Gate-source threshold voltage as a function of junction temperature

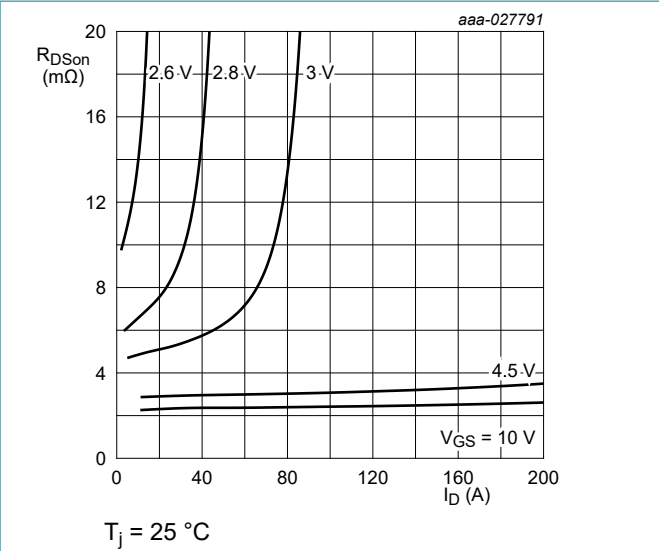


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values

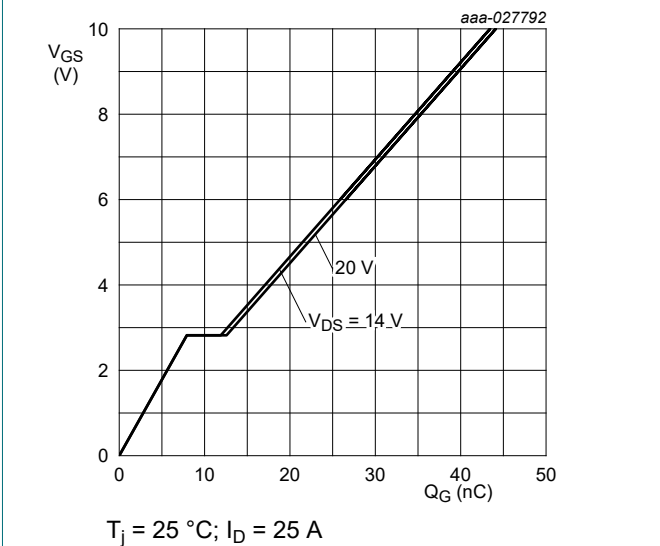


Fig. 11. Gate-source voltage as a function of gate charge; typical values

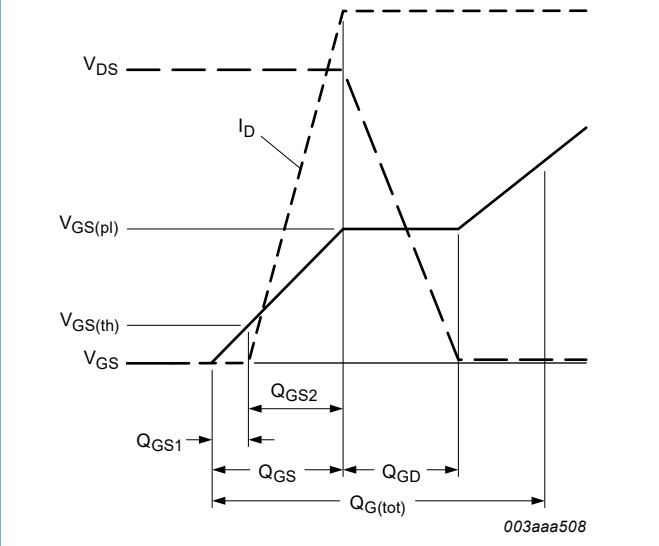
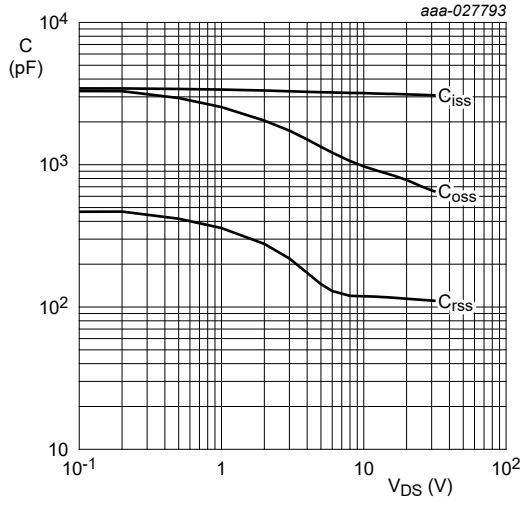
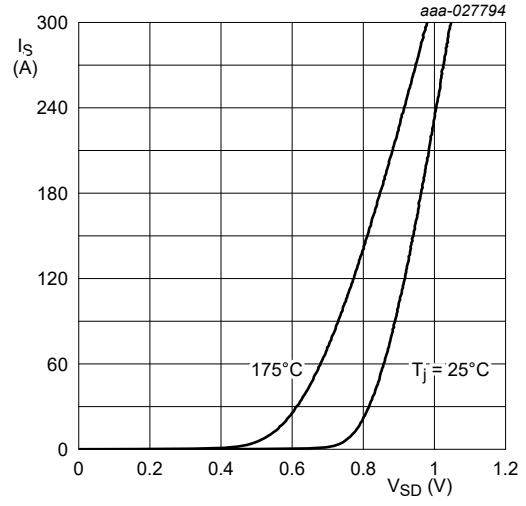


Fig. 12. Gate charge waveform definitions



V<sub>GS</sub> = 0 V; f = 1 MHz

**Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



V<sub>GS</sub> = 0 V

**Fig. 14. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values**



11. Package outline

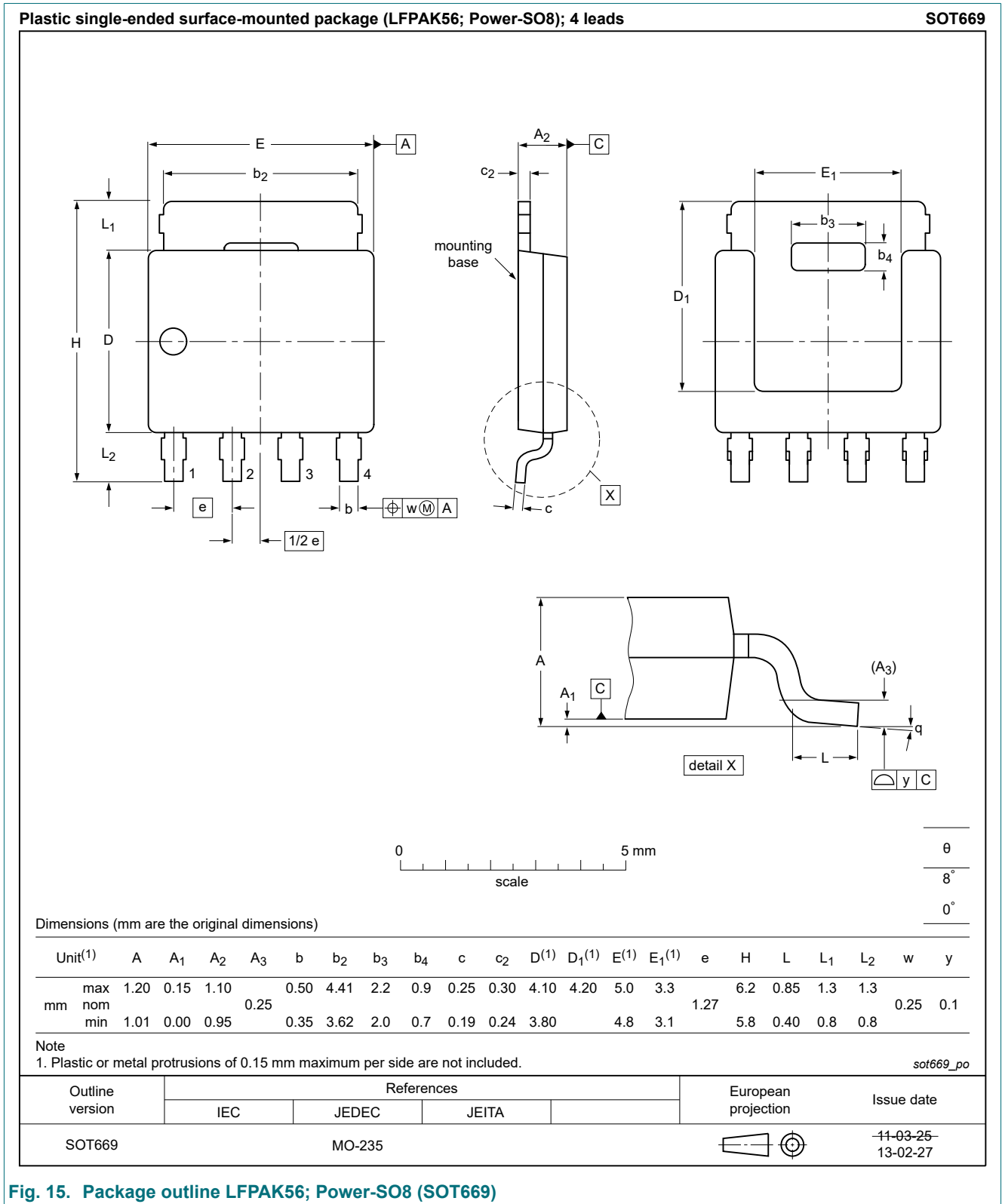


Fig. 15. Package outline LPAK56; Power-SO8 (SOT669)

## 12. Soldering

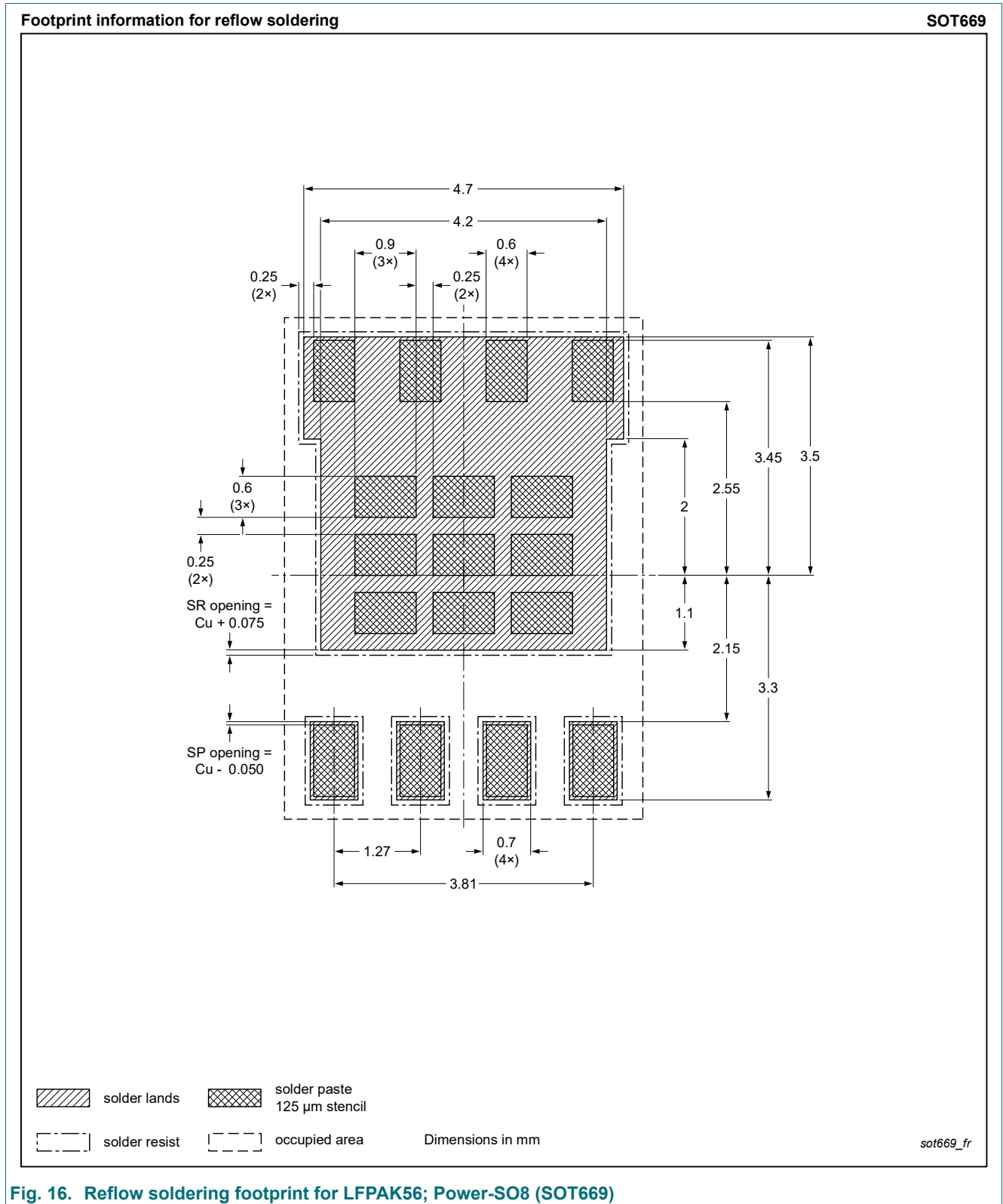
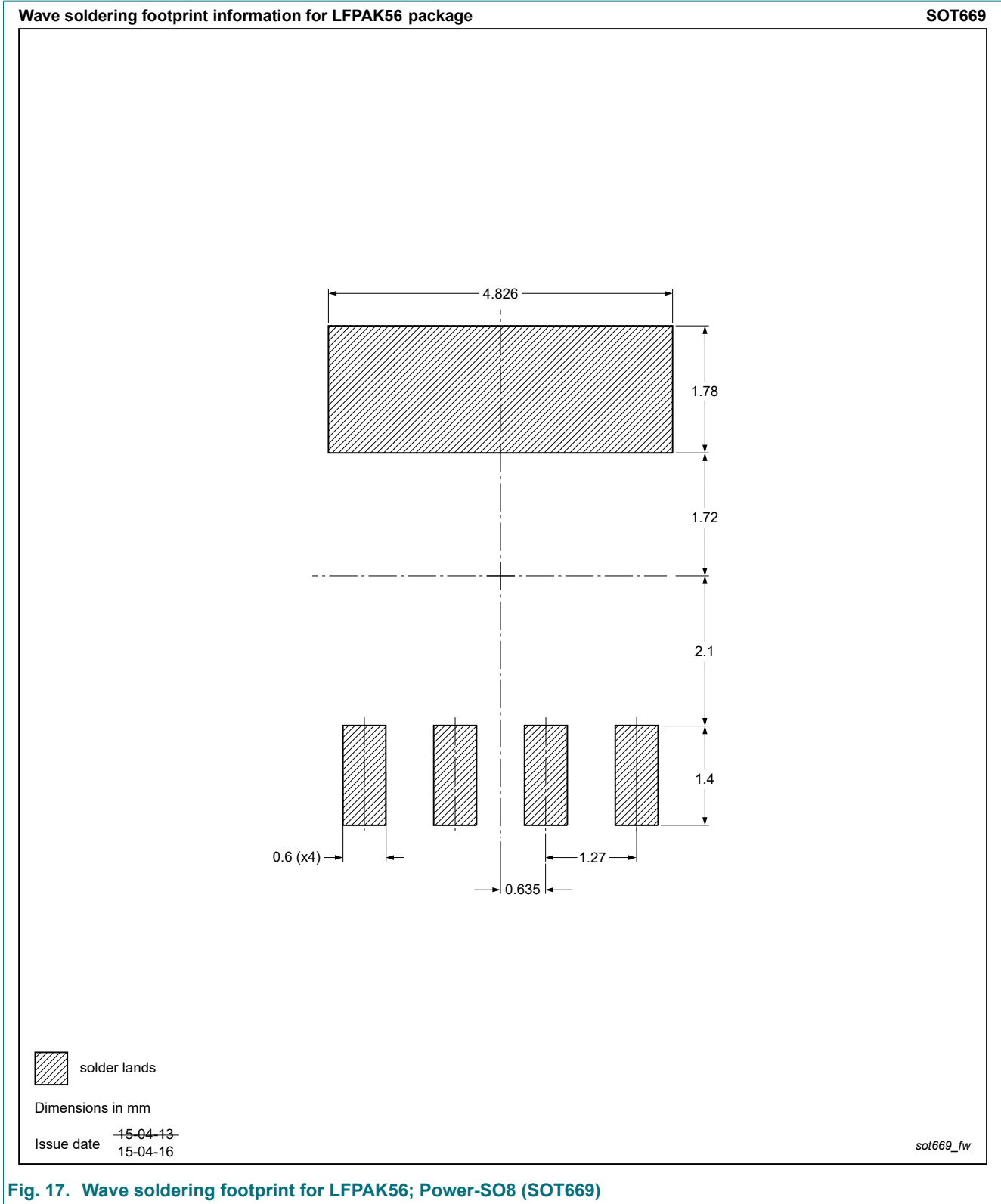


Fig. 16. Reflow soldering footprint for LFPAK56; Power-SO8 (SOT669)



## 13. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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