



BUK9K35-100L

Dual N-channel 100 V, 35 mOhm logic level MOSFET in LFAK56D

12 December 2024

Product data sheet

1. General description

Dual N-channel logic level MOSFET in an LFAK56D (Dual Power-SO8) package. This product has been designed and qualified to AEC-Q101 standard for use in high performance automotive applications.

2. Features and benefits

- Dual MOSFET – two silicon dies in one LFAK56D package for significant space saving
- Trench12 MOSFET technology
- Efficient switching with soft body-diode recovery
- Automotive qualified to AEC-Q101 at 175 °C
- Side-wettable flanks for robust solder joints and automatic optical inspection

3. Applications

- 12 V, 24 V and 48 V automotive systems
- Motor, lighting, and solenoid control
- Transmission control
- LED lighting
- Circuit protection

4. Quick reference data

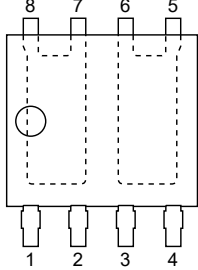
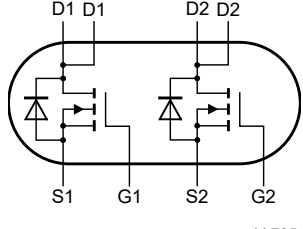
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Limiting values FET1 and FET2						
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	100	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}; \text{Fig. 2}$	[1]	-	23	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}; \text{Fig. 1}$	-	-	42	W
Static characteristics FET1 and FET2						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 5\text{ A}; T_j = 25\text{ °C}; \text{Fig. 11}$	19	24	35	mΩ
Dynamic characteristics FET1 and FET2						
Q_{GD}	gate-drain charge	$I_D = 5\text{ A}; V_{DS} = 50\text{ V}; V_{GS} = 5\text{ V}; T_j = 25\text{ °C}; \text{Fig. 13}; \text{Fig. 14}$	0.93	3.1	6.8	nC

[1] 23 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 <p>LFAK56D; Dual LFAK (SOT1205)</p>	 <p>mbk725</p>
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9K35-100L	LFAK56D; Dual LFAK	plastic, single ended surface mounted package (LFAK56D); 8 leads	SOT1205

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9K35-100L	9351HL

8. Limiting values

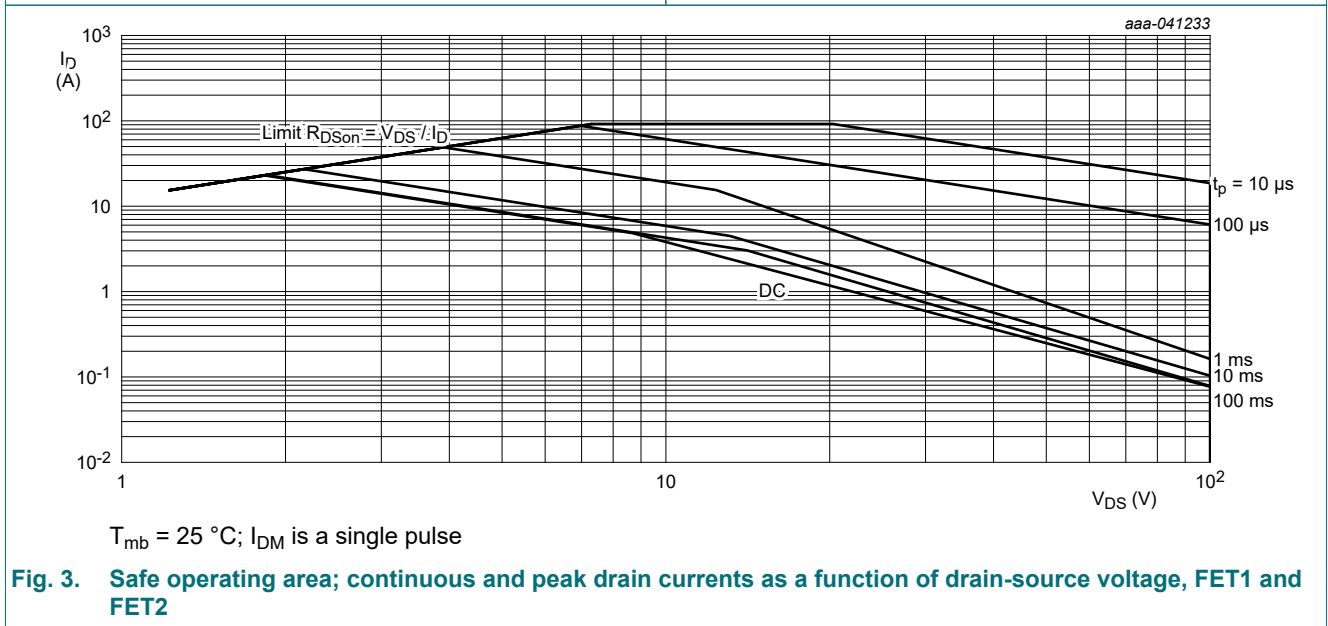
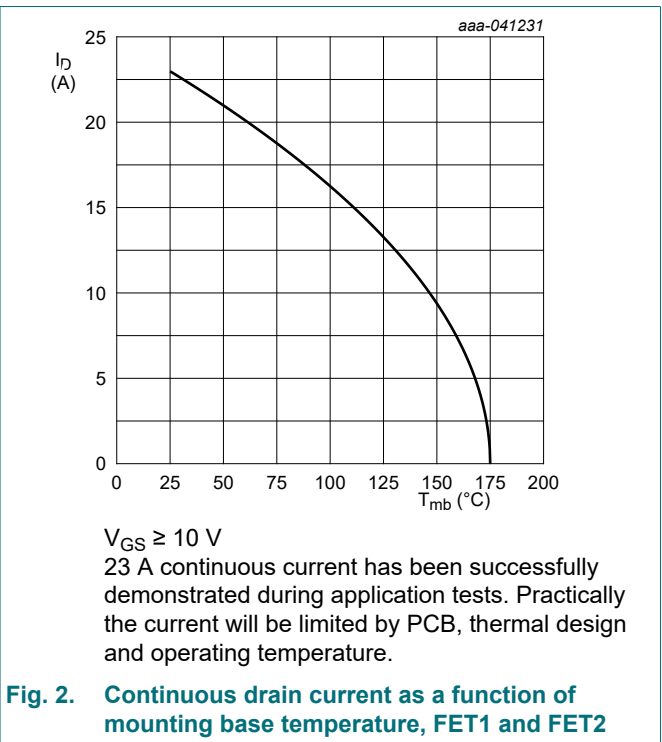
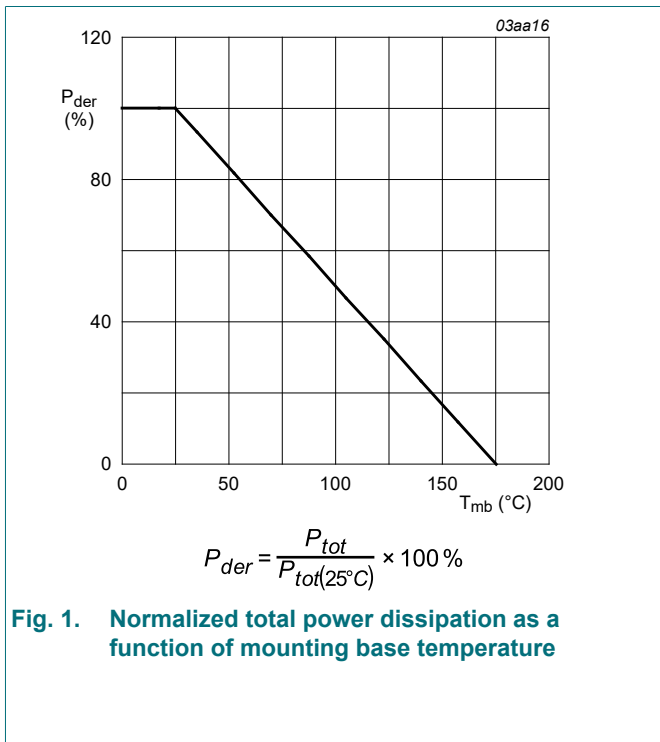
Table 5. Limiting values

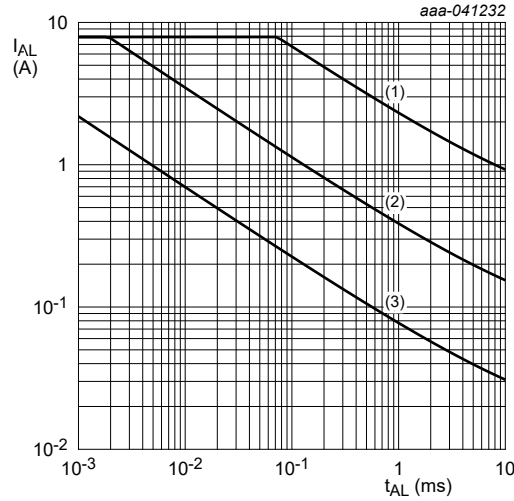
In accordance with the Absolute Maximum Rating System (IEC 60134). $T_j = 25\text{ °C}$ unless otherwise stated.

Symbol	Parameter	Conditions	Min	Max	Unit	
Limiting values FET1 and FET2						
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	100	V	
V_{GS}	gate-source voltage	[1]	-20	20	V	
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	42	W	
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[2]	-	23	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 2		-	16	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 3	-	92	A	
T_{stg}	storage temperature		-55	175	°C	
T_j	junction temperature		-55	175	°C	
Source-drain diode FET1 and FET2						
I_S	source current	$T_{mb} = 25\text{ °C}$	-	23	A	
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$	-	92	A	

Symbol	Parameter	Conditions	Min	Max	Unit	
Avalanche ruggedness FET1 and FET2						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 7.9 \text{ A}$; $V_{sup} \leq 100 \text{ V}$; $R_{GS} = 50 \text{ } \Omega$; $V_{GS} = 5 \text{ V}$; $T_{j(\text{init})} = 25 \text{ }^\circ\text{C}$; unclamped; $t_{AL} = 73 \text{ } \mu\text{s}$; Fig. 4	[3] [4]	-	37.4	mJ
I_{AS}	non-repetitive avalanche current	$V_{sup} = 100 \text{ V}$; $V_{GS} = 5 \text{ V}$; $T_{j(\text{init})} = 25 \text{ }^\circ\text{C}$; $R_{GS} = 50 \text{ } \Omega$; Fig. 4	[3] [4]	-	7.9	A

- [1] Refer to application note AN90001 for further information.
- [2] 23 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [3] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [4] Refer to application note AN10273 for further information.





(1) $T_{j\text{ (init)}} = 25\text{ °C}$; (2) $T_{j\text{ (init)}} = 150\text{ °C}$; (3) Repetitive Avalanche

Fig. 4. Avalanche rating; avalanche current as a function of avalanche time, FET1 and FET2

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	2.28	3.57	K/W

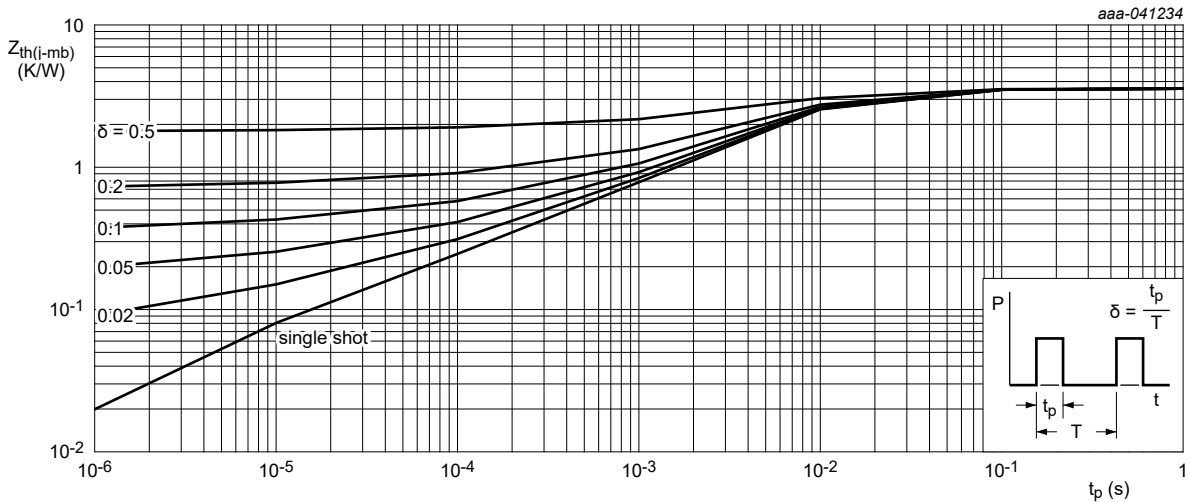


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration, FET1 and FET2

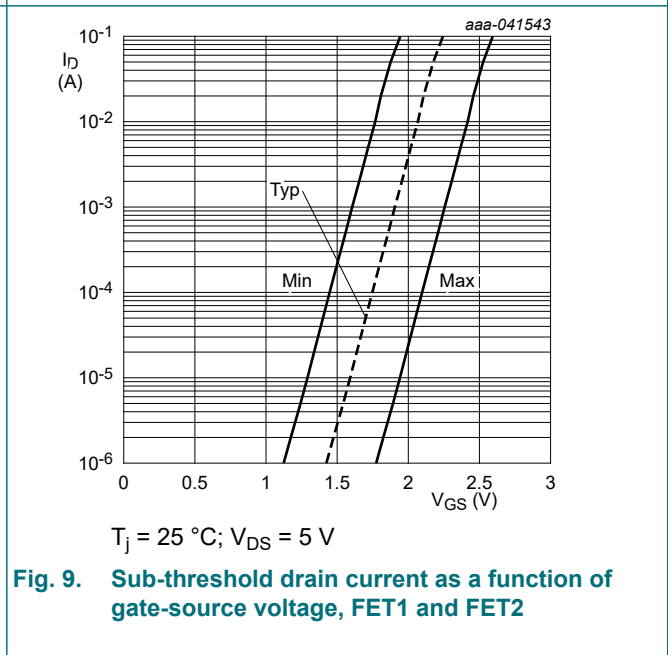
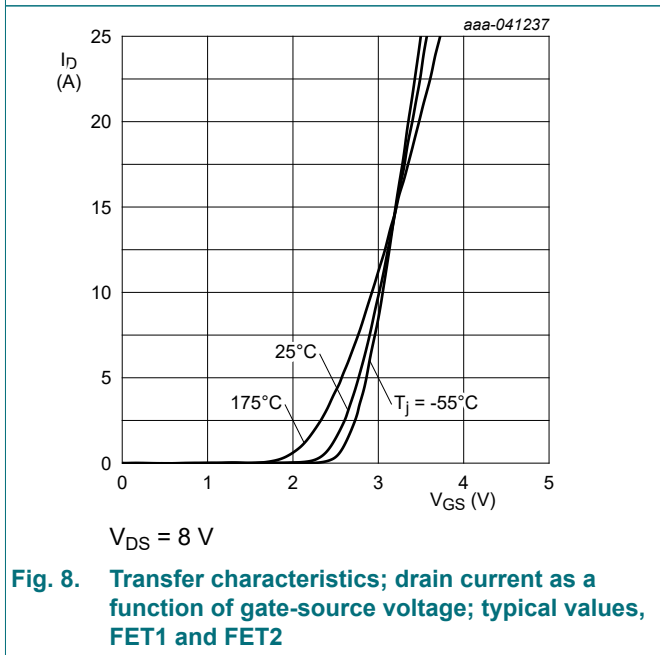
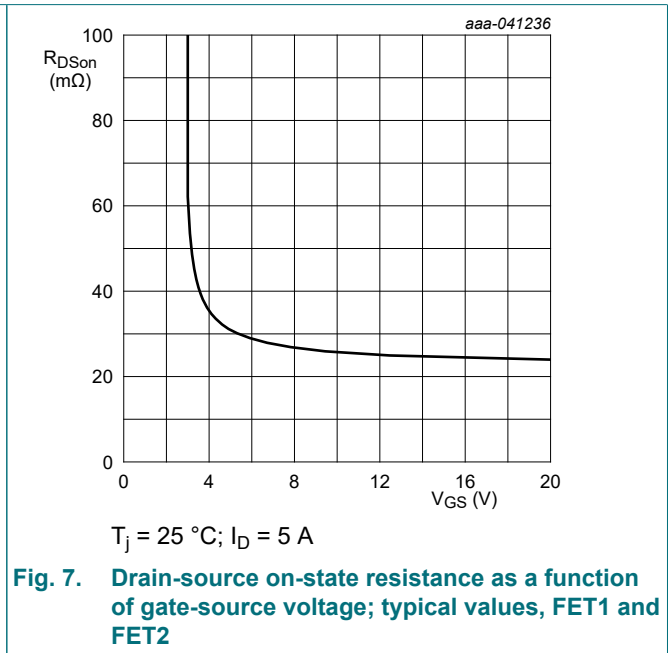
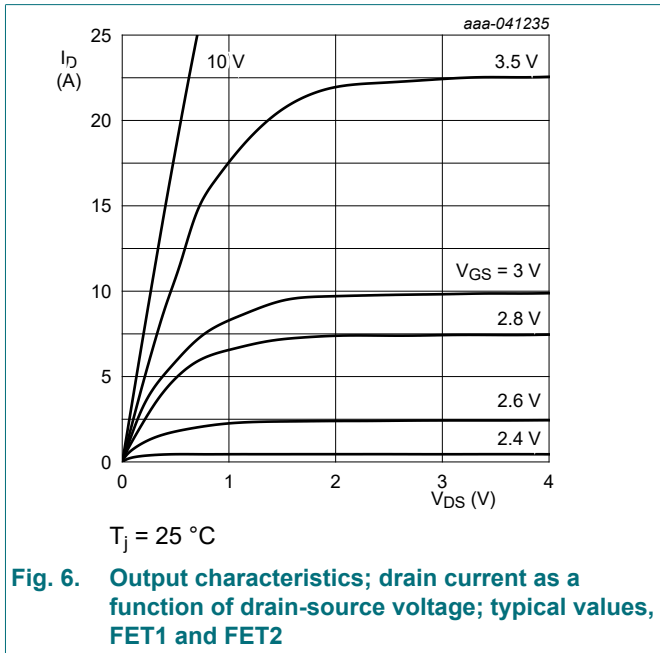
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics FET1 and FET2						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	100	117.3	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -40 \text{ }^\circ C$	92	112	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	90	110	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 0.05 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ C;$ Fig. 9; Fig. 10	1.4	1.7	2.05	V
		$I_D = 0.05 \text{ mA}; V_{DS}=V_{GS}; T_j = 175 \text{ }^\circ C;$ Fig. 10	0.5	-	-	V
		$I_D = 0.05 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ C;$ Fig. 10	-	-	2.45	V
I_{DSS}	drain leakage current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.005	1	μA
		$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ C$	-	2.5	100	μA
		$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ C$	-	30	500	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	150	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	150	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ C;$ Fig. 11	19	24	35	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}; T_j = 100 \text{ }^\circ C;$ Fig. 12	28	37	56	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}; T_j = 125 \text{ }^\circ C;$ Fig. 12	30.5	41	62	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}; T_j = 175 \text{ }^\circ C;$ Fig. 12	37	51	80	m Ω
		$V_{GS} = 4.5 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ C;$ Fig. 11	24	32	52	m Ω
		$V_{GS} = 4.5 \text{ V}; I_D = 5 \text{ A}; T_j = 100 \text{ }^\circ C;$ Fig. 12	35.7	49	84	m Ω
		$V_{GS} = 4.5 \text{ V}; I_D = 5 \text{ A}; T_j = 125 \text{ }^\circ C;$ Fig. 12	39	54	92	m Ω
		$V_{GS} = 4.5 \text{ V}; I_D = 5 \text{ A}; T_j = 175 \text{ }^\circ C;$ Fig. 12	47.4	68	119	m Ω
R_G	gate resistance	$f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$	0.9	1.8	3.6	Ω
Dynamic characteristics FET1 and FET2						
$Q_{G(tot)}$	total gate charge	$I_D = 5 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 5 \text{ V};$ $T_j = 25 \text{ }^\circ C;$ Fig. 13; Fig. 14	5.3	10.7	16.5	nC
		$I_D = 5 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V};$ $T_j = 25 \text{ }^\circ C;$ Fig. 13; Fig. 14	10	20	30	nC
Q_{GS}	gate-source charge	$I_D = 5 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 5 \text{ V};$ $T_j = 25 \text{ }^\circ C;$ Fig. 13; Fig. 14	2	3.3	4.6	nC
Q_{GD}	gate-drain charge	$I_D = 5 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 5 \text{ V};$ $T_j = 25 \text{ }^\circ C;$ Fig. 13; Fig. 14	0.93	3.1	6.8	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 5 \text{ A}; V_{DS} = 50 \text{ V}; T_j = 25 \text{ }^\circ C;$ Fig. 13; Fig. 14	-	2.7	-	V
C_{iss}	input capacitance	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ C;$ Fig. 15	750	1252	1752	pF
C_{oss}	output capacitance	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ C;$ Fig. 15	188	313	500	pF
C_{rss}	reverse transfer capacitance	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ C;$ Fig. 15	13.2	33	52.8	pF

Dual N-channel 100 V, 35 mOhm logic level MOSFET in LPAK56D

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	turn-on delay time	$V_{DS} = 50\text{ V}; R_L = 10\ \Omega; V_{GS} = 4.5\text{ V};$ $R_{G(ext)} = 5\ \Omega; T_j = 25\text{ }^\circ\text{C}$	-	10.7	-	ns
t_r	rise time		-	15.1	-	ns
$t_{d(off)}$	turn-off delay time		-	12.9	-	ns
t_f	fall time		-	10.5	-	ns
Source-drain diode FET1 and FET2						
V_{SD}	source-drain voltage	$I_S = 5\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ Fig. 16	-	0.84	1	V
t_{rr}	reverse recovery time	$I_S = 5\text{ A}; dI_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$	-	42	-	ns
Q_r	recovered charge	$V_{DS} = 50\text{ V}; T_j = 25\text{ }^\circ\text{C};$ Fig. 17	-	28	-	nC



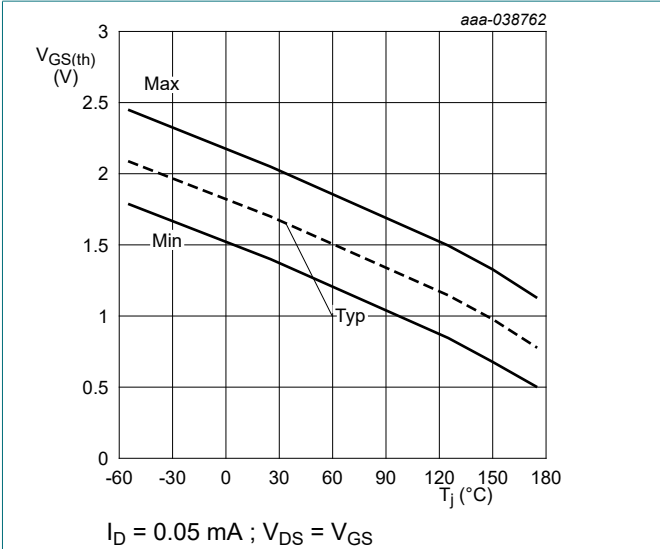


Fig. 10. Gate-source threshold voltage as a function of junction temperature, FET1 and FET2

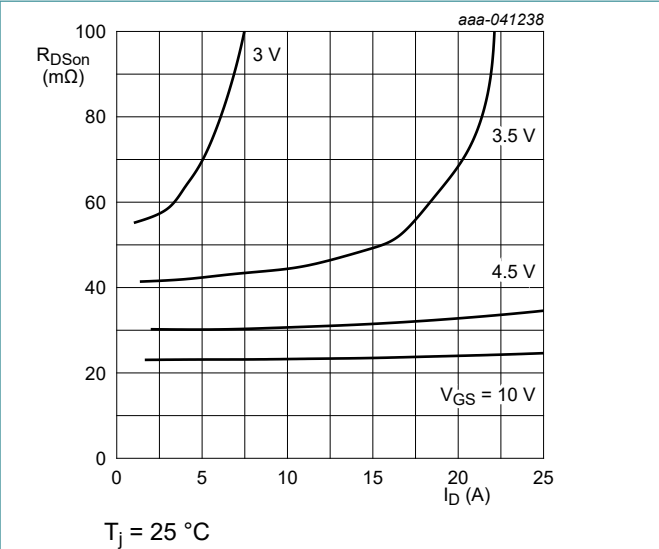


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values, FET1 and FET2

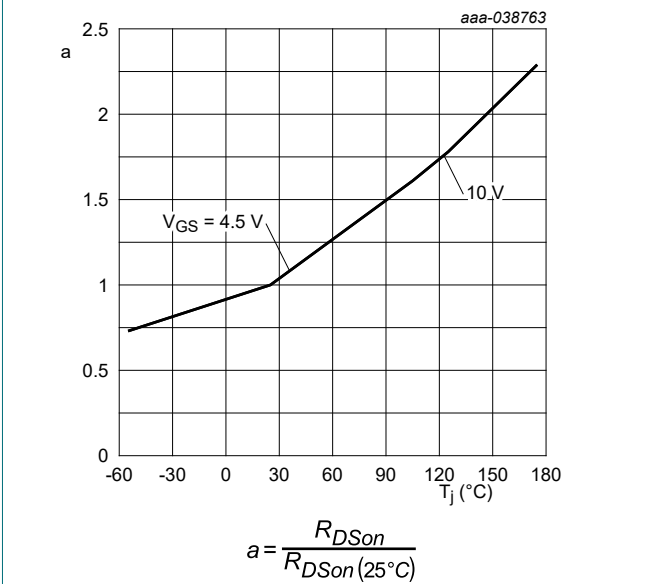


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature, FET1 and FET2

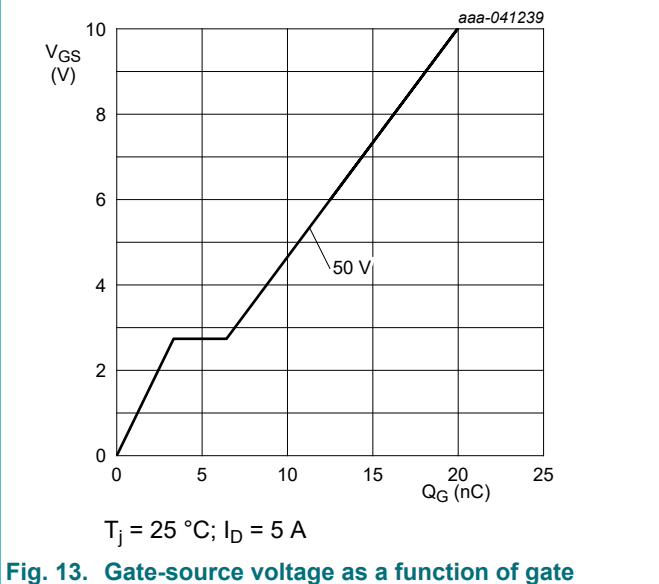


Fig. 13. Gate-source voltage as a function of gate charge; typical values, FET1 and FET2

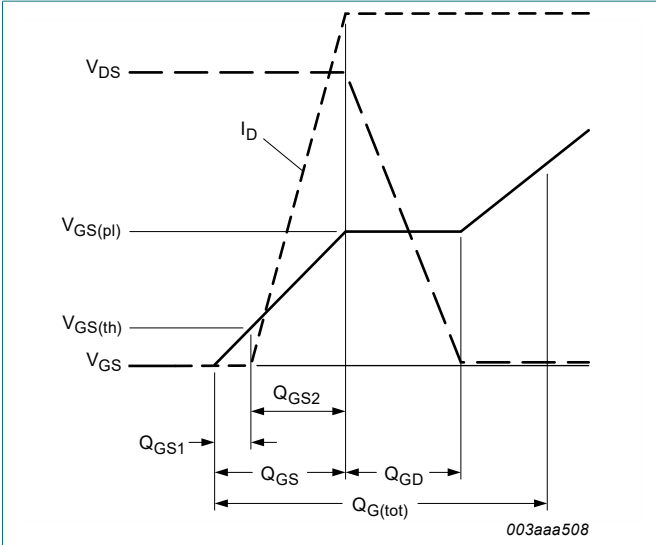


Fig. 14. Gate charge waveform definitions

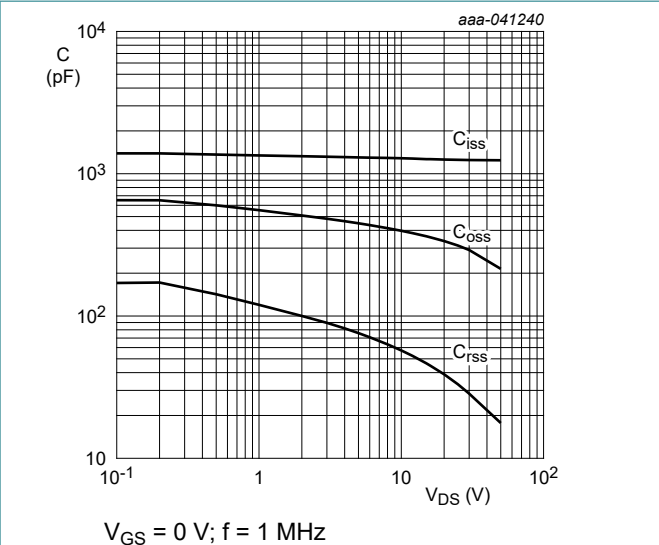


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values, FET1 and FET2

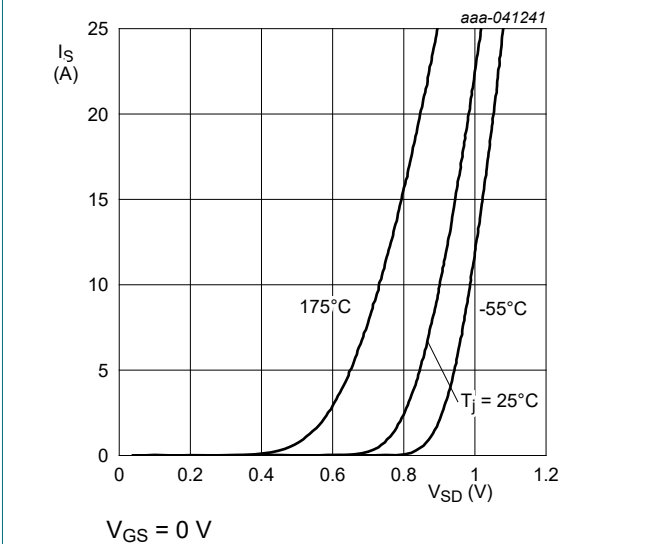


Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values, FET1 and FET2

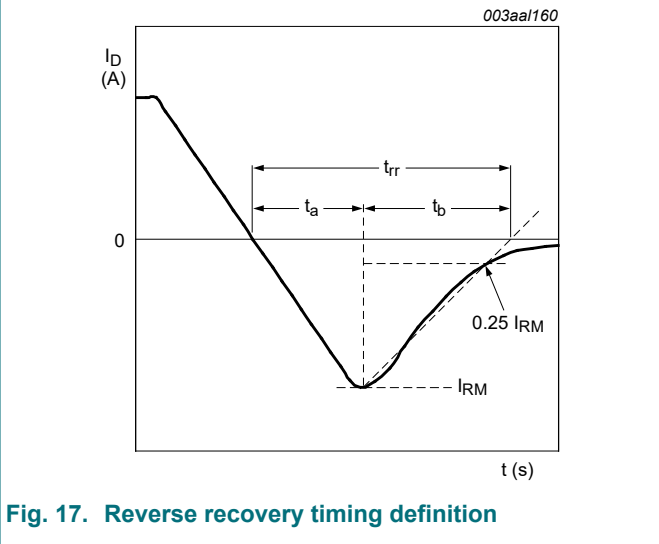


Fig. 17. Reverse recovery timing definition

11. Package outline

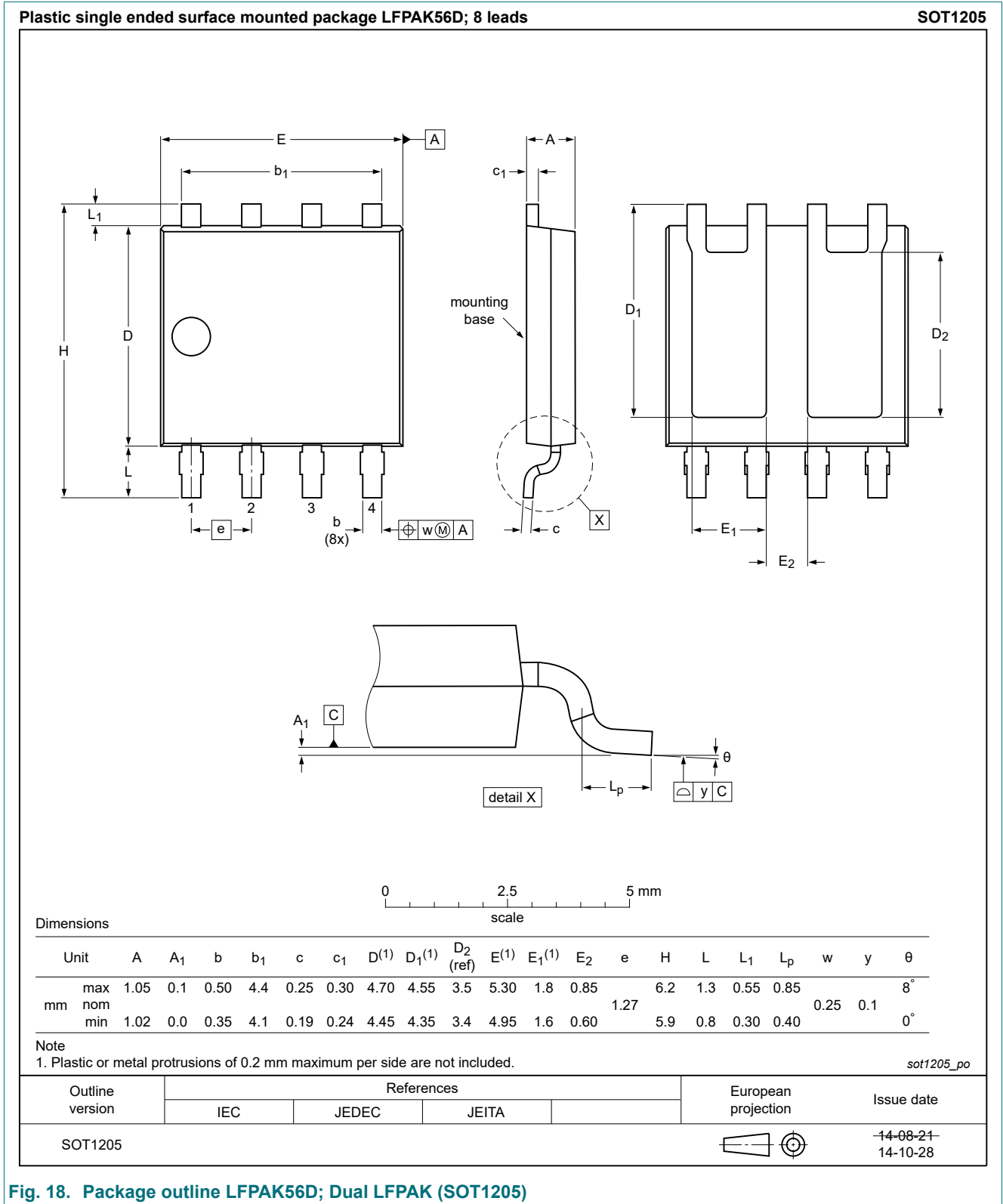


Fig. 18. Package outline LPAK56D; Dual LPAK (SOT1205)

12. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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