1. General description

Dual, logic level N-channel MOSFET in an LFPAK56D package, using Application Specific (ASFET) repetitive avalanche silicon technology. This product has been designed and qualified to AEC-Q101 for use in repetitive avalanche applications.

2. Features and benefits

- Fully automotive qualified to AEC-Q101 at 175 °C
- Repetitive Avalanche rated to 30 °C $T_j$ rise:
  - Tested to 1 Bn avalanche events
- LFPAK copper clip package technology:
  - High robustness and reliability
  - Gull wing leads for high manufacturability and AOI

3. Applications

- 12 V, 24 V and 48 V automotive systems
- Repetitive avalanche topologies
- Engine control
- Transmission control
- Actuator and auxiliary loads

4. Quick reference data

<table>
<thead>
<tr>
<th>Table 1. Quick reference data</th>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$V_{DS}$</td>
<td>drain-source voltage</td>
<td>$25 , ^\circ C \leq T_j \leq 175 , ^\circ C$</td>
<td>-</td>
<td>-</td>
<td>40</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$I_D$</td>
<td>drain current</td>
<td>$V_{GS} = 5 , V$; $T_{mb} = 25 , ^\circ C$; Fig. 2</td>
<td>-</td>
<td>-</td>
<td>18.2</td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>$P_{tot}$</td>
<td>total power dissipation</td>
<td>$T_{mb} = 25 , ^\circ C$; Fig. 1</td>
<td>-</td>
<td>-</td>
<td>32</td>
<td>W</td>
</tr>
</tbody>
</table>

**Static characteristics FET1 and FET2**

| $R_{DSon}$ | drain-source on-state resistance | $V_{GS} = 5 \, V$; $I_D = 5 \, A$; $T_j = 25 \, ^\circ C$; Fig. 14 | -   | 24  | 29  | mΩ   |

**Dynamic characteristics FET1 and FET2**

| $Q_{GD}$ | gate-drain charge | $I_D = 5 \, A$; $V_{DS} = 32 \, V$; $V_{GS} = 5 \, V$; $T_j = 25 \, ^\circ C$; Fig. 16; Fig. 17 | -   | 2.4 | -   | nC   |
5. Pinning information

Table 2. Pinning information

<table>
<thead>
<tr>
<th>Pin</th>
<th>Symbol</th>
<th>Description</th>
<th>Simplified outline</th>
<th>Graphic symbol</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>S1</td>
<td>source1</td>
<td>8 7 6 5</td>
<td>D1 D1</td>
</tr>
<tr>
<td>2</td>
<td>G1</td>
<td>gate1</td>
<td></td>
<td>D2 D2</td>
</tr>
<tr>
<td>3</td>
<td>S2</td>
<td>source2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>G2</td>
<td>gate2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>D2</td>
<td>drain2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>D2</td>
<td>drain2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>D1</td>
<td>drain1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>D1</td>
<td>drain1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

6. Ordering information

Table 3. Ordering information

<table>
<thead>
<tr>
<th>Type number</th>
<th>Package Name</th>
<th>Description</th>
<th>Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>BUK9K25-40RA</td>
<td>LFPAK56D; Dual LFPAK</td>
<td>plastic, single ended surface mounted package (LFPAK56D); 8 leads</td>
<td>SOT1205</td>
</tr>
</tbody>
</table>

7. Marking

Table 4. Marking codes

<table>
<thead>
<tr>
<th>Type number</th>
<th>Marking code</th>
</tr>
</thead>
<tbody>
<tr>
<td>BUK9K25-40RA</td>
<td>92540RA</td>
</tr>
</tbody>
</table>

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{DS}</td>
<td>drain-source voltage</td>
<td>25 °C ≤ T_j ≤ 175 °C</td>
<td>-</td>
<td>40</td>
<td>V</td>
</tr>
<tr>
<td>V_{DGR}</td>
<td>drain-gate voltage</td>
<td>RGS = 20 kΩ</td>
<td>-</td>
<td>40</td>
<td>V</td>
</tr>
<tr>
<td>V_{GS}</td>
<td>gate-source voltage</td>
<td>Pulsed; T_j ≤ 175 °C</td>
<td>[1] [2]</td>
<td>15</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DC; T_j ≤ 175 °C</td>
<td></td>
<td>-10</td>
<td>V</td>
</tr>
<tr>
<td>P_{tot}</td>
<td>total power dissipation</td>
<td>T_{mb} = 25 °C; Fig. 1</td>
<td>-</td>
<td>32</td>
<td>W</td>
</tr>
<tr>
<td>I_D</td>
<td>drain current</td>
<td>V_{GS} = 5 V; T_{mb} = 25 °C; Fig. 2</td>
<td>-</td>
<td>18.2</td>
<td>A</td>
</tr>
<tr>
<td>I_{DM}</td>
<td>peak drain current</td>
<td>V_{GS} = 5 V; T_{mb} = 100 °C; Fig. 2</td>
<td>-</td>
<td>16.6</td>
<td>A</td>
</tr>
<tr>
<td>T_{slg}</td>
<td>storage temperature</td>
<td>pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C; Fig. 3</td>
<td>-</td>
<td>94</td>
<td>A</td>
</tr>
<tr>
<td>T_j</td>
<td>junction temperature</td>
<td>-55</td>
<td>175</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

Source-drain diode FET1 and FET2

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>I_S</td>
<td>source current</td>
<td>T_{mb} = 25 °C</td>
<td>-</td>
<td>18.2</td>
<td>A</td>
</tr>
<tr>
<td>I_{SM}</td>
<td>peak source current</td>
<td>pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C</td>
<td>-</td>
<td>94</td>
<td>A</td>
</tr>
</tbody>
</table>
## Dual N-channel 40 V, 29 mOhm logic level MOSFET in LFPAK56D using Repetitive Avalanche technology

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>E_{DS(AL)}R</td>
<td>repetitive drain-source avalanche energy</td>
<td>I_D = 0.73 A; V_{sup} ≤ 40 V; R_{GS} = 10 Ω; V_{GS} = 10 V; T_{j(rise)} ≤ 30 °C; unclamped; Fig. 4; Fig. 5; Fig. 6</td>
<td>19</td>
<td>-</td>
<td>mJ</td>
</tr>
<tr>
<td>E_{DS(AL)}S</td>
<td>non-repetitive drain-source avalanche energy</td>
<td>I_D = 18.2 A; V_{sup} ≤ 40 V; V_{GS} = 10 V; T_{j(init)} = 25 °C</td>
<td>15</td>
<td>-</td>
<td>mJ</td>
</tr>
</tbody>
</table>

---

1. Accumulated Pulse duration up to 50 hours delivers zero defect ppm.
2. Significantly longer life times are achieved by lowering T_j and or V_{GS}.
3. Repetitive avalanche rating is limited by maximum junction temperature of 175 °C and junction rise of 30 °C
4. Refer to Fig. 5 for the limiting number of avalanche events
5. Refer to Fig. 6 Rdson at Vgs=5V will increase as a function of repetitive avalanche cycles
6. Refer to application note AN10273 for further information
7. Single-pulse avalanche rating limited by maximum junction temperature of 175 °C

---

**Fig. 1. Normalized total power dissipation as a function of mounting base temperature**

\[ P_{der} = \frac{P_{tot}}{P_{tot(25 °C)}} \times 100 \% \]

**Fig. 2. Continuous drain current as a function of mounting base temperature**

**Fig. 3. Safe operating area; continuous and peak drain current as a function of drain-source voltage**
Dual N-channel 40 V, 29 mOhm logic level MOSFET in LFPAK56D using Repetitive Avalanche technology

\[ T_j \text{ is limited to 175 °C and } T_{j\text{rise}} \text{ is limited to 30 °C} \]

**Fig. 4.** Repetitive avalanche rating; avalanche current as a function of avalanche time

**Fig. 5.** Repetitive avalanche rating; maximum number of avalanche events as a function of avalanche energy

\[ T_j \text{ (init) } = 25 \degree \text{C} \]

**Fig. 7.** Single pulse avalanche rating; avalanche current as a function of avalanche time
9. Thermal characteristics

Table 6. Thermal characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{th(j-mb)} )</td>
<td>thermal resistance from junction to mounting base</td>
<td>Fig. 8</td>
<td>-</td>
<td>-</td>
<td>4.68</td>
<td>K/W</td>
</tr>
<tr>
<td>( R_{th(j-a)} )</td>
<td>thermal resistance from junction to ambient</td>
<td>Minimum footprint; mounted on a printed circuit board</td>
<td>-</td>
<td>95</td>
<td>-</td>
<td>K/W</td>
</tr>
</tbody>
</table>

Fig. 8. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Static characteristics FET1 and FET2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{(BR)DSS} )</td>
<td>drain-source breakdown voltage</td>
<td>( I_D = 250 \mu A; V_{GS} = 0 \ V; T_j = -55 \ ^\circ C )</td>
<td>36</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( I_D = 250 \mu A; V_{GS} = 0 \ V; T_j = 25 \ ^\circ C )</td>
<td>40</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>( V_{GS(th)} )</td>
<td>gate-source threshold voltage</td>
<td>( I_D = 1 \ mA; V_{DS}=V_{GS}; T_j = 25 \ ^\circ C ); Fig. 12; Fig. 13</td>
<td>1.4</td>
<td>1.7</td>
<td>2.1</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( I_D = 1 \ mA; V_{DS}=V_{GS}; T_j = 175 \ ^\circ C ); Fig. 12; Fig. 13</td>
<td>0.5</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( I_D = 1 \ mA; V_{DS}=V_{GS}; T_j = -55 \ ^\circ C ); Fig. 12; Fig. 13</td>
<td>-</td>
<td>-</td>
<td>2.45</td>
<td>V</td>
</tr>
<tr>
<td>( I_{DSS} )</td>
<td>drain leakage current</td>
<td>( V_{DS} = 40 \ V; V_{GS} = 0 \ V; T_j = 175 \ ^\circ C )</td>
<td>-</td>
<td>-</td>
<td>500</td>
<td>\mu A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{DS} = 40 \ V; V_{GS} = 0 \ V; T_j = 25 \ ^\circ C )</td>
<td>-</td>
<td>0.02</td>
<td>1</td>
<td>\mu A</td>
</tr>
<tr>
<td>( I_{GSS} )</td>
<td>gate leakage current</td>
<td>( V_{GS} = -10 \ V; V_{DS} = 0 \ V; T_j = 25 \ ^\circ C )</td>
<td>-</td>
<td>2</td>
<td>100</td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{GS} = 10 \ V; V_{DS} = 0 \ V; T_j = 25 \ ^\circ C )</td>
<td>-</td>
<td>2</td>
<td>100</td>
<td>nA</td>
</tr>
<tr>
<td>( R_{DSon} )</td>
<td>drain-source on-state resistance</td>
<td>( V_{GS} = 5 \ V; I_D = 5 \ A; T_j = 25 \ ^\circ C ); Fig. 14</td>
<td>-</td>
<td>24</td>
<td>29</td>
<td>m\Omega</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{GS} = 5 \ V; I_D = 5 \ A; T_j = 175 \ ^\circ C ); Fig. 14; Fig. 15</td>
<td>-</td>
<td>48.2</td>
<td>58</td>
<td>m\Omega</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{GS} = 10 \ V; I_D = 5 \ A; T_j = 25 \ ^\circ C ); Fig. 14</td>
<td>-</td>
<td>19</td>
<td>24</td>
<td>m\Omega</td>
</tr>
</tbody>
</table>
Nexperia

BUK9K25-40RA

Dual N-channel 40 V, 29 mOhm logic level MOSFET in LFPAK56D using Repetitive Avalanche technology

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q_G(tot)</td>
<td>total gate charge</td>
<td>( I_D = 5 , \text{A}; , V_{DS} = 32 , \text{V}; , V_{GS} = 5 , \text{V}; , T_j = 25 , ^\circ \text{C}; , \text{Fig. 16}; , \text{Fig. 17} )</td>
<td>-</td>
<td>6.3</td>
<td>-</td>
<td>nC</td>
</tr>
<tr>
<td>Q_GS</td>
<td>gate-source charge</td>
<td>( I_D = 5 , \text{A}; , V_{DS} = 32 , \text{V}; , V_{GS} = 5 , \text{V}; , T_j = 25 , ^\circ \text{C}; , \text{Fig. 16}; , \text{Fig. 17} )</td>
<td>-</td>
<td>1.4</td>
<td>-</td>
<td>nC</td>
</tr>
<tr>
<td>Q_GD</td>
<td>gate-drain charge</td>
<td>( I_D = 5 , \text{A}; , V_{DS} = 32 , \text{V}; , V_{GS} = 5 , \text{V}; , T_j = 25 , ^\circ \text{C}; , \text{Fig. 16}; , \text{Fig. 17} )</td>
<td>-</td>
<td>2.4</td>
<td>-</td>
<td>nC</td>
</tr>
<tr>
<td>C_{iss}</td>
<td>input capacitance</td>
<td>( V_{DS} = 25 , \text{V}; , V_{GS} = 0 , \text{V}; , f = 1 , \text{MHz}; , T_j = 25 , ^\circ \text{C}; , \text{Fig. 16}; , \text{Fig. 17} )</td>
<td>-</td>
<td>528</td>
<td>701</td>
<td>pF</td>
</tr>
<tr>
<td>C_{oss}</td>
<td>output capacitance</td>
<td>( V_{DS} = 25 , \text{V}; , V_{GS} = 0 , \text{V}; , f = 1 , \text{MHz}; , T_j = 25 , ^\circ \text{C}; , \text{Fig. 16}; , \text{Fig. 17} )</td>
<td>-</td>
<td>95</td>
<td>114</td>
<td>pF</td>
</tr>
<tr>
<td>C_{rss}</td>
<td>reverse transfer capacitance</td>
<td>( V_{DS} = 25 , \text{V}; , V_{GS} = 0 , \text{V}; , f = 1 , \text{MHz}; , T_j = 25 , ^\circ \text{C}; , \text{Fig. 16}; , \text{Fig. 17} )</td>
<td>-</td>
<td>56</td>
<td>76</td>
<td>pF</td>
</tr>
<tr>
<td>t_{on}</td>
<td>turn-on delay time</td>
<td>( V_{DS} = 32 , \text{V}; , R_L = 6.4 , \Omega; , V_{GS} = 5 , \text{V}; , R_{G(\text{ext})} = 5 , \Omega; , T_j = 25 , ^\circ \text{C} )</td>
<td>-</td>
<td>6.2</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>t_r</td>
<td>rise time</td>
<td>( V_{DS} = 32 , \text{V}; , R_L = 6.4 , \Omega; , V_{GS} = 5 , \text{V}; , R_{G(\text{ext})} = 5 , \Omega; , T_j = 25 , ^\circ \text{C} )</td>
<td>-</td>
<td>9.2</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>t_{off}</td>
<td>turn-off delay time</td>
<td>( V_{DS} = 32 , \text{V}; , R_L = 6.4 , \Omega; , V_{GS} = 5 , \text{V}; , R_{G(\text{ext})} = 5 , \Omega; , T_j = 25 , ^\circ \text{C} )</td>
<td>-</td>
<td>10.8</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>t_f</td>
<td>fall time</td>
<td>( V_{DS} = 32 , \text{V}; , R_L = 6.4 , \Omega; , V_{GS} = 5 , \text{V}; , R_{G(\text{ext})} = 5 , \Omega; , T_j = 25 , ^\circ \text{C} )</td>
<td>-</td>
<td>8.9</td>
<td>-</td>
<td>ns</td>
</tr>
</tbody>
</table>

Source-drain diode FET1 and FET2

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{SD}</td>
<td>source-drain voltage</td>
<td>( I_S = 5 , \text{A}; , V_{GS} = 0 , \text{V}; , T_j = 25 , ^\circ \text{C}; , \text{Fig. 19} )</td>
<td>-</td>
<td>0.83</td>
<td>1.2</td>
<td>V</td>
</tr>
<tr>
<td>t_{rr}</td>
<td>reverse recovery time</td>
<td>( I_S = 5 , \text{A}; , dI_S/dt = -100 , \text{A}/\mu\text{s}; , V_{GS} = 0 , \text{V}; , V_{DS} = 20 , \text{V}; , T_j = 25 , ^\circ \text{C} )</td>
<td>-</td>
<td>15.9</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>Q_r</td>
<td>recovered charge</td>
<td>( I_S = 5 , \text{A}; , dI_S/dt = -100 , \text{A}/\mu\text{s}; , V_{GS} = 0 , \text{V}; , V_{DS} = 20 , \text{V}; , T_j = 25 , ^\circ \text{C} )</td>
<td>-</td>
<td>7.6</td>
<td>-</td>
<td>nC</td>
</tr>
</tbody>
</table>

Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

Fig. 10. Drain-source on-state resistance as a function of gate-source voltage; typical values
Fig. 11. Output characteristics; drain current as a function of drain-source voltage; typical values

Fig. 12. Gate-source threshold voltage as a function of junction temperature

Fig. 13. Sub-threshold drain current as a function of gate-source voltage

Fig. 14. Drain-source on-state resistance as a function of drain current; typical values
Fig. 15. Normalized drain-source on-state resistance factor as a function of junction temperature

\[ a = \frac{R_{DS\text{on}}}{R_{DS\text{on} \ (25^\circ C)}} \]

Fig. 16. Gate-source voltage as a function of gate charge; typical values

\[ T_J = 25^\circ C, \ \ I_D = 5A \]

Fig. 17. Gate charge waveform definitions

Fig. 18. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

\[ V_{GS} = 0V, \ f = 1\text{MHz} \]
Fig. 19. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values
11. Package outline

Plastic single ended surface mounted package LFPAK56D; 8 leads

**Dimensions**

<table>
<thead>
<tr>
<th>Unit</th>
<th>A</th>
<th>A₁</th>
<th>b</th>
<th>b₁</th>
<th>c</th>
<th>c₁</th>
<th>D₁(1)</th>
<th>D₂(1)</th>
<th>D₂ (ref)</th>
<th>E₁(1)</th>
<th>E₂</th>
<th>e</th>
<th>H</th>
<th>L</th>
<th>L₁</th>
<th>L_p</th>
<th>w</th>
<th>y</th>
<th>θ</th>
</tr>
</thead>
<tbody>
<tr>
<td>mm</td>
<td>max</td>
<td>1.05</td>
<td>0.1</td>
<td>0.50</td>
<td>4.4</td>
<td>0.25</td>
<td>0.30</td>
<td>4.70</td>
<td>4.55</td>
<td>3.5</td>
<td>5.30</td>
<td>1.8</td>
<td>0.85</td>
<td>6.2</td>
<td>1.3</td>
<td>0.55</td>
<td>0.85</td>
<td>0.25</td>
<td>0.1</td>
</tr>
<tr>
<td></td>
<td>min</td>
<td>1.02</td>
<td>0.0</td>
<td>0.35</td>
<td>4.1</td>
<td>0.19</td>
<td>0.24</td>
<td>4.45</td>
<td>4.35</td>
<td>3.4</td>
<td>4.95</td>
<td>1.6</td>
<td>0.60</td>
<td>5.9</td>
<td>0.8</td>
<td>0.30</td>
<td>0.40</td>
<td>0.25</td>
<td>0.1</td>
</tr>
</tbody>
</table>

**Note**
1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

**Fig. 20. Package outline LFPAK56D; Dual LFPAK (SOT1205)**
12. Soldering

Footprint information for reflow soldering of LFPAK56D package

Fig. 21. Reflow soldering footprint for LFPAK56D; Dual LFPAK (SOT1205)
13. Legal information

Data sheet status

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Objective [short] data sheet</td>
<td>Development</td>
<td>This document contains data from the objective specification for product development.</td>
</tr>
<tr>
<td>Preliminary [short] data sheet</td>
<td>Qualification</td>
<td>This document contains data from the preliminary specification.</td>
</tr>
<tr>
<td>Product [short] data sheet</td>
<td>Production</td>
<td>This document contains the product specification.</td>
</tr>
</tbody>
</table>

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[2] The term “short data sheet” is explained in section “Definitions”.
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BUK9K25-40RA

Dual N-channel 40 V, 29 mOhm logic level MOSFET in LFPAK56D using Repetitive Avalanche technology

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