1. General description

Automotive qualified N-channel MOSFET using the latest Trench 9 low ohmic superjunction technology, housed in a robust LFPAK56 package. This product has been fully designed and qualified to meet AEC-Q101 requirements delivering high performance and endurance.

2. Features and benefits

- Fully automotive qualified to AEC-Q101:
  - 175 °C rating suitable for thermally demanding environments
- Trench 9 Superjunction technology:
  - Reduced cell pitch enables enhanced power density and efficiency with lower $R_{\text{DS(on)}}$ in same footprint
  - Improved SOA and avalanche capability compared to standard TrenchMOS
  - Tight $V_{\text{GS(th)}}$ limits enable easy paralleling of MOSFETs
- LFPAK Gull Wing leads:
  - High Board Level Reliability absorbing mechanical stress during thermal cycling, unlike traditional QFN packages
  - Visual (AOI) soldering inspection, no need for expensive x-ray equipment
  - Easy solder wetting for good mechanical solder joint
- LFPAK copper clip technology:
  - Improved reliability, with reduced $R_{\text{th}}$ and $R_{\text{DS(on)}}$
  - Increases maximum current capability and improved current spreading

3. Applications

- 12 V automotive systems
- Motors, lamps and solenoid control
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

4. Quick reference data

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
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</thead>
<tbody>
<tr>
<td>$V_{DS}$</td>
<td>drain-source voltage</td>
<td>$25 \ ^\circ\mathrm{C} \leq T_j \leq 175 \ ^\circ\mathrm{C}$</td>
<td>-</td>
<td>-</td>
<td>40</td>
<td>V</td>
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<tr>
<td>$I_D$</td>
<td>drain current</td>
<td>$V_{GS} = 10 \ V; T_{mb} = 25 \ ^\circ\mathrm{C}$; Fig. 2</td>
<td>[1]</td>
<td>-</td>
<td>120</td>
<td>A</td>
</tr>
<tr>
<td>$P_{tot}$</td>
<td>total power dissipation</td>
<td>$T_{mb} = 25 \ ^\circ\mathrm{C}$; Fig. 1</td>
<td>-</td>
<td>-</td>
<td>115</td>
<td>W</td>
</tr>
</tbody>
</table>
N-channel 40 V, 3.5 mΩ standard level MOSFET in LFPAK56

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{DSon}$</td>
<td>drain-source on-state resistance</td>
<td>$V_{GS} = 10 , \text{V}; , I_D = 25 , \text{A}; , T_j = 25 , ^\circ \text{C};$</td>
<td>2</td>
<td>2.9</td>
<td>3.5</td>
<td>mΩ</td>
</tr>
</tbody>
</table>

| $Q_{GD}$ | gate-drain charge | $I_D = 25 \, \text{A}; \, V_{DS} = 32 \, \text{V}; \, V_{GS} = 10 \, \text{V};$ | -   | 6   | 15  | nC   |

| $Q_r$ | recovered charge | $I_S = 25 \, \text{A}; \, \frac{dI_S}{dt} = -100 \, \text{A}/\mu\text{s}; \, V_{GS} = 0 \, \text{V}; \, V_{DS} = 20 \, \text{V};$ | -   | 16  | -    | nC   |

| $S$ | softness factor | $I_S = 25 \, \text{A}; \, \frac{dI_S}{dt} = -100 \, \text{A}/\mu\text{s}; \, V_{GS} = 0 \, \text{V}; \, V_{DS} = 20 \, \text{V}; \, T_j = 25 \, ^\circ \text{C}$ | -   | 0.8 | -    |  |

[1] 120A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

5. Pinning information

<table>
<thead>
<tr>
<th>Pin</th>
<th>Symbol</th>
<th>Description</th>
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<th>Graphic symbol</th>
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<td></td>
</tr>
<tr>
<td>2</td>
<td>S</td>
<td>source</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>S</td>
<td>source</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>G</td>
<td>gate</td>
<td></td>
<td></td>
</tr>
<tr>
<td>mb</td>
<td>D</td>
<td>mounting base; connected to drain</td>
<td>LFPAK56: Power-SO8 (SOT669)</td>
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6. Ordering information

<table>
<thead>
<tr>
<th>Type number</th>
<th>Package</th>
<th>Name</th>
<th>Description</th>
<th>Version</th>
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<tr>
<td>BUK7Y3R5-40H</td>
<td>LFPAK56; Power-SO8</td>
<td>plastic, single-ended surface-mounted package; 4 terminals</td>
<td>SOT669</td>
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7. Marking

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<tr>
<td>BUK7Y3R5-40H</td>
<td>73H540</td>
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8. Limiting values

Table 5. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

<table>
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<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DS}$</td>
<td>drain-source voltage</td>
<td>$25 \degree C \leq T_j \leq 175 \degree C$</td>
<td>-</td>
<td>40</td>
<td>V</td>
</tr>
<tr>
<td>$V_{GS}$</td>
<td>gate-source voltage</td>
<td>DC; $T_j \leq 175 \degree C$</td>
<td>-10</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>$P_{tot}$</td>
<td>total power dissipation</td>
<td>$T_{mb} = 25 \degree C$; Fig. 1</td>
<td>-</td>
<td>115</td>
<td>W</td>
</tr>
<tr>
<td>$I_D$</td>
<td>drain current</td>
<td>$V_{GS} = 10 \text{V}; T_{mb} = 25 \degree C$; Fig. 2</td>
<td>120</td>
<td>-</td>
<td>A</td>
</tr>
<tr>
<td>$I_{DM}$</td>
<td>peak drain current</td>
<td>pulsed; $t_p \leq 10 \mu s$; $T_{mb} = 25 \degree C$; Fig. 3</td>
<td>526</td>
<td>-</td>
<td>A</td>
</tr>
<tr>
<td>$T_{stg}$</td>
<td>storage temperature</td>
<td>-55 to 175 \degree C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T_j$</td>
<td>junction temperature</td>
<td>-55 to 175 \degree C</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Source-drain diode

- $I_S$ source current | $T_{mb} = 25 \degree C$ | 120 | - | A |
- $I_{SM}$ peak source current | pulsed; $t_p \leq 10 \mu s$; $T_{mb} = 25 \degree C$ | 526 | - | A |

Avalanche ruggedness

- $E_{DS(\text{AL})S}$ non-repetitive drain-source avalanche energy | $I_D = 120 \text{A}; V_{sup} \leq 40 \text{V}; R_{GS} = 50 \Omega$; $V_{GS} = 10 \text{V}; T_{j(init)} = 25 \degree C$; unclamped; Fig. 4 | 45 | - | mJ |

[1] 120 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

[2] Single-pulse avalanche rating limited by maximum junction temperature of 175 \degree C.


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25\degree C)}} \times 100 \%$$

Fig. 2. Continuous drain current as a function of mounting base temperature

$V_{GS} \geq 10 \text{V}$

(1) 120 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
Nexperia

BUK7Y3R5-40H

N-channel 40 V, 3.5 mΩ standard level MOSFET in LFPAK56

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

\[ T_{mb} = 25 \, ^\circ\text{C}; \; I_{DM} \text{ is a single pulse} \]

Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

\[ (1) \; T_J^{\text{(init)}} = 25 \, ^\circ\text{C}; \; (2) \; T_J^{\text{(init)}} = 150 \, ^\circ\text{C}; \; (3) \; \text{Repetitive Avalanche} \]
9. Thermal characteristics

Table 6. Thermal characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{th(j-mb)}$</td>
<td>thermal resistance from junction to mounting base</td>
<td>Fig. 5</td>
<td>-</td>
<td>1.18</td>
<td>1.3</td>
<td>K/W</td>
</tr>
</tbody>
</table>

![Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration](image)

10. Characteristics

Table 7. Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{(BR)DSS}$</td>
<td>drain-source breakdown voltage</td>
<td>$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 ^\circ C$</td>
<td>40</td>
<td>42.7</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -40 ^\circ C$</td>
<td>-</td>
<td>40.1</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 ^\circ C$</td>
<td>36</td>
<td>39.7</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>$V_{GS(th)}$</td>
<td>gate-source threshold voltage</td>
<td>$I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 ^\circ C$</td>
<td>2.4</td>
<td>3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_D = 1 mA; V_{DS}=V_{GS}; T_j = -55 ^\circ C$</td>
<td>-</td>
<td>-</td>
<td>4.3</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_D = 1 mA; V_{DS}=V_{GS}; T_j = 175 ^\circ C$</td>
<td>1</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>$I_{DSS}$</td>
<td>drain leakage current</td>
<td>$V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 ^\circ C$</td>
<td>-</td>
<td>0.03</td>
<td>1</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DS} = 16 V; V_{GS} = 0 V; T_j = 125 ^\circ C$</td>
<td>-</td>
<td>1</td>
<td>10</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DS} = 40 V; V_{GS} = 0 V; T_j = 175 ^\circ C$</td>
<td>-</td>
<td>37</td>
<td>500</td>
<td>µA</td>
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<tr>
<td>$I_{GSS}$</td>
<td>gate leakage current</td>
<td>$V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 ^\circ C$</td>
<td>-</td>
<td>2</td>
<td>100</td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25 ^\circ C$</td>
<td>-</td>
<td>2</td>
<td>100</td>
<td>nA</td>
</tr>
</tbody>
</table>
### Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
--- | --- | --- | --- | --- | --- | --- |
\( R_{\text{DSon}} \) | drain-source on-state resistance | \( V_{GS} = 10 \, \text{V}; \, I_D = 25 \, \text{A}; \, T_j = 25 \, ^\circ\text{C}; \) \( \text{Fig. 11} \) | 2.0 | 2.9 | 3.5 | mΩ |
\( V_{GS} = 10 \, \text{V}; \, I_D = 25 \, \text{A}; \, T_j = 105 \, ^\circ\text{C}; \) \( \text{Fig. 12} \) | 2.7 | 4.1 | 5.2 | mΩ |
\( V_{GS} = 10 \, \text{V}; \, I_D = 25 \, \text{A}; \, T_j = 125 \, ^\circ\text{C}; \) \( \text{Fig. 12} \) | 2.9 | 4.5 | 5.6 | mΩ |
\( V_{GS} = 10 \, \text{V}; \, I_D = 25 \, \text{A}; \, T_j = 175 \, ^\circ\text{C}; \) \( \text{Fig. 12} \) | 3.4 | 5.4 | 6.7 | mΩ |
\( R_G \) | gate resistance | \( f = 1 \, \text{MHz}; \, T_j = 25 \, ^\circ\text{C} \) | 0.32 | 0.8 | 2 | Ω |

#### Dynamic characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
--- | --- | --- | --- | --- | --- | --- |
\( Q_{G(tot)} \) | total gate charge | \( I_D = 25 \, \text{A}; \, V_{DS} = 32 \, \text{V}; \, V_{GS} = 10 \, \text{V}; \) \( \text{Fig. 13}; \, \text{Fig. 14} \) | - | 31 | 53 | nC |
\( Q_{GS} \) | gate-source charge | \( - \) | 10 | 15 | nC |
\( R_G \) | gate-drain charge | \( - \) | 6 | 15 | nC |
\( C_{iss} \) | input capacitance | \( V_{DS} = 25 \, \text{V}; \, V_{GS} = 0 \, \text{V}; \, f = 1 \, \text{MHz}; \) \( T_j = 25 \, ^\circ\text{C}; \) \( \text{Fig. 15} \) | - | 2294 | 3441 | pF |
\( C_{oss} \) | output capacitance | \( T_j = 25 \, ^\circ\text{C}; \) \( \text{Fig. 15} \) | - | 682 | 954 | pF |
\( C_{rss} \) | reverse transfer capacitance | \( - \) | 112 | 247 | pF |
\( t_{d(on)} \) | turn-on delay time | \( V_{GS} = 30 \, \text{V}; \, R_L = 1.2 \, \Omega; \, V_{GS} = 10 \, \text{V}; \) \( R_G(\text{ext}) = 5 \, \Omega \) | - | 10 | - | ns |
\( t_r \) | rise time | \( - \) | 8 | - | ns |
\( t_{d(off)} \) | turn-off delay time | \( - \) | 19 | - | ns |
\( t_f \) | fall time | \( - \) | 9 | - | ns |

#### Source-drain diode

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
--- | --- | --- | --- | --- | --- | --- |
\( V_{SD} \) | source-drain voltage | \( I_S = 25 \, \text{A}; \, V_{GS} = 0 \, \text{V}; \, T_j = 25 \, ^\circ\text{C}; \) \( \text{Fig. 16} \) | - | 0.8 | 1.2 | V |
\( t_r \) | reverse recovery time | \( I_S = 25 \, \text{A}; \, \text{d}I_S/\text{d}t = -100 \, \text{A}/\mu\text{s}; \, V_{GS} = 0 \, \text{V}; \) \( V_{DS} = 20 \, \text{V}; \) \( \text{Fig. 17} \) | - | 25 | - | ns |
\( Q_r \) | recovered charge | \( - \) | 16 | - | nC |
\( S \) | softness factor | \( I_S = 25 \, \text{A}; \, \text{d}I_S/\text{d}t = -100 \, \text{A}/\mu\text{s}; \, V_{GS} = 0 \, \text{V}; \) \( V_{DS} = 20 \, \text{V}; \, T_j = 25 \, ^\circ\text{C} \) | - | 0.8 | - |
\( I_S = 25 \, \text{A}; \, \text{d}I_S/\text{d}t = -500 \, \text{A}/\mu\text{s}; \, V_{GS} = 0 \, \text{V}; \) \( V_{DS} = 20 \, \text{V}; \, T_j = 25 \, ^\circ\text{C}; \) \( \text{Fig. 17} \) | - | 0.6 | - |
**Fig. 6.** Output characteristics; drain current as a function of drain-source voltage; typical values

- **T<sub>j</sub> = 25 °C**

**Fig. 7.** Drain-source on-state resistance as a function of gate-source voltage; typical values

- **T<sub>j</sub> = 25 °C; I<sub>D</sub> = 25 A**

**Fig. 8.** Transfer characteristics; drain current as a function of gate-source voltage; typical values

- **V<sub>DS</sub> = 12 V**

**Fig. 9.** Gate-source threshold voltage as a function of junction temperature

- **I<sub>D</sub> = 1 mA; V<sub>DS</sub> = V<sub>GS</sub>**
Fig. 10. Sub-threshold drain current as a function of gate-source voltage

Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

Fig. 13. Gate-source voltage as a function of gate charge; typical values
**BUK7Y3R5-40H**

**N-channel 40 V, 3.5 mΩ standard level MOSFET in LFPAK56**

---

**Fig. 14. Gate charge waveform definitions**

**Fig. 15.** Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

**Fig. 16.** Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

**Fig. 17.** Reverse recovery waveform definitions
11. Package outline

Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads

Dimensions (mm are the original dimensions)

<table>
<thead>
<tr>
<th>Unit(1)</th>
<th>A_1</th>
<th>A_2</th>
<th>A_3</th>
<th>b_1</th>
<th>b_2</th>
<th>b_3</th>
<th>b_4</th>
<th>c_2</th>
<th>D(1)_1</th>
<th>D(1)_2</th>
<th>E(1)_1</th>
<th>E(1)_2</th>
<th>e_1</th>
<th>H</th>
<th>L_1</th>
<th>L_2</th>
<th>w</th>
<th>y</th>
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</thead>
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<td>1.10</td>
<td>0.50</td>
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<td>4.10</td>
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<td>3.3</td>
<td>1.27</td>
<td>6.2</td>
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<td>1.3</td>
<td>0.25</td>
<td>0.1</td>
</tr>
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<td>nom</td>
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<td>0.40</td>
<td>0.8</td>
<td>0.8</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

Fig. 18. Package outline LFPAK56; Power-SO8 (SOT669)
12. Soldering

Fig. 19. Reflow soldering footprint for LFPAK56; Power-SO8 (SOT669)
Wave soldering footprint information for LFPAK56 package

Fig. 20. Wave soldering footprint for LFPAK56; Power-SO8 (SOT669)
13. Legal information

Data sheet status

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<thead>
<tr>
<th>Document status</th>
<th>Product status</th>
<th>Definition</th>
</tr>
</thead>
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<tr>
<td>Objective [short] data sheet</td>
<td>Development</td>
<td>This document contains data from the objective specification for product development.</td>
</tr>
<tr>
<td>Preliminary [short] data sheet</td>
<td>Qualification</td>
<td>This document contains data from the preliminary specification.</td>
</tr>
<tr>
<td>Product [short] data sheet</td>
<td>Production</td>
<td>This document contains the product specification.</td>
</tr>
</tbody>
</table>

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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