



BUK7Y3R1-80M

N-channel 80 V, 3.1 mOhm, Standard level MOSFET in LFPAK56

13 February 2024

Product data sheet

1. General description

Automotive qualified N-channel MOSFET using the latest Trench 14 low ohmic split-gate technology, for ultra-low R_{DSon} capability, housed in a LFPAK56 package. This product has been fully designed and qualified to meet AEC-Q101 requirements delivering high performance and endurance.

2. Features and benefits

- Fully automotive qualified to AEC-Q101:
 - 175 °C rating suitable for thermally demanding environments
- Trench 14 split-gate technology:
 - Reduced cell pitch enables enhanced power density and efficiency with lower R_{DSon} in same footprint
 - Fast and efficient switching with optimal damping and low spiking
- LFPAK Gull Wing leads:
 - High Board Level Reliability absorbing mechanical stress during thermal cycling, unlike traditional QFN packages
 - Visual (AOI) soldering inspection, no need for expensive x-ray equipment
 - Easy solder wetting for good mechanical solder joints
- LFPAK copper clip technology:
 - Improved reliability, with reduced R_{th} , R_{DSon} and package inductance
 - Increases maximum current capability and improved current spreading

3. Applications

- 12 V, 24 V and 48 V automotive systems
- Motor, lighting and solenoid control
- Ultra high-performance power switching

4. Quick reference data

Table 1. Quick reference data

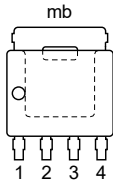
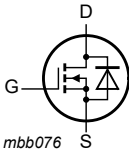
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	-	80	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	-	160	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	-	254	W
T_j	junction temperature			-55	-	175	°C
Static characteristics							
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; Fig. 9		1.7	2.5	3.1	mΩ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25\text{ A}$; $V_{DS} = 40\text{ V}$; $V_{GS} = 10\text{ V}$; Fig. 13 ; Fig. 14	35	70	105	nC

[1] 160 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LPAK56; Power-SO8 (SOT669)	 <i>mbb076</i>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK7Y3R1-80M	LPAK56; Power-SO8	plastic, single-ended surface-mounted package; 4 terminals	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK7Y3R1-80M	73M180Y

8. Limiting values

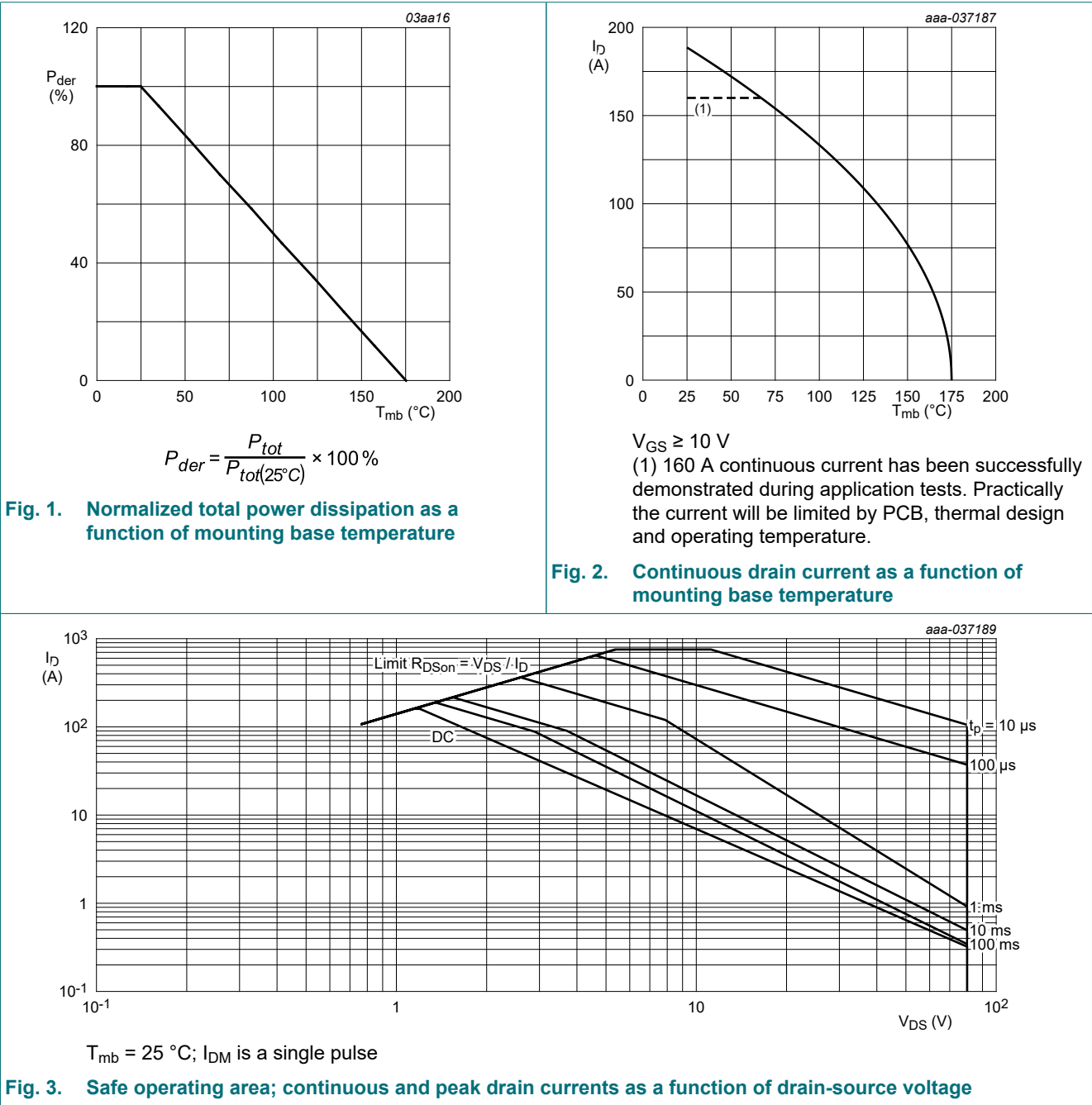
Table 5. Limiting values

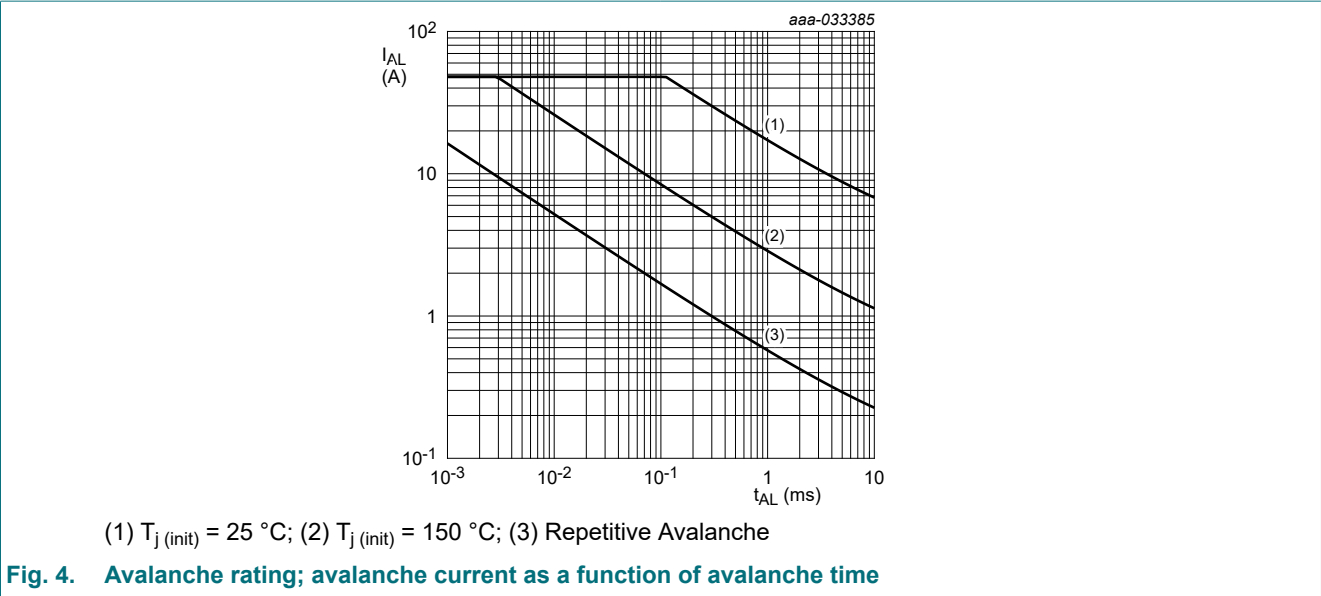
In accordance with the Absolute Maximum Rating System (IEC 60134). $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise stated.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ }^{\circ}\text{C} \leq T_j \leq 175\text{ }^{\circ}\text{C}$	-	80	V
V_{GS}	gate-source voltage		-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ }^{\circ}\text{C}$; Fig. 1	-	254	W
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ }^{\circ}\text{C}$; Fig. 2	[1]	160	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ }^{\circ}\text{C}$; Fig. 2	-	133	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ }^{\circ}\text{C}$; Fig. 3	-	754	A
T_{stg}	storage temperature		-55	175	$^{\circ}\text{C}$
T_j	junction temperature		-55	175	$^{\circ}\text{C}$

Symbol	Parameter	Conditions		Min	Max	Unit
Source-drain diode						
I _S	source current	T _{mb} = 25 °C		-	160	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	754	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 49 A; V _{sup} ≤ 80 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped; Fig. 4	[2] [3] [4]	-	289	mJ

- [1] 160 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [2] Protected by 100% test
- [3] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [4] Refer to application note AN10273 for further information.



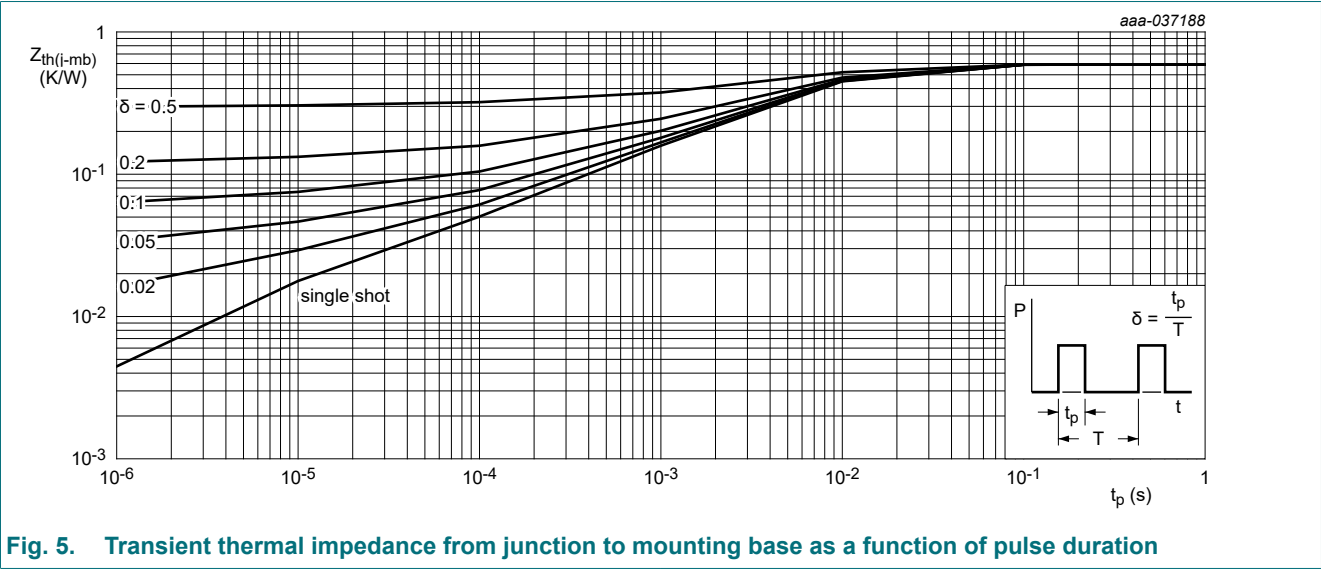


9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	0.43	0.59	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	-	24	-	K/W

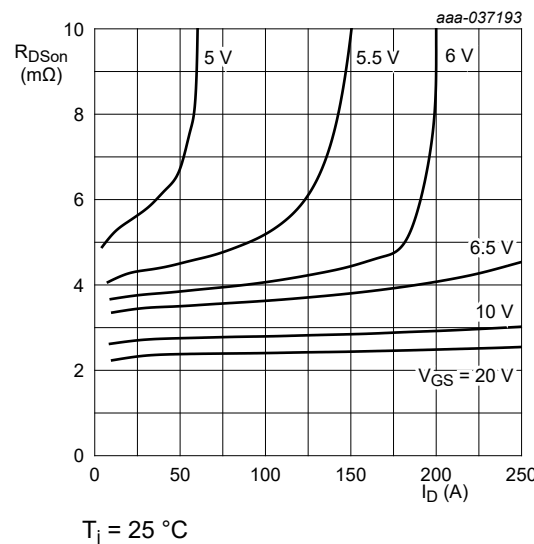
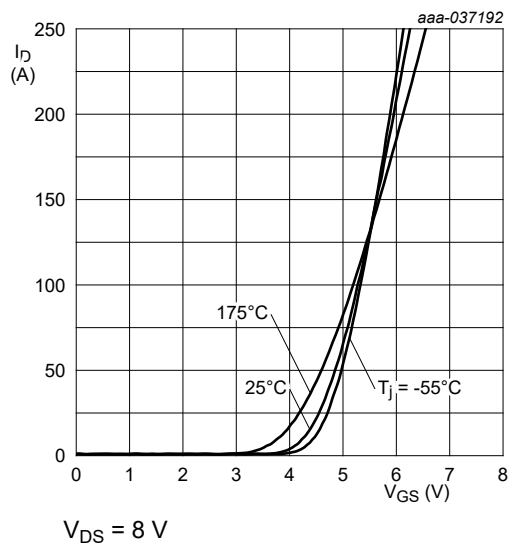
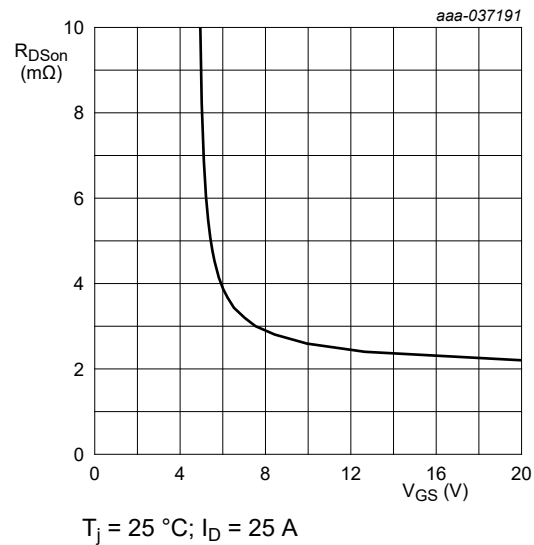
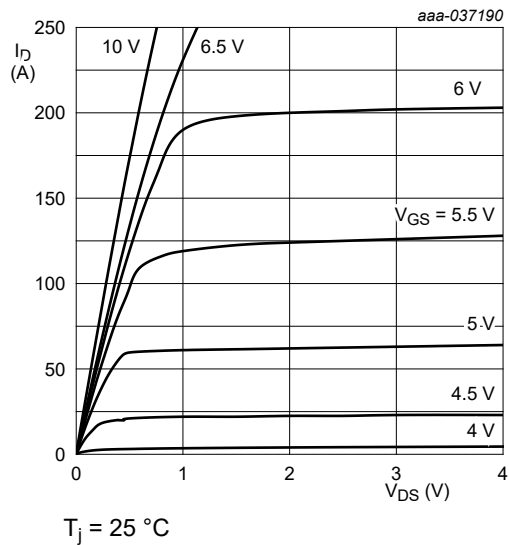
[1] Device on 4 layer PCB. Refer to TN00008 for further information.

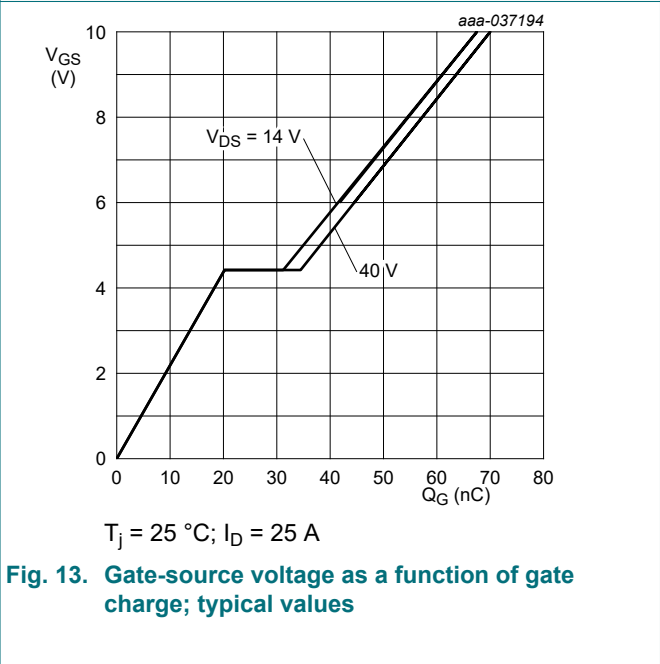
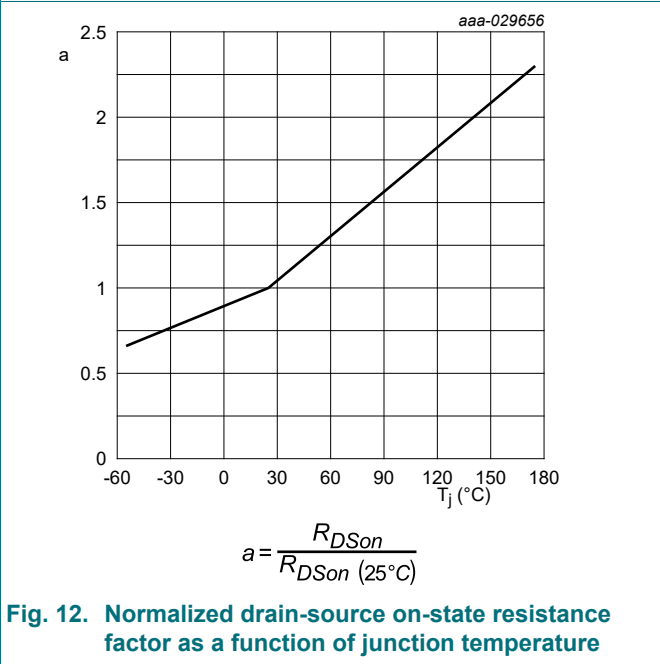
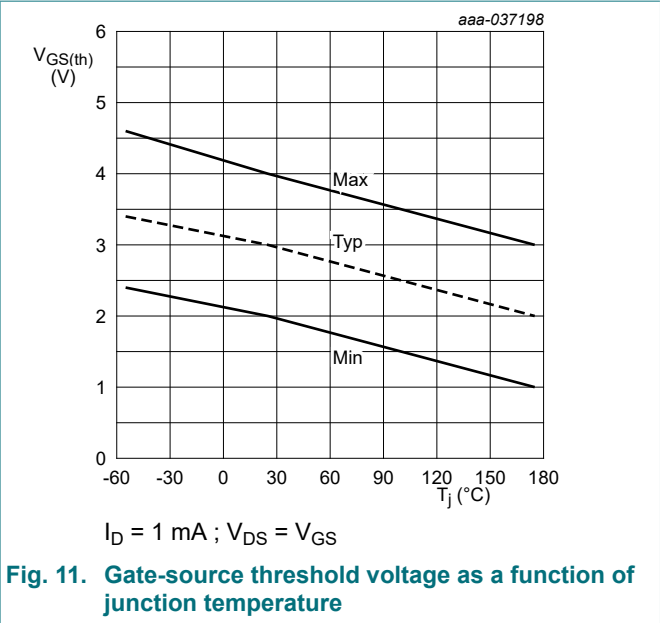
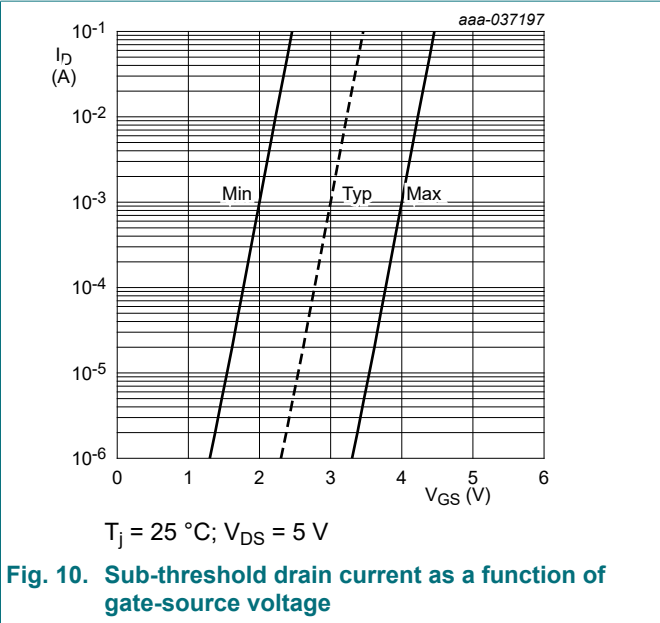


10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _J = 25 °C		80	89	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _J = -40 °C		-	86	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _J = -55 °C		72	85	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} =V _{GS} ; T _J = 25 °C; Fig. 10		2	3	4	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _J = 175 °C; Fig. 11		1	2	-	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _J = -55 °C; Fig. 11		-	3.4	4.6	V
I _{DSS}	drain leakage current	V _{DS} = 80 V; V _{GS} = 0 V; T _J = 25 °C		-	0.07	1	μA
		V _{DS} = 80 V; V _{GS} = 0 V; T _J = 125 °C		-	2	100	μA
		V _{DS} = 80 V; V _{GS} = 0 V; T _J = 175 °C		-	50	500	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _J = 25 °C		-	2	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _J = 25 °C		-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _J = 25 °C; Fig. 9		1.7	2.5	3.1	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _J = 105 °C; Fig. 12		2.6	4	5	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _J = 125 °C; Fig. 12		2.9	4.5	5.5	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _J = 175 °C; Fig. 12		3.7	5.8	7.1	mΩ
R _G	gate resistance	f = 1 MHz; T _J = 25 °C		0.35	0.7	1.4	Ω
Dynamic characteristics							
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 40 V; V _{GS} = 10 V; Fig. 13 ; Fig. 14		35	70	105	nC
Q _{GS}	gate-source charge			8	20	32	nC
Q _{GD}	gate-drain charge			5	14	32	nC
C _{iss}	input capacitance	V _{DS} = 40 V; V _{GS} = 0 V; f = 1 MHz; T _J = 25 °C; Fig. 15		2938	4896	6854	pF
C _{oss}	output capacitance			448	1121	2018	pF
C _{rss}	reverse transfer capacitance			11	53	122	pF
t _{d(on)}	turn-on delay time	V _{DS} = 40 V; R _L = 1.6 Ω; V _{GS} = 10 V; R _{G(ext)} = 5 Ω		-	20	-	ns
t _r	rise time			-	19	-	ns
t _{d(off)}	turn-off delay time			-	38	-	ns
t _f	fall time			-	22	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _J = 25 °C; Fig. 16		-	0.81	1	V
t _{rr}	reverse recovery time	I _S = 25 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 40 V; Fig. 17		-	38	-	ns
Q _r	recovered charge			-	36	-	nC





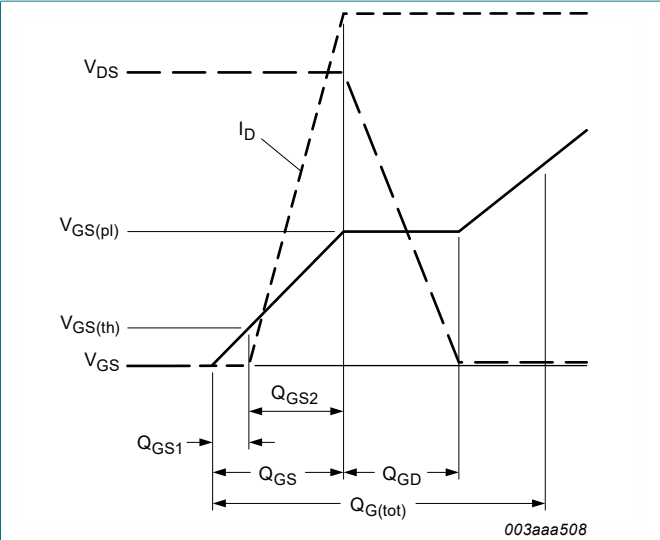


Fig. 14. Gate charge waveform definitions

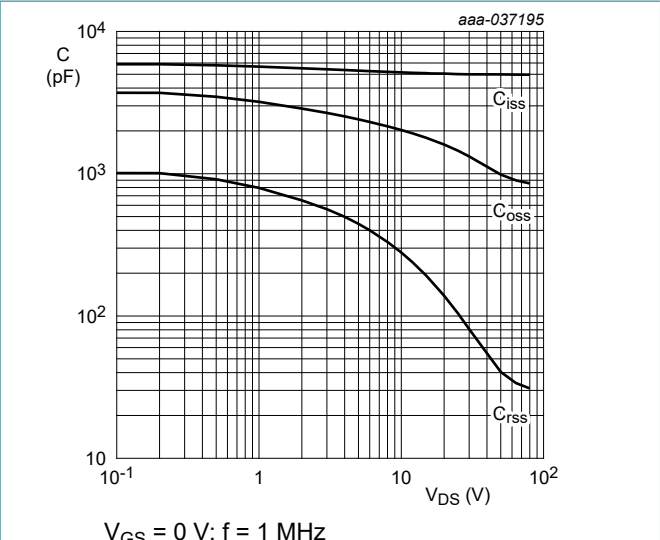


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

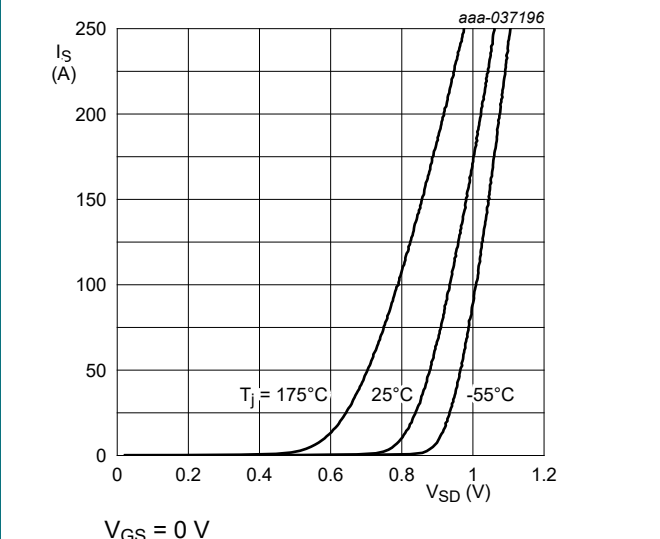


Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

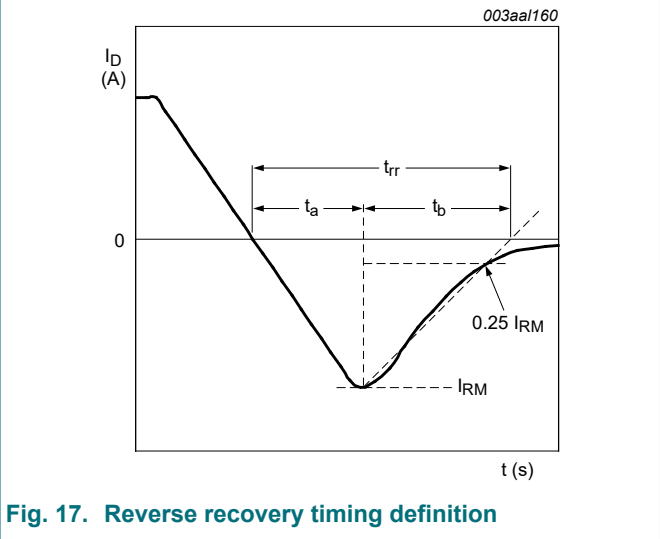


Fig. 17. Reverse recovery timing definition

11. Package outline

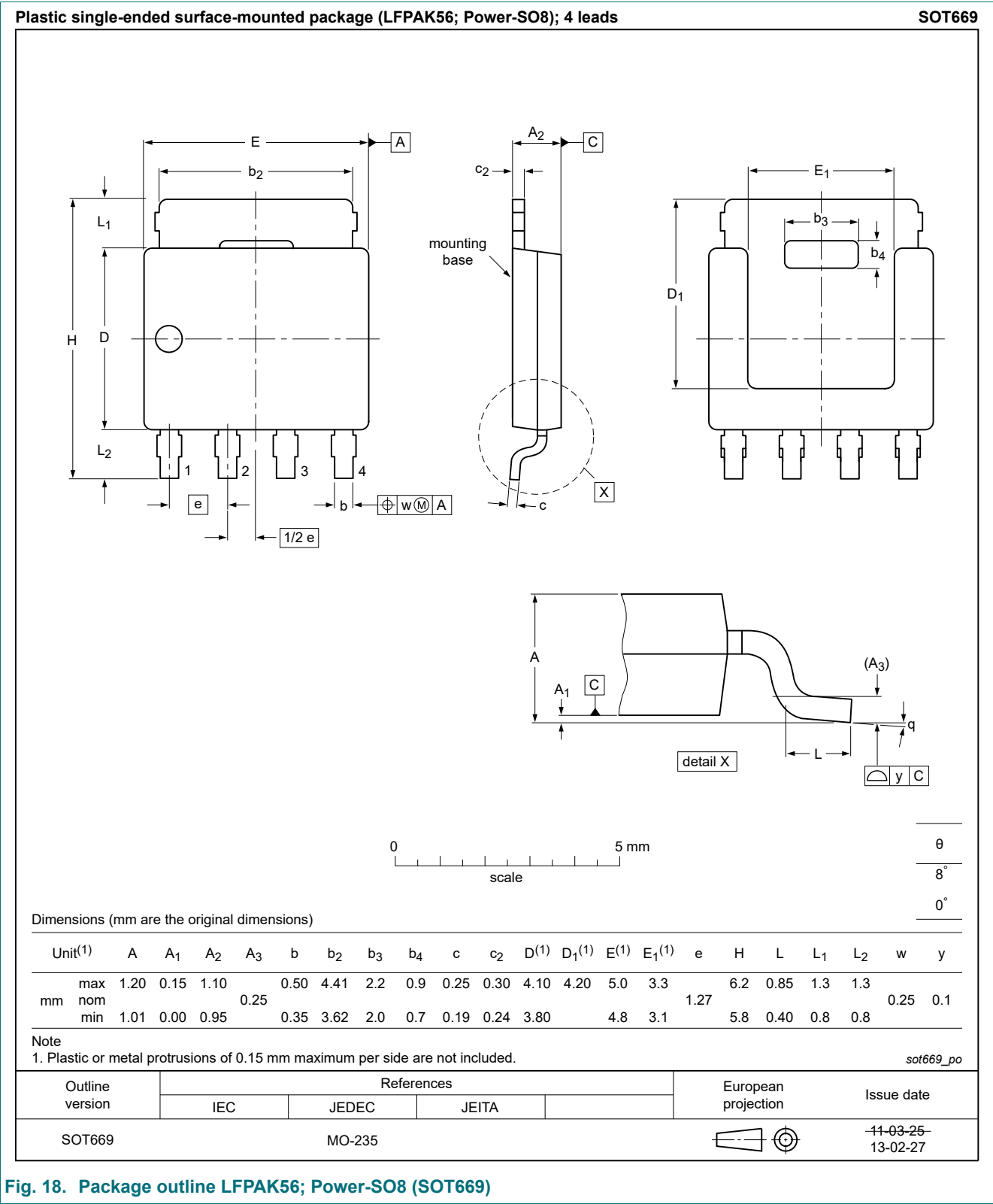


Fig. 18. Package outline LPAK56; Power-SO8 (SOT669)

12. Soldering

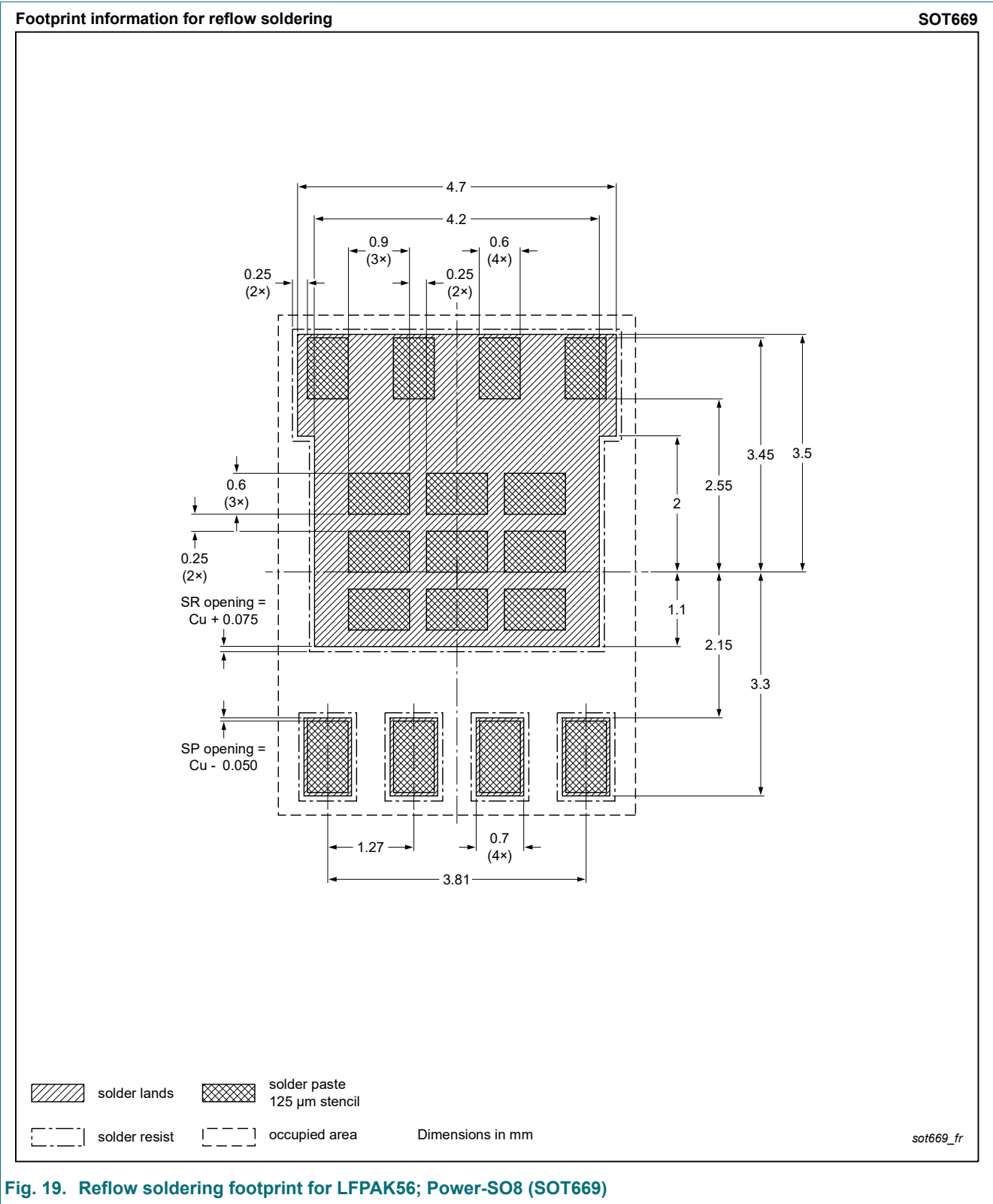


Fig. 19. Reflow soldering footprint for LPAK56; Power-SO8 (SOT669)

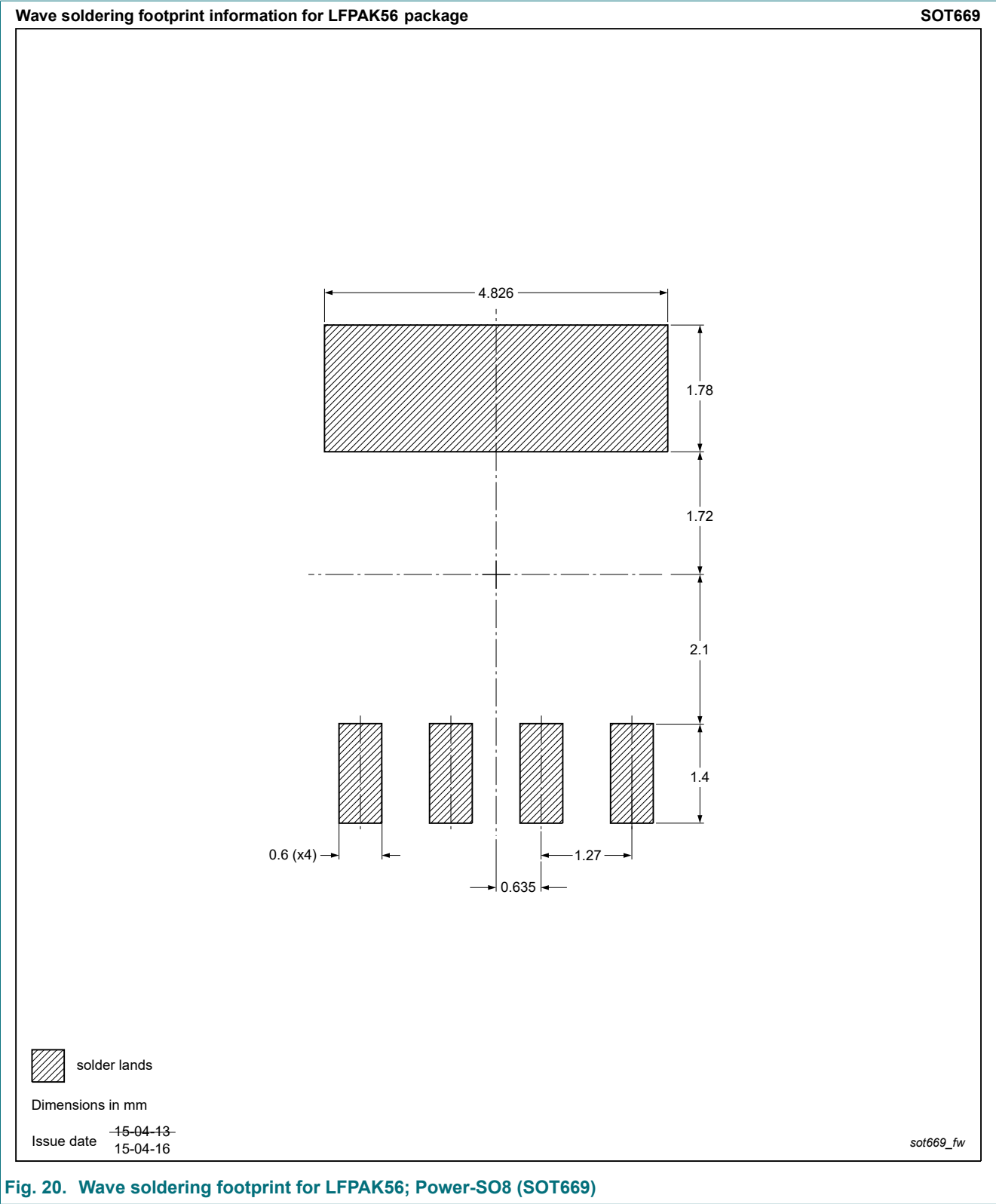


Fig. 20. Wave soldering footprint for LFPAK56; Power-SO8 (SOT669)

13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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