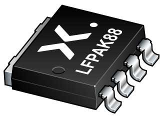


BUK7S1R2-80M

N-channel 80 V, 1.2 mOhm, Standard level MOSFET in LFPAK88

9 October 2023 **Objective data sheet**

1. General description

Automotive qualified N-channel MOSFET using the latest Trench 14 low ohmic split-gate technology, for ultra-low R_{DSon} capability, housed in a LFPAK88 package. This product has been fully designed and qualified to meet AEC-Q101 requirements delivering high performance and endurance.

2. Features and benefits

- Fully automotive qualified to AEC-Q101:
  - 175 °C rating suitable for thermally demanding environments
- Trench 14 split-gate technology:
  - Reduced cell pitch enables enhanced power density and efficiency with lower R_{DSon} in same footprint
  - Fast and efficient switching with high damping and low spiking
- LFPAK Gull Wing leads:
  - High Board Level Reliability absorbing mechanical stress during thermal cycling, unlike traditional QFN packages
  - Visual (AOI) soldering inspection, no need for expensive x-ray equipment
  - Easy solder wetting for good mechanical solder joints
- LFPAK copper clip technology:
  - Improved reliability, with reduced R_{th}, R_{DSon} and package inductance
  - Increases maximum current capability and improved current spreading

3. Applications

- 12 V, 24 V and 48 V automotive systems
- Motor, lighting and solenoid control
- Ultra high-performance power switching

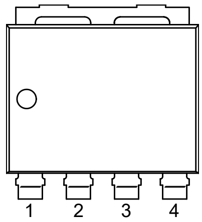
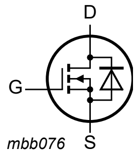
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	-	80	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C		-	-	351	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	341	W
T_j	junction temperature			-55	-	175	°C
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C		[tbd]	1	1.2	mΩ
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 64 V; V_{GS} = 10 V		[tbd]	205	[tbd]	nC

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 LFPAK88 (SOT1235)	
2	S	source		
3	S	source		
4	S	source		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK7S1R2-80M	LFPAK88	plastic, single-ended surface-mounted package (LFPAK88); 4 leads; 2 mm pitch; 8 mm x 8 mm x 1.6 mm body	SOT1235

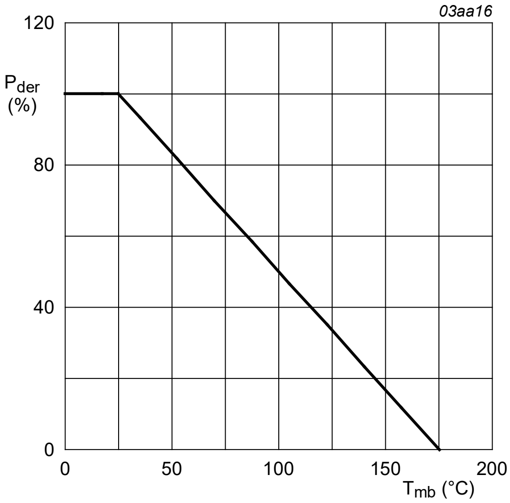
7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). T_j *= 25 °C unless otherwise stated.*

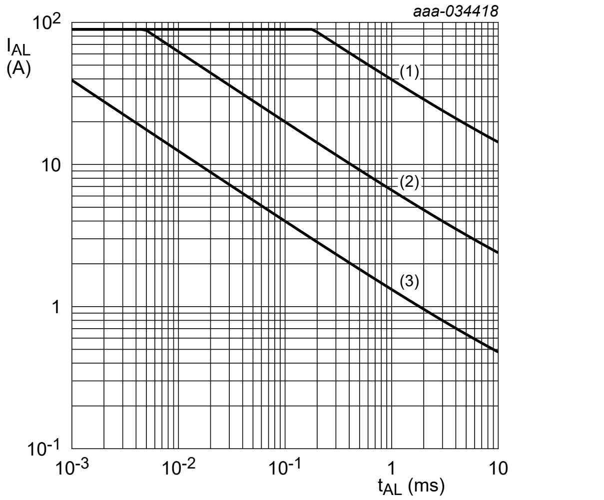
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	80	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	341	W
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C		-	351	A
		V_{GS} = 10 V; T_{mb} = 100 °C		-	248	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	1406	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C		-	284	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	1406	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 92 A; V_{sup} ≤ 80 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 2	[1]	-	878	mJ

[1] Protected by 100% test



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



(1) $T_{j\,(init)}$ = 25 °C; (2) $T_{j\,(init)}$ = 150 °C; (3) Repetitive Avalanche

Fig. 2. Avalanche rating; avalanche current as a function of avalanche time

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 3		-	0.2	0.44	K/W

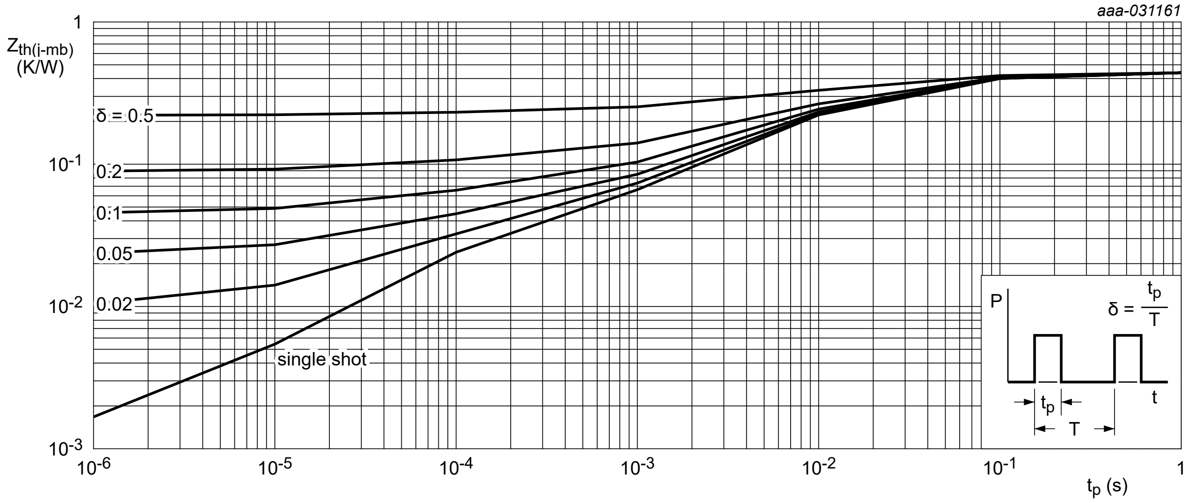


Fig. 3. Transient thermal impedance from junction to mounting base as a function of pulse duration

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		80	89	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -40 °C		[tbd]	86	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		72	85	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 °C		2	3	4	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = 175 °C		1	2	-	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = -55 °C		-	3.4	4.6	V
I_{DSS}	drain leakage current	V_{DS} = 80 V; V_{GS} = 0 V; T_j = 25 °C		-	0.07	1	µA
		V_{DS} = 60 V; V_{GS} = 0 V; T_j = 125 °C		-	[tbd]	[tbd]	µA
		V_{DS} = 80 V; V_{GS} = 0 V; T_j = 125 °C		-	2	100	µA
		V_{DS} = 80 V; V_{GS} = 0 V; T_j = 175 °C		-	-	500	µA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C		[tbd]	1	1.2	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 105 °C		[tbd]	1.6	1.9	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 125 °C		[tbd]	1.7	2.1	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C		[tbd]	2.2	2.8	mΩ
R_G	gate resistance	f = 1 MHz; T_j = 25 °C		[tbd]	0.65	[tbd]	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 64 V; V_{GS} = 10 V		[tbd]	205	[tbd]	nC
		I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V		-	[tbd]	-	nC
Q_{GS}	gate-source charge	I_D = 25 A; V_{DS} = 64 V; V_{GS} = 10 V		[tbd]	62	[tbd]	nC
Q_{GD}	gate-drain charge			[tbd]	42	[tbd]	nC
C_{iss}	input capacitance	V_{DS} = 64 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C		[tbd]	14456	[tbd]	pF
C_{oss}	output capacitance			[tbd]	3305	[tbd]	pF
C_{rss}	reverse transfer capacitance			[tbd]	57	[tbd]	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 64 V; R_L = 2.4 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 5 Ω		-	57	-	ns
t_r	rise time			-	51	-	ns
$t_{d(off)}$	turn-off delay time			-	102	-	ns
t_f	fall time			-	63	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C		-	0.8	1	V
t_{rr}	reverse recovery time	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 40 V; Fig. 4		-	102	-	ns
Q_r	recovered charge			-	85	-	nC

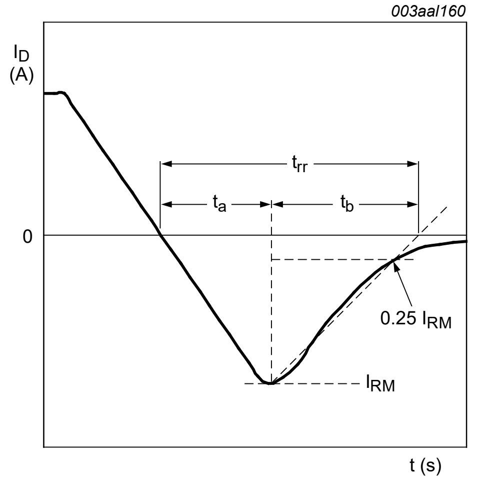
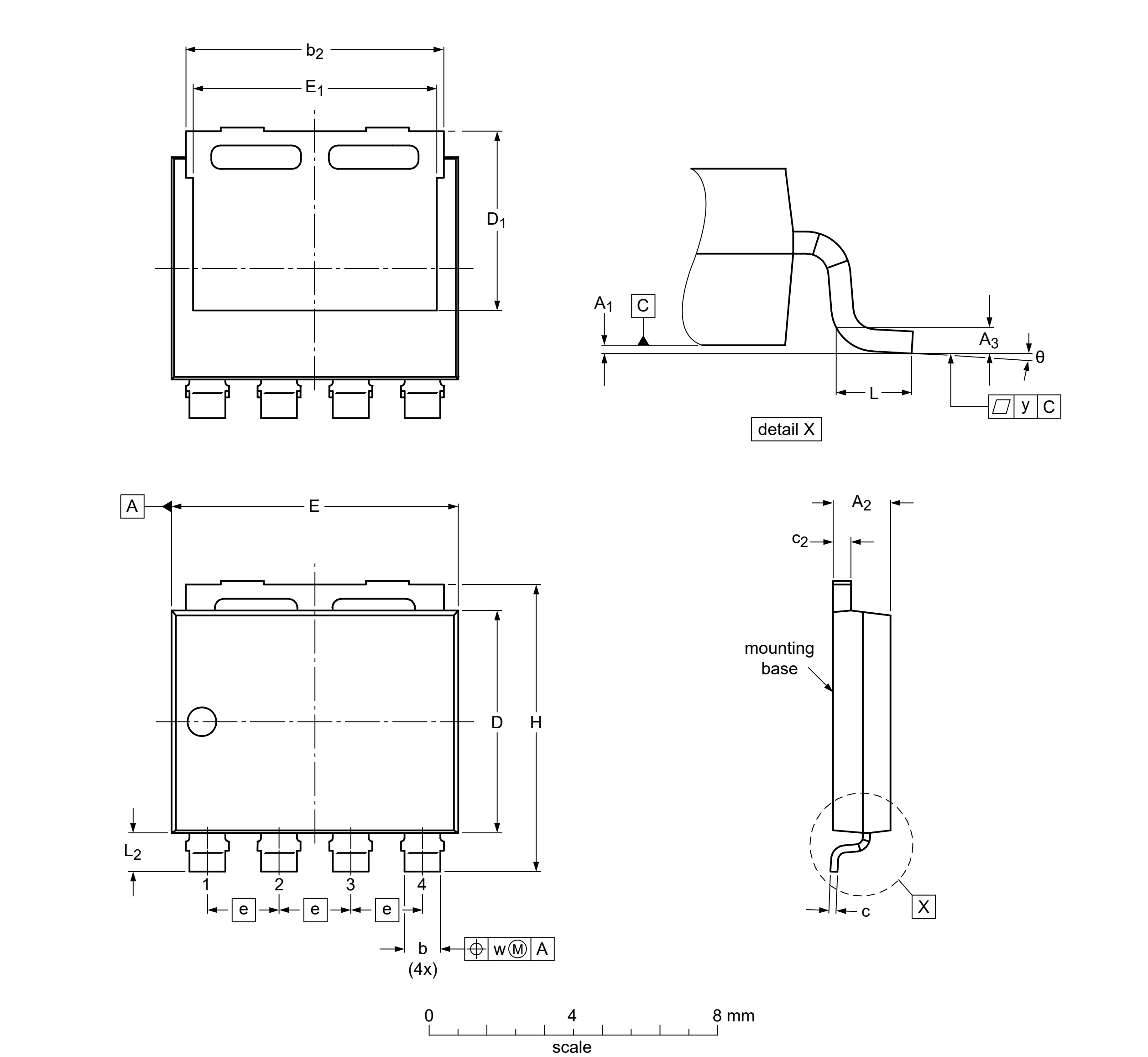


Fig. 4. Reverse recovery timing definition

10. Package outline

Plastic single-ended surface-mounted package (LFPAK88); 4 leads **SOT1235**



Dimensions (mm are the original dimensions)

Unit		A_1	A_2	A_3	b	b_2	c	c_2	D(1)	D_1(1)	E(1)	E_1(1)	e	H(1)	L	L_2	w	y	θ
mm	max	0.15	1.7		1.1	7.3	0.24	0.55	6.3	5.1	8.1	6.9		8.1	0.8	1.3			8°
	nom			0.25									2.0				0.25	0.10	
	min	0.00	1.5		0.9	7.1	0.18	0.45	6.1	4.9	7.9	6.7		7.8	0.6	0.9			0°

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

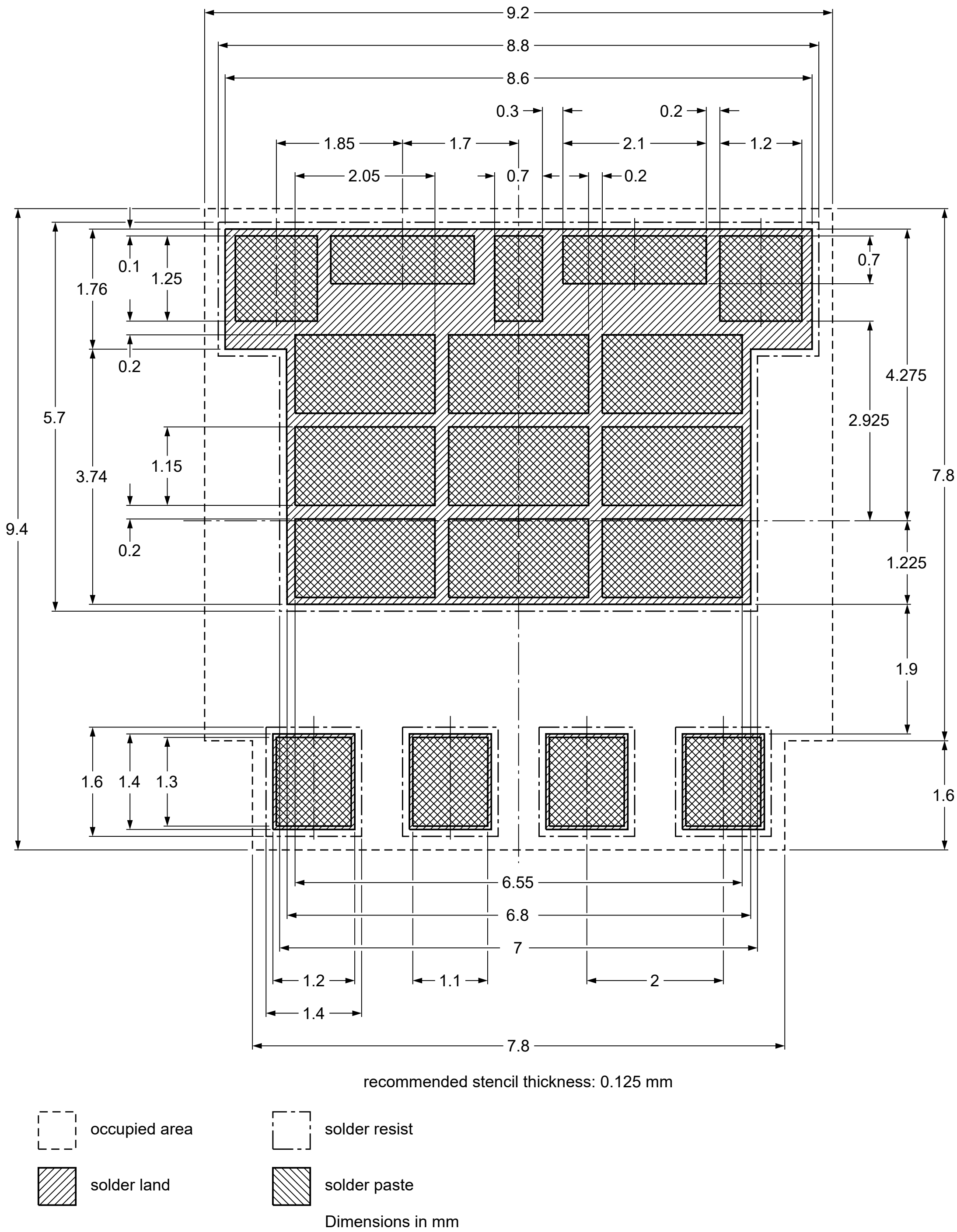
sot1235_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1235						~~17-08-02~~ 17-08-07

Fig. 5. Package outline LFPAK88 (SOT1235)

11. Soldering

Footprint information for reflow soldering of LFPAK88 package **SOT1235**



Issue date ~~18-12-12~~ 18-12-13

sot1235_fr

Fig. 6. Reflow soldering footprint for LFPAK88 (SOT1235)

12. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".
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