1. General description

Automotive qualified standard level N-channel MOSFET in an LFPAK33 package using Trench 9 TrenchMOS technology. This product has been designed and qualified to AEC-Q101 for use in high performance automotive applications.

2. Features and benefits

- Fully automotive qualified to AEC-Q101 at 175 °C
- Trench 9 superjunction technology:
  - Low power losses, high power density
- LFPAK copper clip package technology:
  - High robustness and reliability
  - Gull wing leads for high manufacturability and AOI
- Repetitive avalanche rated

3. Applications

- 12 V automotive systems
- Powertrain, chassis, body and infotainment applications
- Medium/Low power motor drive
- DC-DC systems
- LED lighting

4. Quick reference data

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DS}$</td>
<td>drain-source voltage</td>
<td>$25 , ^\circ C \leq T_{j} \leq 175 , ^\circ C$</td>
<td>-</td>
<td>-</td>
<td>40</td>
<td>V</td>
</tr>
<tr>
<td>$I_D$</td>
<td>drain current</td>
<td>$V_{GS} = 10 , V$; $T_{mb} = 25 , ^\circ C$; Fig. 2</td>
<td>-</td>
<td>-</td>
<td>80</td>
<td>A</td>
</tr>
<tr>
<td>$P_{tot}$</td>
<td>total power dissipation</td>
<td>$T_{mb} = 25 , ^\circ C$; Fig. 1</td>
<td>-</td>
<td>-</td>
<td>101</td>
<td>W</td>
</tr>
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</table>

Static characteristics

- $R_{DSon}$: drain-source on-state resistance
- $V_{GS} = 10 \, V$; $I_D = 25 \, A$; $T_{j} = 25 \, ^\circ C$; Fig. 11
- 1.8 2.6 3.3 mΩ

Dynamic characteristics

- $Q_{GD}$: gate-drain charge
- $I_D = 25 \, A$; $V_{DS} = 32 \, V$; $V_{GS} = 10 \, V$; Fig. 13; Fig. 14
- - 6.6 13.2 nC

Source-drain diode

- $Q_r$: recovered charge
- $I_S = 25 \, A$; $dI_S/dt = -100 \, A/\mu s$; $V_{GS} = 0 \, V$; $V_{DS} = 20 \, V$; Fig. 17
- - 21 - nC
N-channel 40 V, 3.3 mΩ standard level MOSFET in LFPAK33

<table>
<thead>
<tr>
<th>Symbol</th>
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<th>Conditions</th>
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<th>Typ</th>
<th>Max</th>
<th>Unit</th>
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</thead>
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<tr>
<td>S</td>
<td>softness factor</td>
<td>(I_S = 25 \text{ A}; \frac{\text{d}I_S}{\text{d}t} = -100 \text{ A/µs}; V_{GS} = 0 \text{ V}; V_{DS} = 20 \text{ V}; T_j = 25 ^\circ \text{C}; \text{Fig. 16} )</td>
<td>-</td>
<td>0.68</td>
<td>-</td>
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[1] 80A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

5. Pinning information

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<th>Graphic symbol</th>
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<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>S</td>
<td>source</td>
<td></td>
<td></td>
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<tr>
<td>3</td>
<td>S</td>
<td>source</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>G</td>
<td>gate</td>
<td></td>
<td></td>
</tr>
<tr>
<td>mb</td>
<td>D</td>
<td>Mounting base; connected to drain</td>
<td>LFPAK33 (SOT1210)</td>
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6. Ordering information

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<td>BUK7M3R3-40H</td>
<td>LFPAK33</td>
<td>Plastic, single ended surface mounted package (LFPAK33); 8 leads; 0.65 mm pitch</td>
<td>SOT1210</td>
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7. Marking

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8. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

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</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Parameter</td>
<td>Conditions</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>V_{DS}</td>
<td>drain-source voltage</td>
<td>25 °C ≤ T_j ≤ 175 °C</td>
<td>-</td>
<td>40 V</td>
</tr>
<tr>
<td></td>
<td>V_{GS}</td>
<td>gate-source voltage</td>
<td>DC; T_j ≤ 175 °C</td>
<td>-10</td>
<td>20 V</td>
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<tr>
<td></td>
<td>P_{tot}</td>
<td>total power dissipation</td>
<td>T_{mb} = 25 °C; \text{Fig. 1}</td>
<td>-101</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td>I_D</td>
<td>drain current</td>
<td>(V_{GS} = 10 \text{ V}; T_{mb} = 25 ^\circ \text{C}; \text{Fig. 2} )</td>
<td>[1]</td>
<td>80 A</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>(V_{GS} = 10 \text{ V}; T_{mb} = 100 ^\circ \text{C}; \text{Fig. 2} )</td>
<td>-</td>
<td>80 A</td>
</tr>
<tr>
<td></td>
<td>I_{DM}</td>
<td>peak drain current</td>
<td>pulsed; (t_p ≤ 10 \mu\text{s}; T_{mb} = 25 ^\circ \text{C}; \text{Fig. 3} )</td>
<td>[1]</td>
<td>475 A</td>
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<tr>
<td></td>
<td>T_{stg}</td>
<td>storage temperature</td>
<td>-55</td>
<td>175</td>
<td>°C</td>
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<td></td>
<td>T_j</td>
<td>junction temperature</td>
<td>-55</td>
<td>175</td>
<td>°C</td>
</tr>
</tbody>
</table>

Source-drain diode
**Nexperia**

**BUK7M3R3-40H**

N-channel 40 V, 3.3 mΩ standard level MOSFET in LFPAK33

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
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<td>$I_S$</td>
<td>source current</td>
<td>$T_{mb} = 25 , ^\circ C$</td>
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<td>80</td>
<td>A</td>
</tr>
<tr>
<td>$I_{SM}$</td>
<td>peak source current</td>
<td>pulsed; $t_p \leq 10 , \mu s$; $T_{mb} = 25 , ^\circ C$</td>
<td>-</td>
<td>475</td>
<td>A</td>
</tr>
</tbody>
</table>

**Avalanche ruggedness**

| $E_{DS(AL)}$ | non-repetitive drain-source avalanche energy | $I_D = 80 \, A$; $V_{sup} \leq 40 \, V$; $R_{GS} = 50 \, \Omega$; $V_{GS} = 10 \, V$; $T_{j(init)} = 25 \, ^\circ C$; unclamped; [2] [3] | - | 57 | mJ |

[1] 80A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

[2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.


---

![Fig. 1](aaa-028618)  
Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25\,^\circ C)}} \times 100\%$$

![Fig. 2](aaa-028618)  
Continuous drain current as a function of mounting base temperature

$V_{GS} \geq 10 \, V$

(1) 80A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

![Fig. 3](aaa-028608)  
Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25 \, ^\circ C$; $I_{SM}$ is a single pulse
9. Thermal characteristics

Table 6. Thermal characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{th(j-mb)}$</td>
<td>thermal resistance from junction to mounting base</td>
<td>Fig. 5</td>
<td>-</td>
<td>1.3</td>
<td>1.48</td>
<td>K/W</td>
</tr>
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</table>

Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{(BR)DSS}$</td>
<td>drain-source breakdown voltage</td>
<td>$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 ^\circ C$</td>
<td>40</td>
<td>43</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -40 ^\circ C$</td>
<td>-</td>
<td>40.5</td>
<td>-</td>
<td>V</td>
</tr>
</tbody>
</table>
### Symbol | Parameter | Conditions | Min | Typ | Max | Unit
--- | --- | --- | --- | --- | --- | ---
| | | \( I_D = 250 \mu A; V_{GS} = 0 \text{ V}; T_j = -55 ^\circ C \) | 36 | 40 | - | V
| \( V_{GS(th)} \) | gate-source threshold voltage | \( I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 ^\circ C; \text{ Fig. 9; Fig. 10} \) | 2.4 | 3 | 3.6 | V
| | | \( I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 ^\circ C; \text{ Fig. 9} \) | - | - | 4.3 | V
| | | \( I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 175 ^\circ C; \text{ Fig. 9} \) | 1 | - | - | V
| \( I_{DSS} \) | drain leakage current | \( V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 ^\circ C \) | - | 0.07 | 1 | \( \mu A \)
| | | \( V_{DS} = 16 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 ^\circ C \) | - | 0.94 | 10 | \( \mu A \)
| | | \( V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 ^\circ C \) | - | 80 | 500 | \( \mu A \)
| \( I_{GSS} \) | gate leakage current | \( V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 ^\circ C \) | - | 2 | 100 | nA
| | | \( V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 ^\circ C \) | - | 2 | 100 | nA
| \( R_{DSon} \) | drain-source on-state resistance | \( V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 ^\circ C; \text{ Fig. 11} \) | 1.8 | 2.6 | 3.3 | m\( \Omega \)
| | | \( V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 105 ^\circ C; \text{ Fig. 12} \) | 2.5 | 4 | 5.3 | m\( \Omega \)
| | | \( V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 125 ^\circ C; \text{ Fig. 12} \) | 2.8 | 4.4 | 5.8 | m\( \Omega \)
| | | \( V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 ^\circ C; \text{ Fig. 12} \) | 3.5 | 5.5 | 7.2 | m\( \Omega \)
| \( R_G \) | gate resistance | \( f = 1 \text{ MHz}; T_j = 25 ^\circ C \) | 0.3 | 0.8 | 2 | \( \Omega \)

#### Dynamic characteristics

| \( Q_{G(tot)} \) | total gate charge | \( I_D = 25 \text{ A}; V_{DS} = 32 \text{ V}; V_{GS} = 10 \text{ V}; \text{ Fig. 13; Fig. 14} \) | - | 32 | 45 | nC
| \( Q_{GS} \) | gate-source charge | | - | 9 | 14 | nC
| \( Q_{GD} \) | gate-drain charge | | - | 6.6 | 13.2 | nC
| \( C_{iss} \) | input capacitance | \( V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25 ^\circ C; \text{ Fig. 15} \) | - | 2169 | 3037 | pF
| \( C_{oss} \) | output capacitance | \( V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25 ^\circ C; \text{ Fig. 15} \) | - | 592 | 829 | pF
| \( C_{rss} \) | reverse transfer capacitance | | - | 113 | 250 | pF
| \( t_{d(on)} \) | turn-on delay time | \( V_{DS} = 30 \text{ V}; R_L = 1.2 \Omega; V_{GS} = 10 \text{ V}; R_{G(ext)} = 5 \Omega \) | - | 8.4 | - | ns
| \( t_r \) | rise time | | - | 7.3 | - | ns
| \( t_{d(off)} \) | turn-off delay time | | - | 19 | - | ns
| \( t_f \) | fall time | | - | 9.1 | - | ns

#### Source-drain diode

| \( V_{SD} \) | source-drain voltage | \( I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 ^\circ C; \text{ Fig. 16} \) | - | 0.82 | 1.2 | V
| \( t_{rr} \) | reverse recovery time | \( I_S = 25 \text{ A}; \text{ dI}_S/\text{dt} = -100 \text{ A}/\mu \text{s}; V_{GS} = 0 \text{ V}; V_{DS} = 20 \text{ V} \) | - | 27 | - | ns
| \( Q_r \) | recovered charge | \( I_S = 25 \text{ A}; \text{ dI}_S/\text{dt} = -100 \text{ A}/\mu \text{s}; V_{GS} = 0 \text{ V}; V_{DS} = 20 \text{ V}; \text{ Fig. 17} \) | - | 21 | - | nC
| \( S \) | softness factor | \( I_S = 25 \text{ A}; \text{ dI}_S/\text{dt} = -100 \text{ A}/\mu \text{s}; V_{GS} = 0 \text{ V}; V_{DS} = 20 \text{ V}; T_j = 25 ^\circ C; \text{ Fig. 16} \) | - | 0.68 | - | 
| | | \( I_S = 25 \text{ A}; \text{ dI}_S/\text{dt} = -500 \text{ A}/\mu \text{s}; V_{DS} = 0 \text{ V}; V_{DS} = 20 \text{ V}; T_j = 25 ^\circ C; \text{ Fig. 16} \) | - | 0.49 | - | 

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Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

Fig. 9. Gate-source threshold voltage as a function of junction temperature
N-channel 40 V, 3.3 mΩ standard level MOSFET in LFPAK33

**Fig. 10.** Sub-threshold drain current as a function of gate-source voltage

\[ I_D \text{ (A)} \]
\[ V_{GS} \text{ (V)} \]
\[ 10^{-1} \]
\[ 10^{-2} \]
\[ 10^{-3} \]
\[ 10^{-4} \]
\[ 10^{-5} \]
\[ 10^{-6} \]
\[ 0 \]
\[ 1 \]
\[ 2 \]
\[ 3 \]
\[ 4 \]
\[ 5 \]
\[ T_j = 25 \degree C; V_{DS} = 5 \text{ V} \]

**Fig. 11.** Drain-source on-state resistance as a function of drain current; typical values

\[ R_{DSon} \text{ (mΩ)} \]
\[ I_D \text{ (A)} \]
\[ 0 \]
\[ 20 \]
\[ 40 \]
\[ 60 \]
\[ 80 \]
\[ 100 \]
\[ 120 \]
\[ 4.5 \text{ V} \]
\[ 5 \text{ V} \]
\[ 5.5 \text{ V} \]
\[ 6 \text{ V} \]
\[ V_{GS} \leq 10 \text{ V} \]

**Fig. 12.** Normalized drain-source on-state resistance factor as a function of junction temperature

\[ a = \frac{R_{DSon}}{R_{DSon} (25 \degree C)} \]
\[ T_j \text{ (°C)} \]
\[ 0 \]
\[ 10 \]
\[ 20 \]
\[ 30 \]
\[ 40 \]
\[ 50 \]
\[ 60 \]
\[ 70 \]
\[ 80 \]
\[ 90 \]
\[ 100 \]
\[ 110 \]
\[ 120 \]
\[ 130 \]
\[ 140 \]
\[ 150 \]
\[ 160 \]
\[ 170 \]
\[ 180 \]

**Fig. 13.** Gate-source voltage as a function of gate charge; typical values

\[ V_{GS} \text{ (V)} \]
\[ V_{DS} = 14 \text{ V} \]
\[ 32 \text{ V} \]
\[ V_{DS} \leq 14 \text{ V} \]

\[ Q_G \text{ (nC)} \]
\[ 0 \]
\[ 2 \]
\[ 4 \]
\[ 6 \]
\[ 8 \]
\[ 10 \]
\[ 12 \]
\[ 14 \]
\[ 16 \]
\[ 18 \]

\[ T_j = 25 \degree C; I_D = 25 \text{ A} \]
Fig. 14. Gate charge waveform definitions

Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

Fig. 17. Reverse recovery timing definition
11. Package outline

Plastic single ended surface mounted package (LFPAK33); 8 leads  SOT1210

Dimensions

<table>
<thead>
<tr>
<th>Unit(1)</th>
<th>A</th>
<th>A₁</th>
<th>b(1)</th>
<th>b₁(1)</th>
<th>c</th>
<th>c₁</th>
<th>D ref</th>
<th>D₁</th>
<th>D₂</th>
<th>E(1)</th>
<th>E₁</th>
<th>e</th>
<th>e₁</th>
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<th>L</th>
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<th>w</th>
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<td>0.00</td>
<td>0.25</td>
<td>2.00</td>
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<td>2.00</td>
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<td>0.13</td>
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<td>0.30</td>
<td>0.20</td>
<td>0.10</td>
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Note:
1. Plastic or metal protrusions of 0.15 mm per side are not included.

Fig. 18. Package outline LFPAK33 (SOT1210)
12. Legal information

Data sheet status

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<tbody>
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<td>Objective [short] data sheet</td>
<td>Development</td>
<td>This document contains data from the objective specification for product development.</td>
</tr>
<tr>
<td>Preliminary [short] data sheet</td>
<td>Qualification</td>
<td>This document contains data from the preliminary specification.</td>
</tr>
<tr>
<td>Product [short] data sheet</td>
<td>Production</td>
<td>This document contains the product specification.</td>
</tr>
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</table>

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term "short data sheet" is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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BUK7M3R3-40H

N-channel 40 V, 3.3 mΩ standard level MOSFET in LFPAK33

Product data sheet 29 January 2019

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