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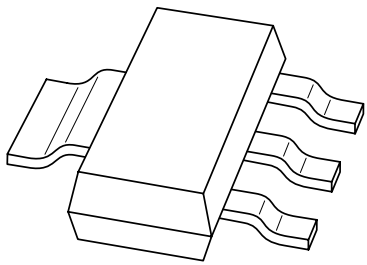
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Kind regards,

Team Nexperia

# DATA SHEET



## **BSP89**

**N-channel enhancement mode  
vertical D-MOS transistor**

Product specification  
Supersedes data of 1997 Jun 23

2001 May 18

# N-channel enhancement mode vertical D-MOS transistor

**BSP89**

## FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

## DESCRIPTION

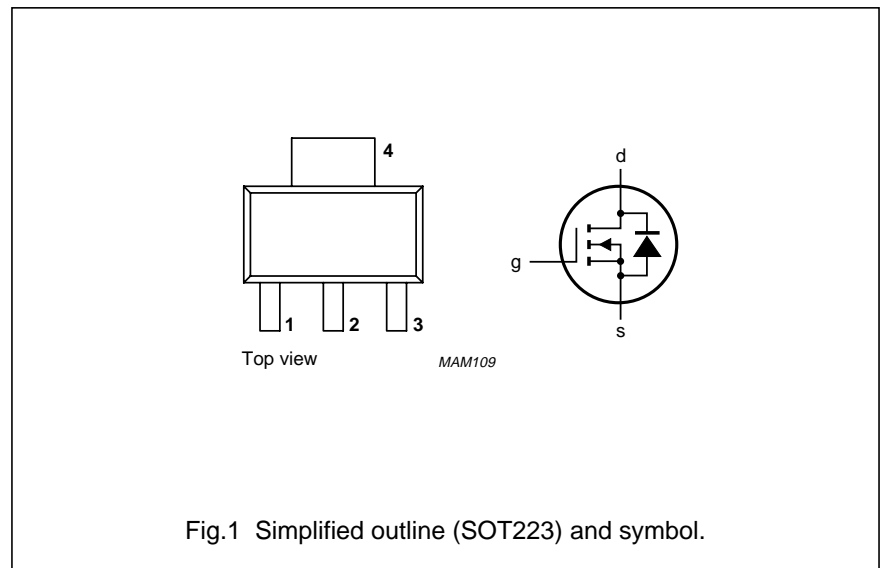
N-channel enhancement mode vertical D-MOS transistor in a SOT223 package, intended for use as a surface-mounted device in line current interrupters in telephone sets and for application in relay, high speed and line transformer drivers.

## PINNING - SOT223

PIN	DESCRIPTION
Code: BSP89	
1	gate
2	drain
3	source
4	drain

## QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
$V_{DS}$	drain-source voltage (DC)	240	V
$V_{GSth}$	gate-source threshold voltage	2	V
$I_D$	drain current (DC)	375	mA
$R_{DSon}$	drain-source on-state resistance	5	$\Omega$



## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	drain-source voltage (DC)		–	240	V
$V_{GSO}$	gate-source voltage (DC)	open drain	–	$\pm 20$	V
$I_D$	drain current (DC)		–	375	mA
$I_{DM}$	peak drain current		–	1.5	A
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ }^\circ\text{C}$ ; note 1	–	1.5	W
$T_{stg}$	storage temperature		–55	+150	$^\circ\text{C}$
$T_j$	junction temperature		–	150	$^\circ\text{C}$

## Note

1. Transistor mounted on an epoxy printed circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 cm<sup>2</sup>.

# N-channel enhancement mode vertical D-MOS transistor

BSP89

## THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient; note 1	83.3	K/W

### Note

1. Transistor mounted on an epoxy printed circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 cm<sup>2</sup>.

## CHARACTERISTICS

$T_j = 25\text{ °C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 10\ \mu\text{A}; V_{GS} = 0$	240	–	–	V
$I_{DSS}$	drain-source leakage current	$V_{DS} = 60\ \text{V}; V_{GS} = 0$	–	–	200	nA
$I_{GSS}$	gate-source leakage current	$V_{GS} = \pm 20\ \text{V}; V_{DS} = 0$	–	–	100	nA
$V_{GSth}$	gate-source threshold voltage	$I_D = 1\ \text{mA}; V_{GS} = V_{DS}$	0.8	–	2	V
$R_{DSon}$	drain-source on-state resistance	$I_D = 340\ \text{mA}; V_{GS} = 10\ \text{V}$	–	2.8	5	$\Omega$
		$I_D = 340\ \text{mA}; V_{GS} = 4.5\ \text{V}$	–	–	7.5	$\Omega$
$ Y_{fs} $	transfer admittance	$I_D = 340\ \text{mA}; V_{DS} = 25\ \text{V}$	140	600	–	mS
$C_{iss}$	input capacitance	$V_{DS} = 25\ \text{V}; V_{GS} = 0; f = 1\ \text{MHz}$	–	100	120	pF
$C_{oss}$	output capacitance	$V_{DS} = 25\ \text{V}; V_{GS} = 0; f = 1\ \text{MHz}$	–	20	30	pF
$C_{rss}$	reverse transfer capacitance	$V_{DS} = 25\ \text{V}; V_{GS} = 0; f = 1\ \text{MHz}$	–	10	15	pF
<b>Switching times (see Figs 3 and 4)</b>						
$t_{on}$	turn-on time	$I_D = 250\ \text{mA}; V_{DD} = 50\ \text{V}; V_{GS} = 0\ \text{to}\ 10\ \text{V}$	–	6	10	ns
$t_{off}$	turn-off time	$I_D = 250\ \text{mA}; V_{DD} = 50\ \text{V}; V_{GS} = 0\ \text{to}\ 10\ \text{V}$	–	47	60	ns

N-channel enhancement mode vertical D-MOS transistor

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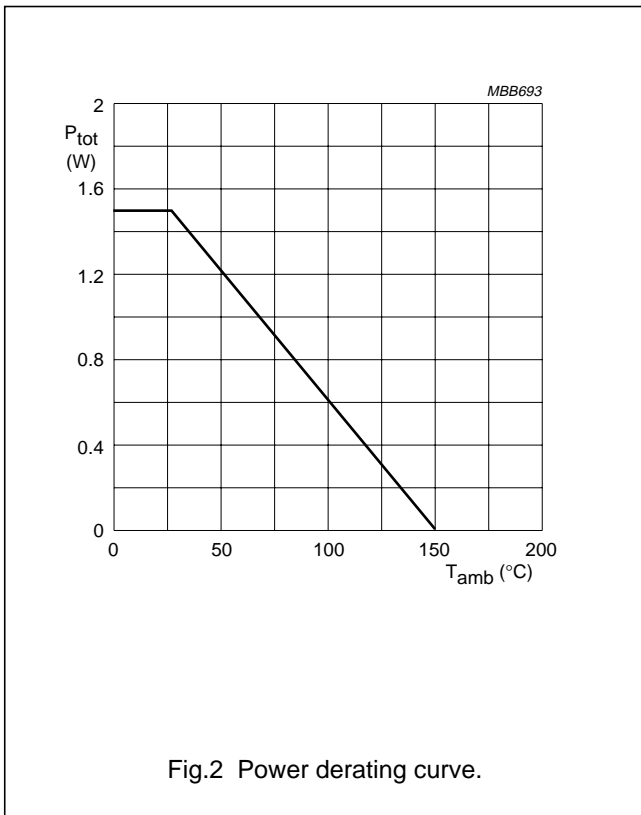


Fig.2 Power derating curve.

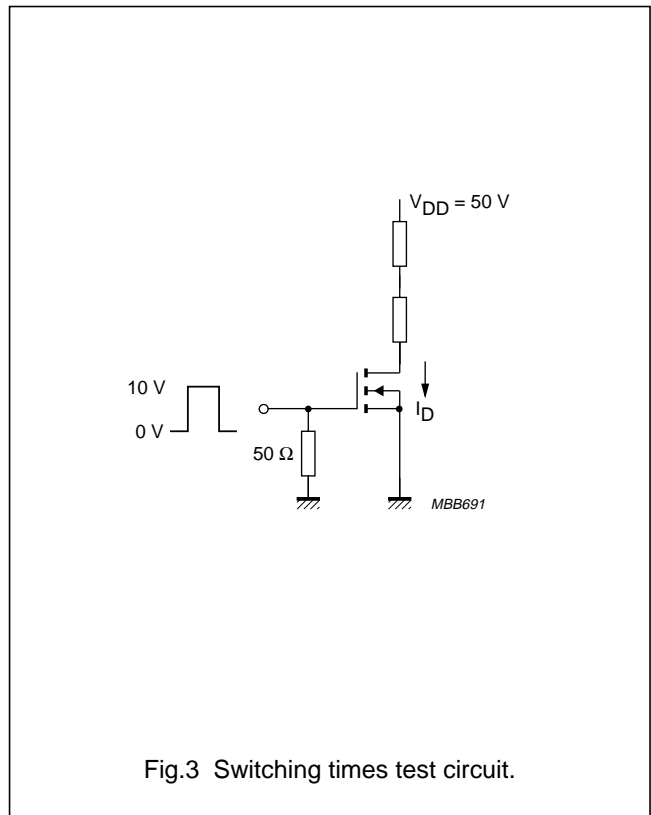


Fig.3 Switching times test circuit.

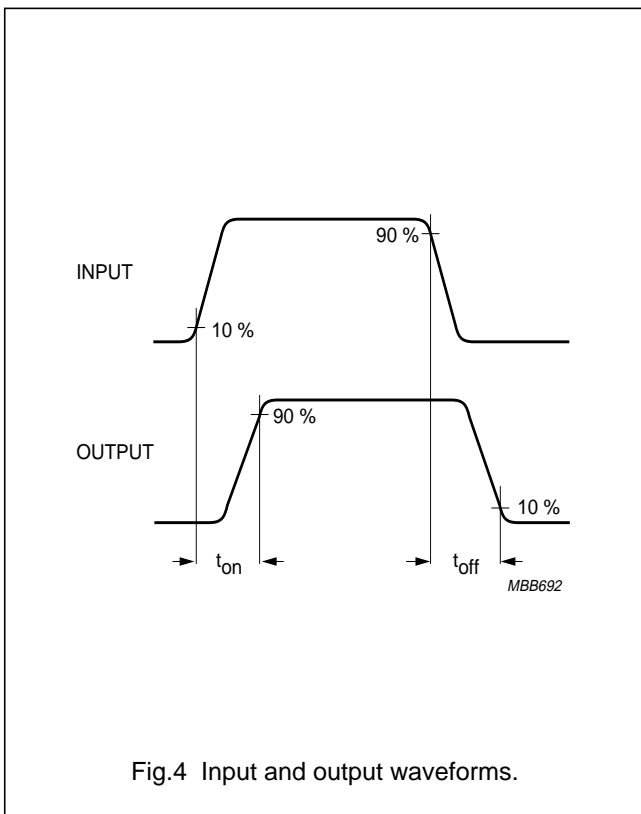


Fig.4 Input and output waveforms.

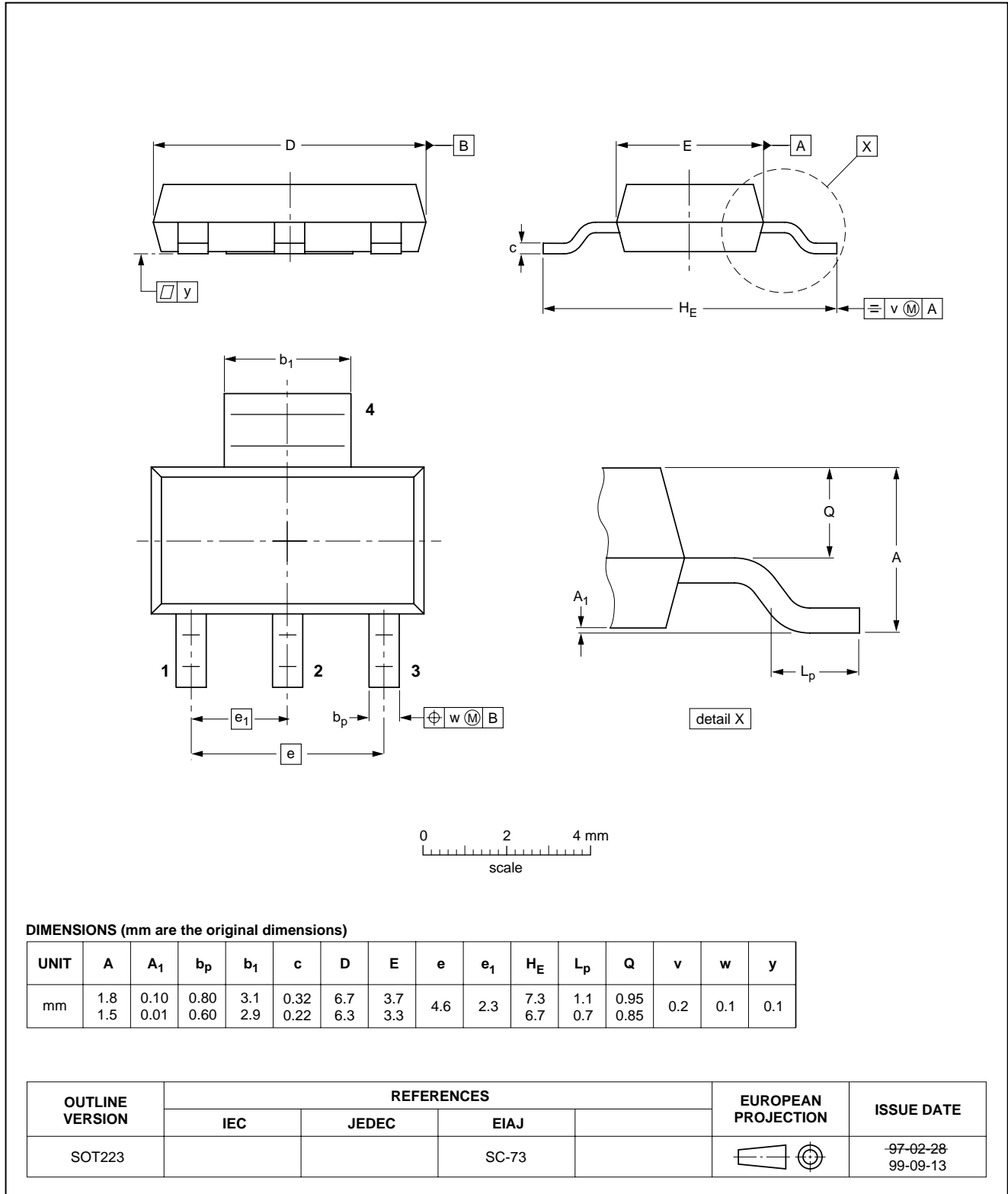
N-channel enhancement mode  
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PACKAGE OUTLINE

Plastic surface mounted package; collector pad for good heat transfer; 4 leads

SOT223



# N-channel enhancement mode vertical D-MOS transistor

BSP89

## DATA SHEET STATUS

DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)</sup>	DEFINITIONS
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N-channel enhancement mode  
vertical D-MOS transistor

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BSP89

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