



# 74LVT162244B-Q100

3.3 V 16-bit buffer/driver with 30  $\Omega$  termination resistors;  
3-state

Rev. 1 — 6 November 2025

Product data sheet

## 1. General description

The 74LVT162244B-Q100 is a 16-bit buffer/line driver with 3-state outputs. The device can be used as four 4-bit buffers, two 8-bit buffers or one 16-bit buffer. The device features four output enables (1OE, 2OE, 3OE and 4OE), each controlling four of the 3-state outputs. A HIGH on nOE causes the outputs to assume a high-impedance OFF-state. Bus hold data inputs eliminate the need for external pull-up resistors to define unused inputs.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 3) and is suitable for use in automotive applications.

## 2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 3)
  - Specified from -40 °C to +85 °C
- 16-bit bus interface
- 3-state buffers
- Outputs include series resistance of 30  $\Omega$  making external termination resistors unnecessary
- Output capability: +12 mA/-12 mA
- Wide supply voltage range from 2.7 V to 3.6 V
- BiCMOS high speed and output drive
- Direct interface with TTL levels
- Overvoltage tolerant inputs to 5.5 V
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up 3-state
- No bus current loading when output is tied to 5 V bus
- I<sub>OFF</sub> circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 500 mA per JESD 78 Class II Level B
- Complies with JEDEC standard JESD8C (2.7 V to 3.6 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

## 3. Ordering information

Table 1. Ordering information

| Type number                          | Package           |         |   |                          |
|--------------------------------------|-------------------|---------|---|--------------------------|
|                                      | Temperature range | Name    | Description   | Version                  |
| <a href="#">74LVT162244BDGG-Q100</a> | -40 °C to +85 °C  | TSSOP48 | plastic thin shrink small outline package;<br>48 leads; body width 6.1 mm | <a href="#">SOT362-1</a> |

4. Functional diagram

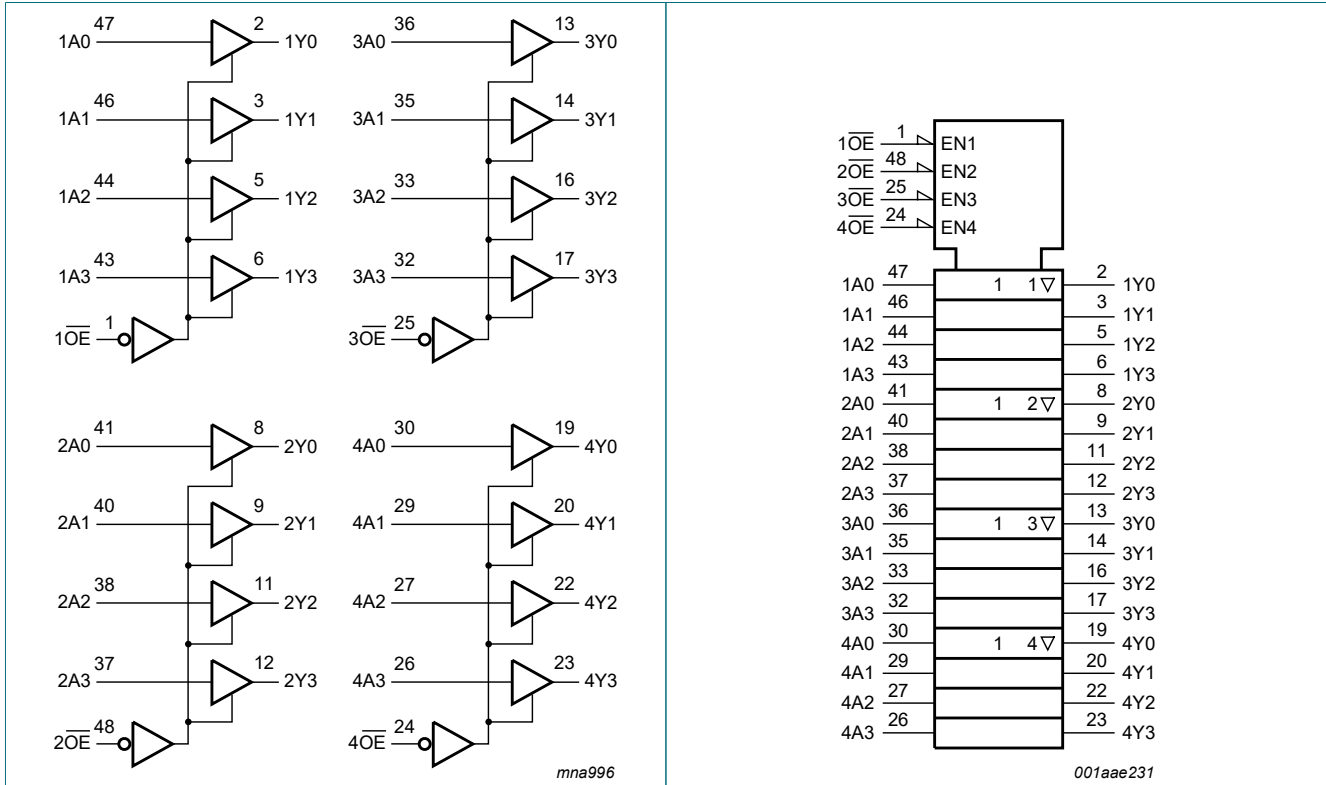


Fig. 1. Logic symbol

Fig. 2. IEC logic symbol

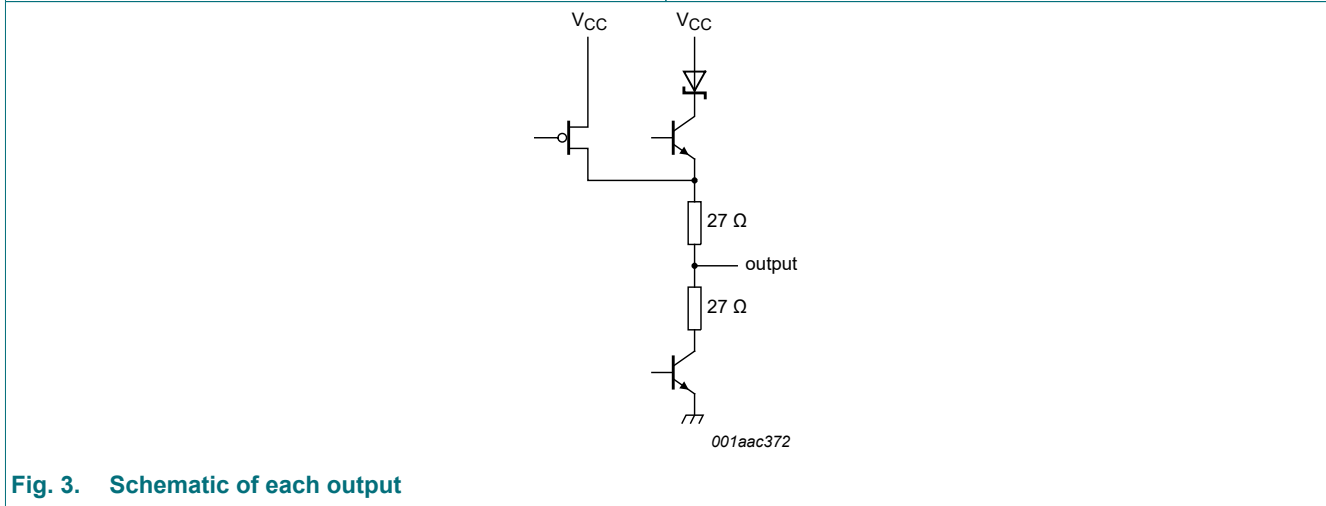
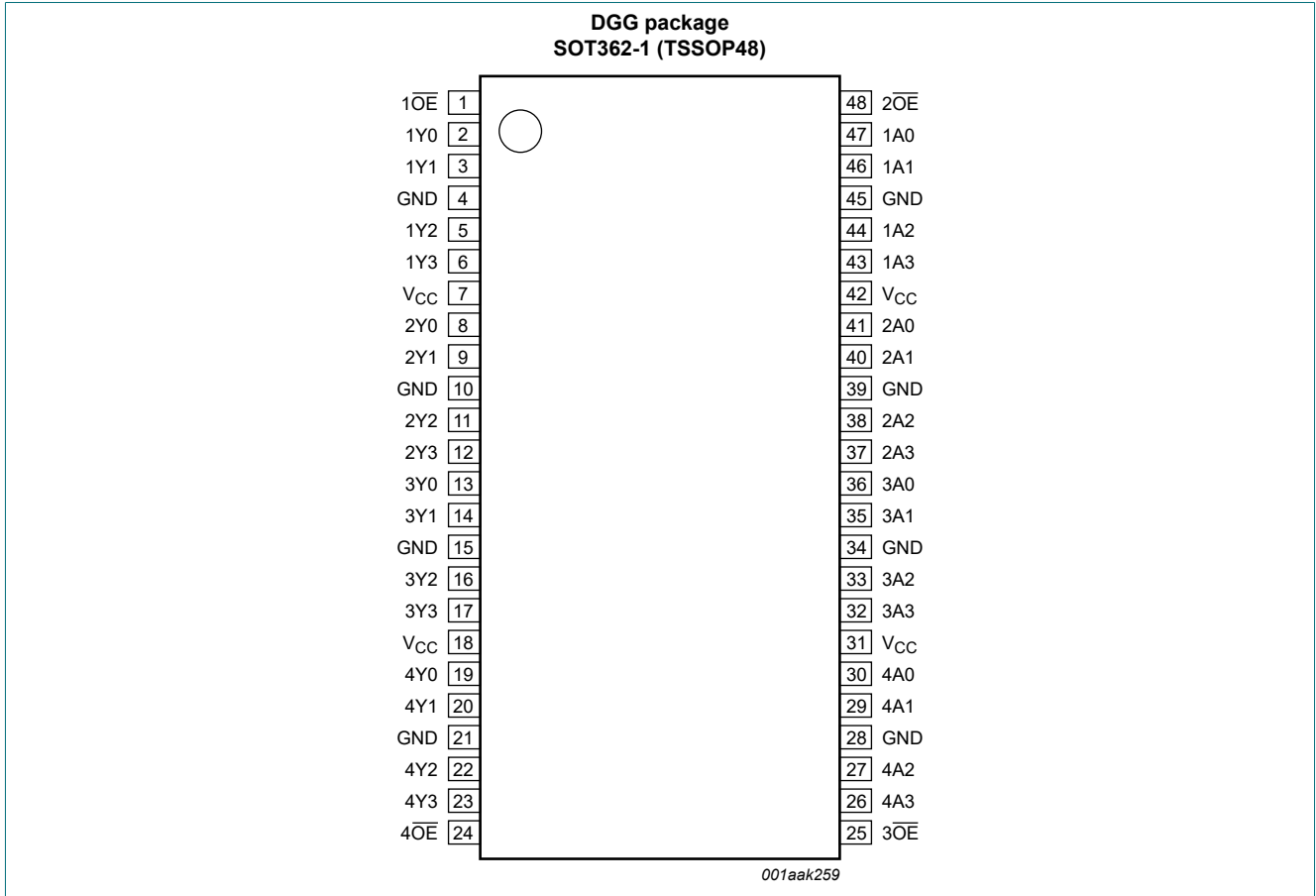


Fig. 3. Schematic of each output

## 5. Pinning information

### 5.1. Pinning



### 5.2. Pin description

Table 2. Pin description

| Symbol             | Pin                           | Description                       |
|--------------------|-------------------------------|-----------------------------------|
| 1OE, 2OE, 3OE, 4OE | 1, 48, 25, 24                 | output enable inputs (active LOW) |
| 1A0, 1A1, 1A2, 1A3 | 47, 46, 44, 43                | data inputs                       |
| 2A0, 2A1, 2A2, 2A3 | 41, 40, 38, 37                | data inputs                       |
| 3A0, 3A1, 3A2, 3A3 | 36, 35, 33, 32                | data inputs                       |
| 4A0, 4A1, 4A2, 4A3 | 30, 29, 27, 26                | data inputs                       |
| 1Y0, 1Y1, 1Y2, 1Y3 | 2, 3, 5, 6                    | data outputs                      |
| 2Y0, 2Y1, 2Y2, 2Y3 | 8, 9, 11, 12                  | data outputs                      |
| 3Y0, 3Y1, 3Y2, 3Y3 | 13, 14, 16, 17                | data outputs                      |
| 4Y0, 4Y1, 4Y2, 4Y3 | 19, 20, 22, 23                | data outputs                      |
| GND                | 4, 10, 15, 21, 28, 34, 39, 45 | ground (0 V)                      |
| VCC                | 7, 18, 31, 42                 | supply voltage                    |

## 6. Functional description

**Table 3. Function table**

*H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.*

| Input |     | Output |
|-------|-----|--------|
| nOE   | nAn | nYn    |
| L     | L   | L      |
| L     | H   | H      |
| H     | X   | Z      |

## 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol    | Parameter               | Conditions                        | Min      | Max  | Unit         |
|-----------|-------------------------|-----------------------------------|----------|------|--------------|
| $V_{CC}$  | supply voltage          |                                   | -0.5     | +4.6 | V            |
| $V_I$     | input voltage           |                                   | [1] -0.5 | +7.0 | V            |
| $V_O$     | output voltage          | output in OFF-state or HIGH-state | [1] -0.5 | +7.0 | V            |
| $I_{IK}$  | input clamping current  | $V_I < 0$ V                       | -        | -50  | mA           |
| $I_{OK}$  | output clamping current | $V_O < 0$ V                       | -        | -50  | mA           |
| $I_O$     | output current          | output in LOW-state               | -        | 128  | mA           |
|           |                         | output in HIGH-state              | -        | -64  | mA           |
| $T_{stg}$ | storage temperature     |                                   | -65      | +150 | $^{\circ}$ C |
| $T_j$     | junction temperature    |                                   | [2] -    | 150  | $^{\circ}$ C |

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

## 8. Recommended operating conditions

**Table 5. Operating conditions**

| Symbol              | Parameter                           | Conditions      | Min | Typ | Max | Unit         |
|---------------------|-------------------------------------|-----------------|-----|-----|-----|--------------|
| $V_{CC}$            | supply voltage                      |                 | 2.7 | -   | 3.6 | V            |
| $V_I$               | input voltage                       |                 | 0   | -   | 5.5 | V            |
| $T_{amb}$           | ambient temperature                 | in free air     | -40 | -   | +85 | $^{\circ}$ C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | outputs enabled | -   | -   | 10  | ns/V         |

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions;  $T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $85\text{ }^{\circ}\text{C}$ ; voltages are referenced to GND (ground = 0 V).

| Symbol          | Parameter                          | Conditions   | Min | Typ[1]    | Max       | Unit          |
|-----------------|------------------------------------|--|-----|-----------|-----------|---------------|
| $V_{IK}$        | input clamping voltage             | $V_{CC} = 2.7\text{ V}$ ; $I_{IK} = -18\text{ mA}$   | -   | -         | -1.2      | V             |
| $V_{IH}$        | HIGH-level input voltage           |  | 2.0 | -         | -         | V             |
| $V_{IL}$        | LOW-level input voltage            |  | -   | -         | 0.8       | V             |
| $V_{OH}$        | HIGH-level output voltage          | $V_{CC} = 3.0\text{ V}$ ; $I_{OH} = -12\text{ mA}$   | 2.0 | -         | -         | V             |
| $V_{OL}$        | LOW-level output voltage           | $V_{CC} = 3.0\text{ V}$ ; $I_{OL} = 12\text{ mA}$  | -   | -         | 0.8       | V             |
| $I_{OH}$        | HIGH-level output current          |  | -   | -         | -12       | mA            |
| $I_{OL}$        | LOW-level output current           |  | -   | -         | 12        | mA            |
| $I_I$           | input leakage current              | all input pins   |     |           |           |               |
|                 |                                    | $V_{CC} = 0\text{ V}$ or $3.6\text{ V}$ ; $V_I = 5.5\text{ V}$   | -   | 0.4       | 10        | $\mu\text{A}$ |
|                 |                                    | control pins   |     |           |           |               |
|                 |                                    | $V_{CC} = 3.6\text{ V}$ ; $V_I = V_{CC}$ or GND  | -   | $\pm 0.1$ | $\pm 1$   | $\mu\text{A}$ |
|                 |                                    | data pins  |     |           |           |               |
|                 |                                    | $V_{CC} = 3.6\text{ V}$ ; $V_I = V_{CC}$ [2]   | -   | 0.1       | 1         | $\mu\text{A}$ |
|                 |                                    | $V_{CC} = 3.6\text{ V}$ ; $V_I = 0\text{ V}$ [2]   | -   | -0.4      | -5        | $\mu\text{A}$ |
| $I_{OFF}$       | power-off leakage current          | $V_{CC} = 0\text{ V}$ ; $V_I$ or $V_O = 0\text{ V}$ to $4.5\text{ V}$  | -   | 0.1       | $\pm 100$ | $\mu\text{A}$ |
| $I_{BHL}$       | bus hold LOW current               | nAn input; $V_{CC} = 3\text{ V}$ ; $V_I = 0.8\text{ V}$  | 75  | 135       | -         | $\mu\text{A}$ |
| $I_{BHH}$       | bus hold HIGH current              | nAn input; $V_{CC} = 3\text{ V}$ ; $V_I = 2.0\text{ V}$  | -75 | -135      | -         | $\mu\text{A}$ |
| $I_{BHLO}$      | bus hold LOW overdrive current     | nAn input; $V_{CC} = 3.6\text{ V}$ ; $V_I = 0\text{ V}$ to $3.6\text{ V}$ [3]  | 500 | -         | -         | $\mu\text{A}$ |
| $I_{BHHO}$      | bus hold HIGH overdrive current    | nAn input; $V_{CC} = 3.6\text{ V}$ ; $V_I = 0\text{ V}$ to $3.6\text{ V}$ [3]  | -   | -         | -500      | $\mu\text{A}$ |
| $I_{CEX}$       | output high leakage current        | output in HIGH-state when $V_O > V_{CC}$ ; $V_O = 5.5\text{ V}$ ; $V_{CC} = 3.0\text{ V}$  | -   | 50        | 125       | $\mu\text{A}$ |
| $I_{O(pu/pd)}$  | power-up/power-down output current | $V_{CC} \leq 1.2\text{ V}$ ; $V_O = 0.5\text{ V}$ to $V_{CC}$ ; $V_I = \text{GND}$ or $V_{CC}$ ; n $\overline{\text{OE}}$ = don't care [4] | -   | 1         | $\pm 100$ | $\mu\text{A}$ |
| $I_{OZ}$        | OFF-state output current           | $V_{CC} = 3.6\text{ V}$ ; $V_I = V_{IL}$ or $V_{IH}$   |     |           |           |               |
|                 |                                    | output HIGH: $V_O = 3.0\text{ V}$  | -   | 0.5       | 5         | $\mu\text{A}$ |
|                 |                                    | output LOW: $V_O = 0.5\text{ V}$   | -   | 0.5       | -5        | $\mu\text{A}$ |
| $I_{CC}$        | supply current                     | $V_{CC} = 3.6\text{ V}$ ; $V_I = \text{GND}$ or $V_{CC}$ ; $I_O = 0\text{ A}$  |     |           |           |               |
|                 |                                    | outputs HIGH   | -   | 0.07      | 0.12      | mA            |
|                 |                                    | outputs LOW  | -   | 4.0       | 6         | mA            |
|                 |                                    | outputs disabled [5]   | -   | 0.07      | 0.12      | mA            |
| $\Delta I_{CC}$ | additional supply current          | per input pin; $V_{CC} = 3\text{ V}$ to $3.6\text{ V}$ ; one input at $V_{CC} - 0.6\text{ V}$ and other inputs at $V_{CC}$ or GND [6]      | -   | 0.1       | 0.2       | mA            |
| $C_I$           | input capacitance                  | n $\overline{\text{OE}}$ ; $V_I = 0\text{ V}$ or $3\text{ V}$  | -   | 3         | -         | pF            |
| $C_O$           | output capacitance                 | Outputs disabled; $V_O = 0\text{ V}$ or $3.0\text{ V}$   | -   | 9         | -         | pF            |

[1] Typical values are measured at 3.3 V and  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

[2] Unused pins at  $V_{CC}$  or GND.

[3] This is the bus hold overdrive current required to force the input to the opposite logic state.

[4] This parameter is valid for any  $V_{CC}$  between 0 V and 1.2 V with a transition time of up to 10 ms.

From  $V_{CC} = 1.2\text{ V}$  to  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  a transition time of 100  $\mu\text{s}$  is permitted. This parameter is valid for  $T_{amb} = 25\text{ }^{\circ}\text{C}$  only.

[5] Measured with outputs pulled to  $V_{CC}$  or GND.

[6] This is the increase in supply current for each input at the specified voltage level other than  $V_{CC}$  or GND.

## 10. Dynamic characteristics

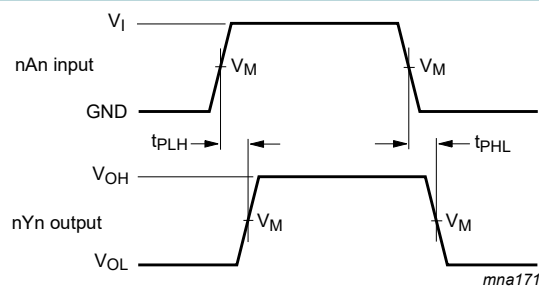
**Table 7. Dynamic characteristics**

At recommended operating conditions;  $T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $85\text{ }^{\circ}\text{C}$ ; voltages are referenced to GND (ground = 0 V); for test circuit see [Fig. 6](#).

| Symbol    | Parameter                           | Conditions  | Min | Typ[1] | Max | Unit |
|-----------|-------------------------------------|---|-----|--------|-----|------|
| $t_{PLH}$ | LOW to HIGH propagation delay       | nAn to nYn; see <a href="#">Fig. 4</a>              |     |        |     |      |
|           |                                     | $V_{CC} = 2.7\text{ V}$                             | -   | -      | 5.0 | ns   |
|           |                                     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$            | 0.5 | 2.8    | 4.2 | ns   |
| $t_{PHL}$ | HIGH to LOW propagation delay       | nAn to nYn; see <a href="#">Fig. 4</a>              |     |        |     |      |
|           |                                     | $V_{CC} = 2.7\text{ V}$                             | -   | -      | 5.0 | ns   |
|           |                                     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$            | 0.5 | 2.5    | 4.2 | ns   |
| $t_{PZH}$ | OFF-state to HIGH propagation delay | $n\overline{OE}$ to nYn; see <a href="#">Fig. 5</a> |     |        |     |      |
|           |                                     | $V_{CC} = 2.7\text{ V}$                             | -   | -      | 7.0 | ns   |
|           |                                     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$            | 1.0 | 3.5    | 5.5 | ns   |
| $t_{PZL}$ | OFF-state to LOW propagation delay  | $n\overline{OE}$ to nYn; see <a href="#">Fig. 5</a> |     |        |     |      |
|           |                                     | $V_{CC} = 2.7\text{ V}$                             | -   | -      | 6.5 | ns   |
|           |                                     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$            | 1.0 | 3.1    | 5.5 | ns   |
| $t_{PHZ}$ | HIGH to OFF-state propagation delay | $n\overline{OE}$ to nYn; see <a href="#">Fig. 5</a> |     |        |     |      |
|           |                                     | $V_{CC} = 2.7\text{ V}$                             | -   | -      | 6.0 | ns   |
|           |                                     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$            | 1.0 | 3.6    | 5.5 | ns   |
| $t_{PLZ}$ | LOW to OFF-state propagation delay  | $n\overline{OE}$ to nYn; see <a href="#">Fig. 5</a> |     |        |     |      |
|           |                                     | $V_{CC} = 2.7\text{ V}$                             | -   | -      | 6.0 | ns   |
|           |                                     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$            | 1.0 | 3.1    | 5.5 | ns   |

[1] Typical values are measured at  $V_{CC} = 3.3\text{ V}$  and  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

### 10.1. Waveforms and test circuit



Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output drop that occur with the output load.

**Fig. 4. Input (nAn) to output (nYn) propagation delay**

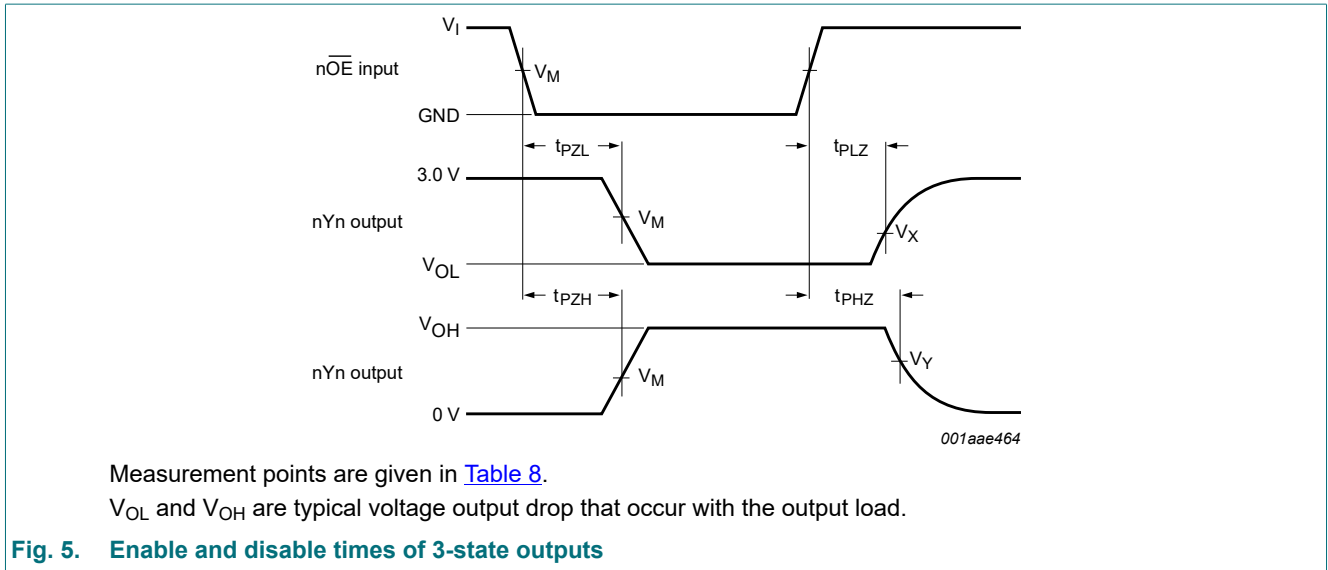


Table 8. Measurement points

| Input |       | Output |                  |                  |
|-------|-------|--------|------------------|------------------|
| $V_1$ | $V_M$ | $V_M$  | $V_X$            | $V_Y$            |
| 2.7 V | 1.5 V | 1.5 V  | $V_{OL} + 0.3 V$ | $V_{OH} - 0.3 V$ |

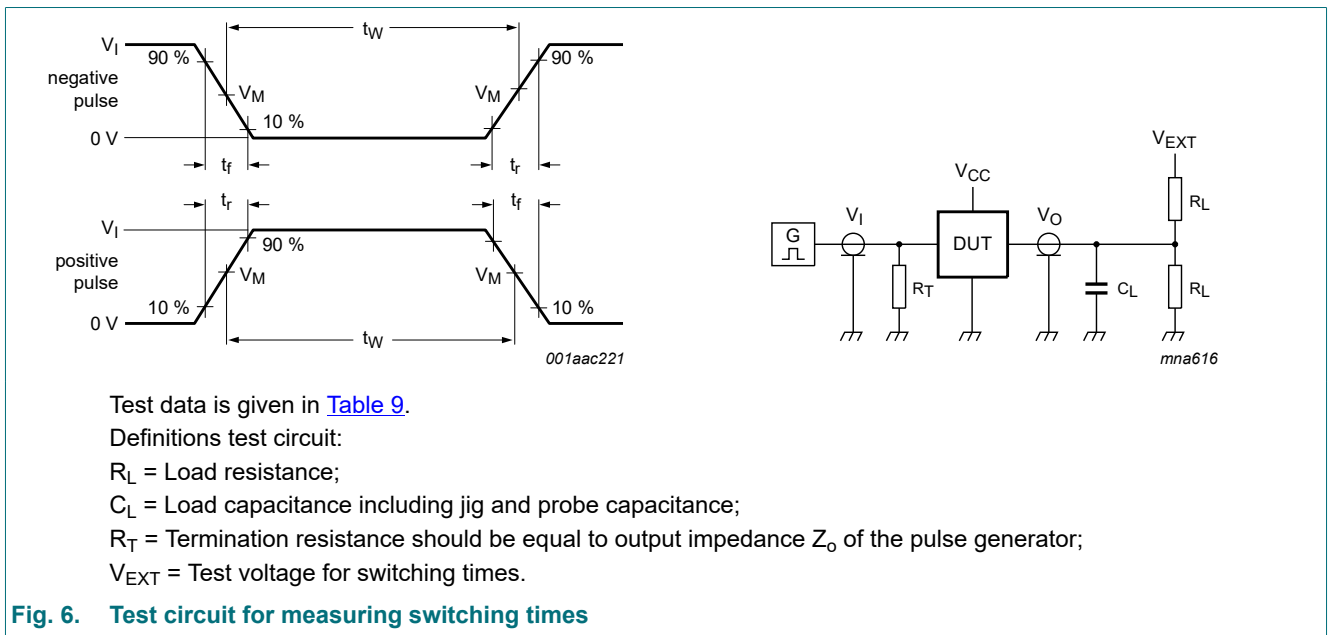


Table 9. Test data

| Input |                       |        |                       | Load  |       | $V_{EXT}$          |                    |                    |
|-------|-----------------------|--------|-----------------------|-------|-------|--------------------|--------------------|--------------------|
| $V_1$ | $f_i$                 | $t_w$  | $t_r, t_f$            | $C_L$ | $R_L$ | $t_{PHZ}, t_{PZH}$ | $t_{PLZ}, t_{PZL}$ | $t_{PLH}, t_{PHL}$ |
| 2.7 V | $\leq 10 \text{ MHz}$ | 500 ns | $\leq 2.5 \text{ ns}$ | 50 pF | 500 Ω | GND                | 6 V                | open               |

11. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1

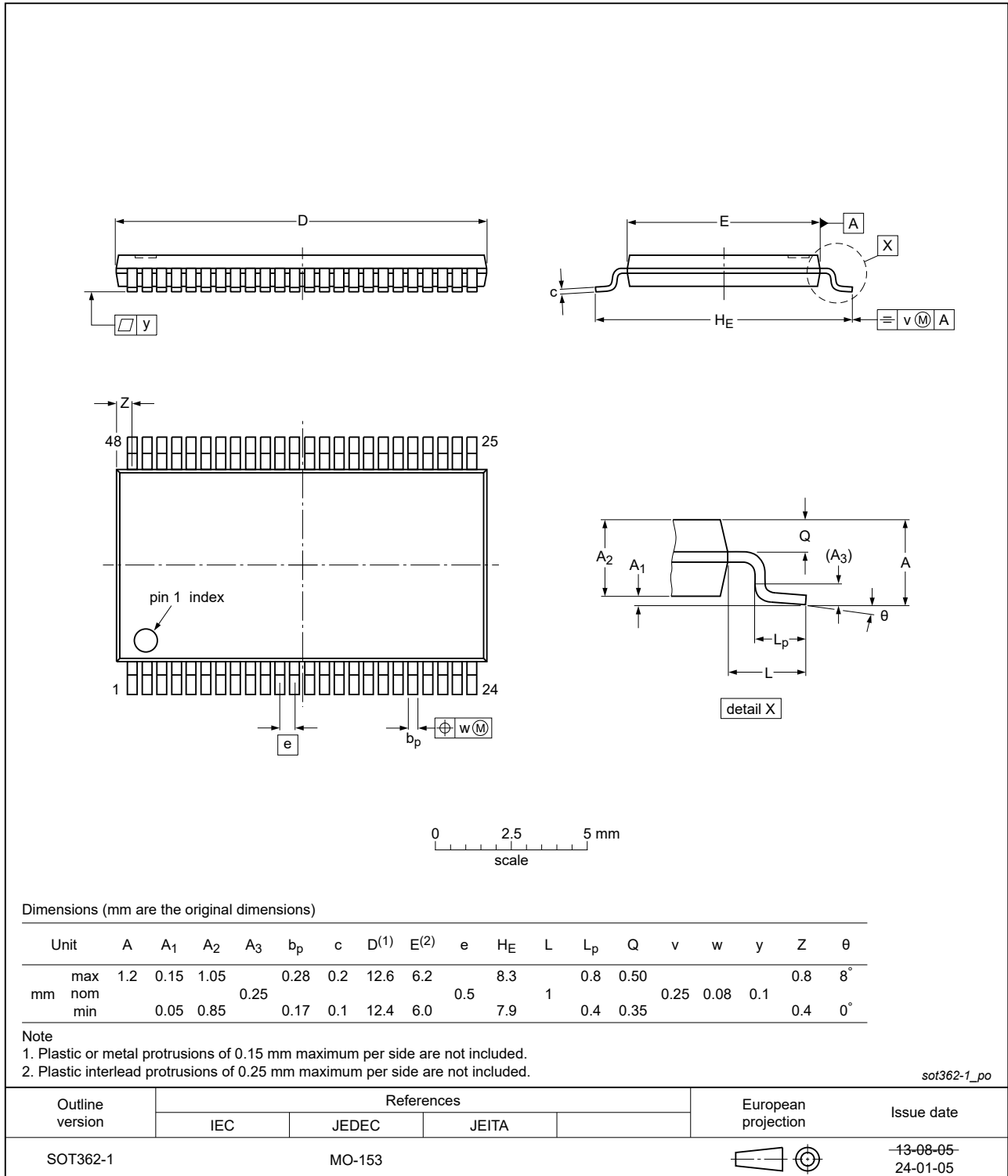


Fig. 7. Package outline SOT362-1 (TSSOP48)

## 12. Abbreviations

Table 10. Abbreviations

| Acronym | Description                                     |
|---------|---|
| ANSI    | American National Standards Institute           |
| BiCMOS  | Bipolar Complementary Metal Oxide Semiconductor |
| CDM     | Charged Device Model                            |
| DUT     | Device Under Test                               |
| ESD     | ElectroStatic Discharge                         |
| ESDA    | ElectroStatic Discharge Association             |
| HBM     | Human Body Model                                |
| JEDEC   | Joint Electron Device Engineering Council       |
| TTL     | Transistor-Transistor Logic                     |

## 13. Revision history

Table 11. Revision history

| Document ID           | Release date | Data sheet status  | Change notice | Supersedes |
|-----------------------|--------------|--------------------|---------------|------------|
| 74LVT162244B_Q100 v.1 | 20251106     | Product data sheet | -             | -          |

## 14. Legal information

### Data sheet status

| Document status [1][2]         | Product status [3] | Definition  |
|--------------------------------|--------------------|---|
| Objective [short] data sheet   | Development        | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification      | This document contains data from the preliminary specification.                       |
| Product [short] data sheet     | Production         | This document contains the product specification.                                     |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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