

74LVT14-Q100

3.3 V hex inverter Schmitt trigger Rev. 1 — 25 January 2024

nexperia

1. General description

The 74LVT14 is a hex inverter with Schmitt-trigger inputs. Bus hold data inputs eliminate the need for external pull-up resistors to define unused inputs. This device is fully specified for partial power down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 3) and is suitable for use in automotive applications.

2. Features and benefits

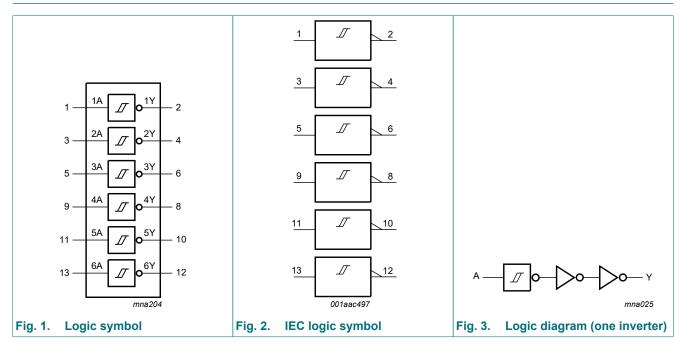
- Automotive product qualification in accordance with AEC-Q100 (Grade 3)
 Specified from -40 °C to +85 °C
- Different positive and negative going input threshold voltages
- Tolerant of slow input transitions
- Wide supply voltage range from 2.7 to 3.6 V
- Overvoltage tolerant inputs to 5.5 V
- BiCMOS high speed and output drive
- Output capability: +32 mA/-20 mA
- High noise immunity
- Direct interface with TTL levels
- No bus current loading when output is tied to 5 V bus
- Power-up 3-state
- IOFF circuitry provides partial Power-down mode operation
- Latch-up protection exceeds 500 mA per JESD78 class II level A
- Complies with JEDEC standard JESD8C (2.7 V to 3.6 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

3. Ordering information

Table 1. Ordering information

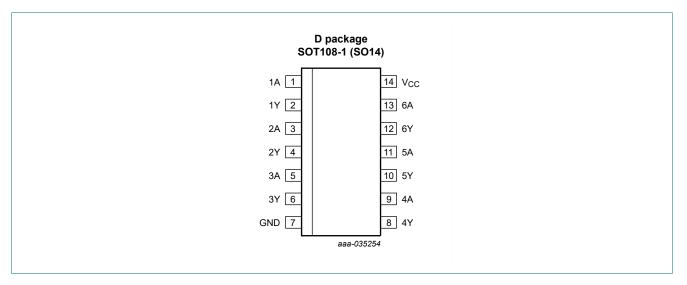
Type number	Package				
	Temperature range	Name	Description	Version	
74LVT14D-Q100	-40 °C to +85 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	<u>SOT108-1</u>	

4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description					
Symbol	Pin	Description			
1A, 2A, 3A, 4A, 5A, 6A	1, 3, 5, 9, 11, 13	data input			
1Y, 2Y, 3Y, 4Y, 5Y, 6Y	2, 4, 6, 8, 10, 12	data output			
GND	7	ground (0 V)			
V _{cc}	14	positive supply voltage			

6. Functional description

Table 3. Function selection

H = HIGH voltage level; L = LOW voltage level.

Inputs	Output
nA	nY
L	Н
Н	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CC}	supply voltage			-0.5	+4.6	V
VI	input voltage		[1]	-0.5	+7.0	V
Vo	output voltage	output in OFF or HIGH state	[1]	-0.5	+7.0	V
l _{IK}	input clamping current	V ₁ < 0 V		-50	-	mA
I _{ОК}	output clamping current	V _O < 0 V		-50	-	mA
lo	output current	output in LOW state		-	64	mA
		output in HIGH state		-32	-	mA
T _{stg}	storage temperature			-65	+150	°C
Tj	junction temperature		[2]	-	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +85 °C		-	500	mW

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

8. Recommended operating conditions

Table 5.	Recommended	operating	conditions
		oporating	00110110110

Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
V _{CC}	supply voltage		2.7	-	3.6	V
VI	input voltage		0	-	5.5	V
I _{OH}	HIGH-level output current		-20	-	-	mA
I _{OL}	LOW-level output current		-	-	32	mA
T _{amb}	ambient temperature	in free air	-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	output enabled	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40	Unit		
			Min	Typ <mark>[1]</mark>	Max	
V _{T+}	positive-going threshold voltage	V _{CC} = 3.3 V; see <u>Fig. 4</u>	1.5	1.7	2.0	V
V _{T-}	negative-going threshold voltage	V _{CC} = 3.3 V; see <u>Fig. 4</u>	0.9	1.1	1.3	V
V _H	hysteresis voltage	V _{CC} = 3.3 V; see <u>Fig. 4</u>	0.4	0.6	-	V
V _{IK}	input clamping voltage	$V_{CC} = 2.7 \text{ V}; \text{ I}_{IK} = -18 \text{ mA}$	-1.2	-	-	V
V _{OH}	HIGH-level output voltage	V_{CC} = 2.7 V to 3.6 V; I _{OH} = -100 µA	V _{CC} - 0.2	-	-	V
		V _{CC} = 2.7 V; I _{OH} = -6 mA	2.4	-	-	V
		V _{CC} = 3.0 V; I _{OH} = -20 mA	2.0	-	-	V
V _{OL} LOW-le	LOW-level output voltage	V _{CC} = 2.7 V; I _{OL} = 100 µA	-	-	0.2	V
		V _{CC} = 2.7 V; I _{OL} = 24 mA	-	-	0.5	V
		V _{CC} = 3.0 V; I _{OL} = 32 mA	-	-	0.5	V
l _l	input leakage current	V _{CC} = 0 V or 3.6 V; V _I = 5.5 V	-	-	10	μA
		V_{CC} = 3.6 V; V_{I} = V_{CC} or GND	-	-	±1	μA
I _{OFF}	power-off leakage current	$V_{CC} = 0 V; V_1 \text{ or } V_0 = 0 V \text{ to } 4.5 V$	-	-	±100	μA
I _{CC}	supply current	$V_{CC} = 3.6 \text{ V}; \text{ V}_{I} = \text{GND or } \text{V}_{CC}; \text{ I}_{O} = 0 \text{ A}$				
		outputs HIGH	-	-	0.02	mA
		outputs LOW	-	1.5	3	mA
ΔI _{CC}	additional supply current	per input pin; V_{CC} = 3.0 V to 3.6 V; [2] one input = V_{CC} - 0.6 V and other inputs at V_{CC} or GND	-	-	0.2	mA
CI	input capacitance	V _I = 0 V or 3.0 V	-	3	-	pF

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

[2] This is the increase in the supply current for each input at the specified voltage level other than V_{CC} or GND.

10. Dynamic characteristics

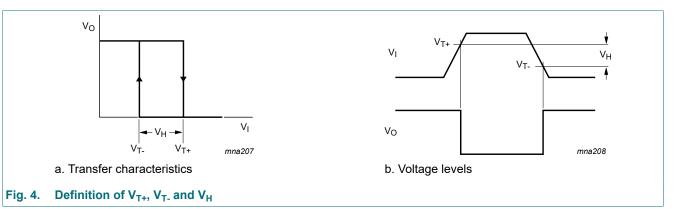
Table 7. Dynamic characteristics

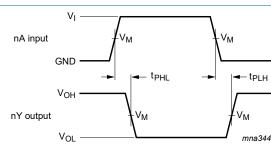
Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 6.

Symbol	Parameter	Conditions	-40	-40 °C to +85 °C			
			Min	Typ [1]	Max		
t _{PLH} LOW to HIGH propagation dela		nA to nY; see <u>Fig. 5</u>					
		V _{CC} = 2.7 V	-	-	6.9	ns	
		V _{CC} = 3.3 V + 0.3 V	1.0	3.8	5.7	ns	
t _{PHL}	HIGH to LOW propagation delay	nA to nY; see Fig. 5					
		V _{CC} = 2.7 V	-	-	4.1	ns	
		V _{CC} = 3.3 V + 0.3 V	1.0	3.2	4.5	ns	

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 3.3 V.

10.1. Waveforms and test circuit





Measurement points are given in Table 8.

 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 5. nA input to nY output propagation delays

Table 8. Measurement points

V _{cc}	Input	Output
	V _M	V _M
2.7 V to 3.6 V	1.5 V	1.5 V

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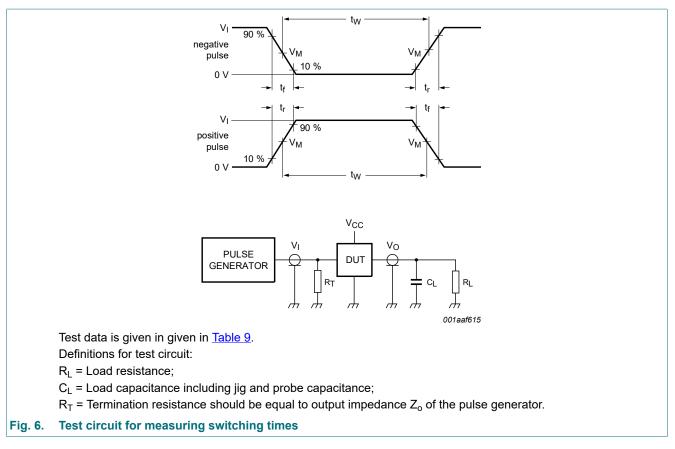


Table 9. Test data

Supply	Input				Load	
V _{cc}	VI	f _i	tw	t _r , t _f	RL	CL
2.7 V to 3.3 V	2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	500 Ω	50 pF

11. Package outline

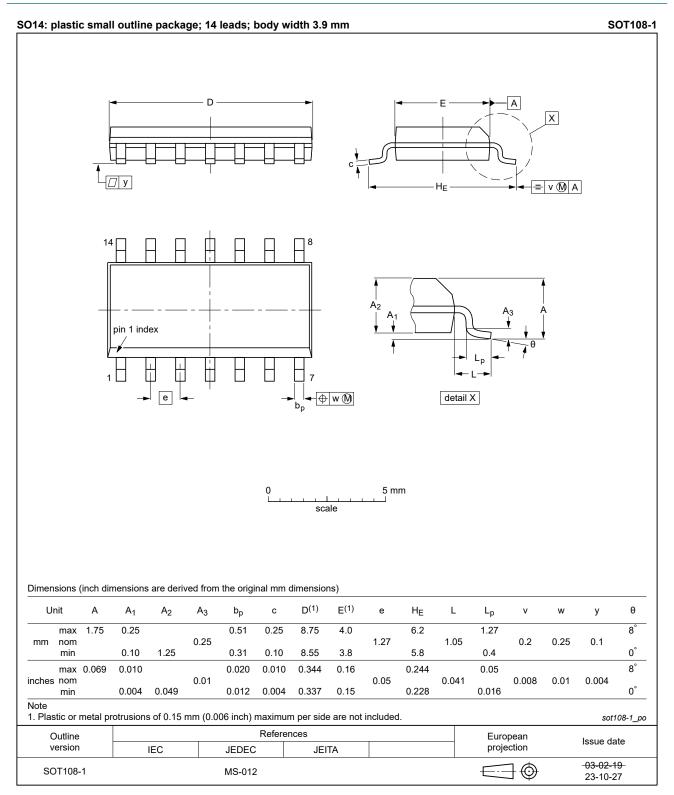


Fig. 7. Package outline SOT108-1 (SO14)

12. Abbreviations

Table 10. Abbreviations				
Acronym	Description			
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor			
CDM	Charged Device Model			
DUT	Device Under Test			
ESD	ElectroStatic Discharge			
НВМ	Human Body Model			
TTL	Transistor-Transistor Logic			

13. Revision history

Table	11	Revision	history
Table		IVEAIPIOLI	matory

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVT14_Q100 v.1	20240125	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

 Please consult the most recently issued document before initiating or completing a design.

- [2] The term 'short data sheet' is explained in section "Definitions".
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