74LVT04

3.3 V Hex inverter

Rev. 5 — 18 April 2024 Product data sheet

1. General description

The 74LVT04 is a hex inverter. This device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 2.7 to 3.6 V
- Overvoltage tolerant inputs to 5.5 V
- BiCMOS high speed and output drive
- Direct interface with TTL levels
- No bus current loading when output is tied to 5 V bus
- Power-up 3-state
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 500 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
  - JESD8C (2.7 V to 3.6 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVT04D	-40 °C to +85 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LVT04PW	-40 °C to +85 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

4. Functional diagram

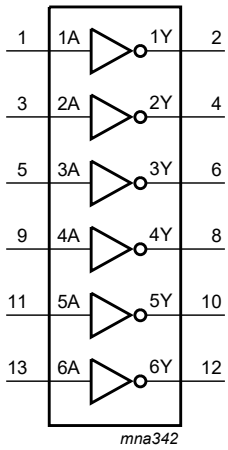

Fig. 1. Logic symbol

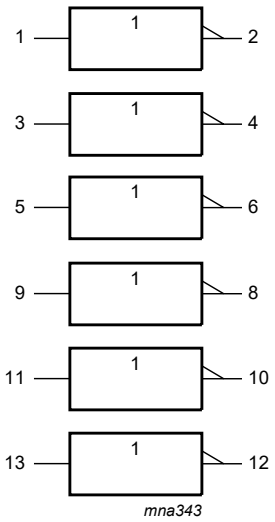

Fig. 2. IEC logic symbol

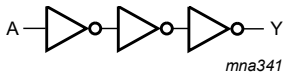

Fig. 3. Logic diagram for one gate

5. Pinning information

5.1. Pinning

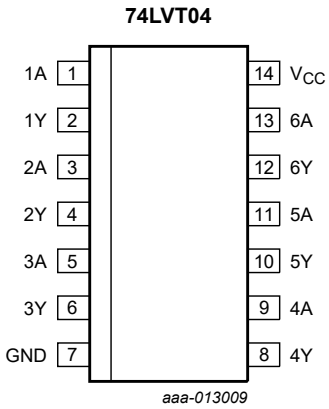

Fig. 4. Pin configuration SOT108-1 (SO14)

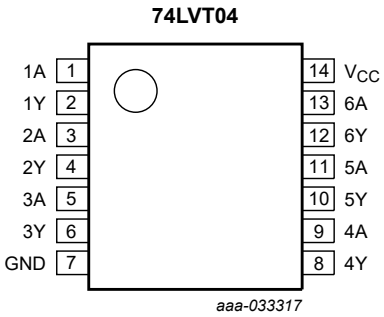

Fig. 5. Pin configuration SOT402-1 (TSSOP14)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
nA	1, 3, 5, 9, 11, 13	data input
nY	2, 4, 6, 8, 10, 12	data output
GND	7	ground (0 V)
V_{CC}	14	supply voltage

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6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

Input	Output
nA	**nY**
L	H
H	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.6	V
V_I	input voltage	[1]	-0.5	+7.0	V
V_O	output voltage	output in OFF-state or HIGH-state [1]	-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
I_{OK}	output clamping current	$V_O < 0$ V	-50	-	mA
I_O	output current	output in LOW-state	-	64	mA
		output in HIGH-state	-	-32	mA
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature	[2]	-	150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +85 °C [3]	-	500	mW

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.
[3] For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		2.7	3.6	V
V_I	input voltage		0	5.5	V
V_{IH}	HIGH-level input voltage		2.0	-	V
V_{IL}	LOW-level input voltage		-	0.8	V
I_{OH}	HIGH-level output current		-	-20	mA
I_{OL}	LOW-level output current		-	32	mA
T_{amb}	ambient temperature	in free air	-40	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	outputs enabled	-	10	ns/V

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9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ [1]	Max	
V_{IK}	input clamp voltage	V_{CC} = 2.7 V; I_{IK} = -18 mA	-	-	-1.2	V
V_{OH}	LOW-level input voltage	V_{CC} = 2.7 V to 3.6 V; I_{OH} = -100 µA	V_{CC} - 0.2	-	-	V
		V_{CC} = 2.7 V; I_{OH} = -6 mA	2.4	-	-	V
		V_{CC} = 3.0 V; I_{OH} = -20 mA	2.0	-	-	V
V_{OL}	LOW-level output voltage	V_{CC} = 2.7 V; I_{OL} = -100 µA	-	-	0.2	V
		V_{CC} = 2.7 V; I_{OL} = 24 mA	-	-	0.5	V
		V_{CC} = 3.0 V; I_{OL} = 32 mA	-	-	0.5	V
I_I	input leakage current	V_{CC} = 0 V or 3.6 V; V_I = 5.5 V	-	-	10	µA
		V_{CC} = 3.6 V; V_I = V_{CC} or GND	-	-	±1	µA
I_{OFF}	output off current	V_{CC} = 0 V; V_I or V_O = 0 V to 4.5 V	-	-	±100	µA
I_{CCH}	quiescent supply current	V_{CC} = 3.6 V; outputs HIGH; V_I = GND or V_{CC}, I_O = 0 V	-	-	0.02	mA
I_{CCL}	quiescent supply current	V_{CC} = 3.6 V; outputs LOW; V_I = GND or V_{CC}; I_O = 0 V	-	1.5	3	mA
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 3 V to 3.6 V; one input at V_{CC} - 0.6 V; other inputs at V_{CC} or GND [2]	-	-	0.2	mA
C_I	input capacitance	V_I = 3 V or 0 V	-	3	-	pF

[1] All typical values are at V_{CC} = 3.3 V and T_{amb} = 25°C.
[2] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; for test circuit, see Fig. 7.

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ [1]	Max	
t_{PLH}	LOW to OFF-state propagation delay	nA to nY; see Fig. 6				
		V_{CC} = 2.7 V	-	-	4.7	ns
		V_{CC} = 3.3 V ± 0.3 V	1.0	2.6	3.9	ns
t_{PHL}	OFF-state to LOW propagation delay	nA to nY; see Fig. 6				ns
		V_{CC} = 2.7 V	-	-	3.2	
		V_{CC} = 3.3 V ± 0.3 V	1.0	2.5	3.5	ns

[1] All typical values are at V_{CC} = 3.3 V and T_{amb} = 25°C.

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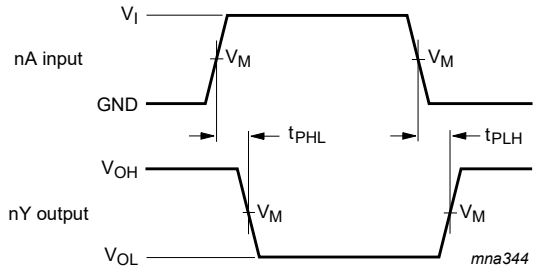
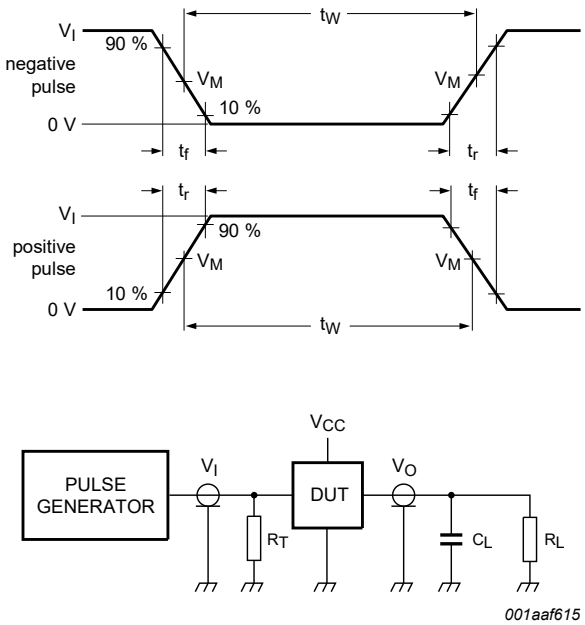
10.1. Waveform and test circuit



V_M = 50%; V_I = GND to V_{CC}.
V_M = 1.5 V; V_I = GND to 2.7 V

Fig. 6. The input nA to output nY propagation delays



Test data is given in Table 8.
Definitions test circuit:
R_T = termination resistance should be equal to output impedance Z_o of the pulse generator.
C_L = load capacitance including jig and probe capacitance.
R_L = Load resistance.

Fig. 7. Test circuit for measuring switching times

Table 8. Test data

Input				Load	
V_I	f_i	t_W	t_r, t_f	C_L	R_L
2.7 V	≤ 10 MHz	500 ns	≤2.5 ns	50 pF	500 Ω

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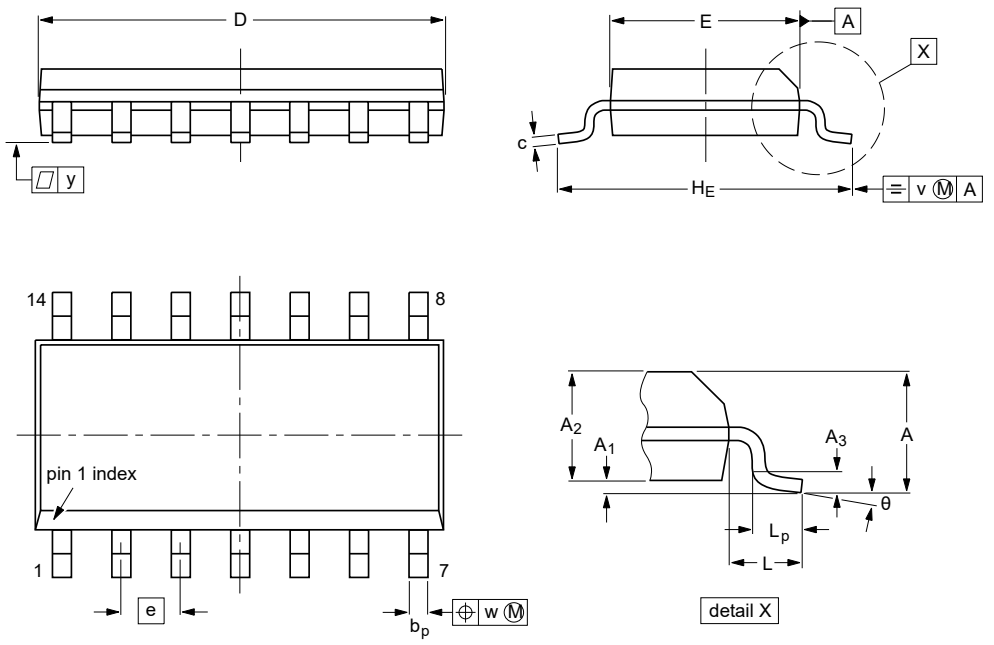
11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



Dimensions (inch dimensions are derived from the original mm dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.75	0.25			0.51	0.25	8.75	4.0		6.2		1.27				8°
	nom				0.25					1.27		1.05		0.2	0.25	0.1	
	min		0.10	1.25		0.31	0.10	8.55	3.8		5.8		0.4				0°
inches	max	0.069	0.010			0.020	0.010	0.344	0.16		0.244		0.05				8°
	nom				0.01					0.05		0.041		0.008	0.01	0.004	
	min		0.004	0.049		0.012	0.004	0.337	0.15		0.228		0.016				0°

Note
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

sot108-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT108-1		MS-012				~~03-02-19~~ 23-10-27

Fig. 8. Package outline SOT108-1 (SO14)

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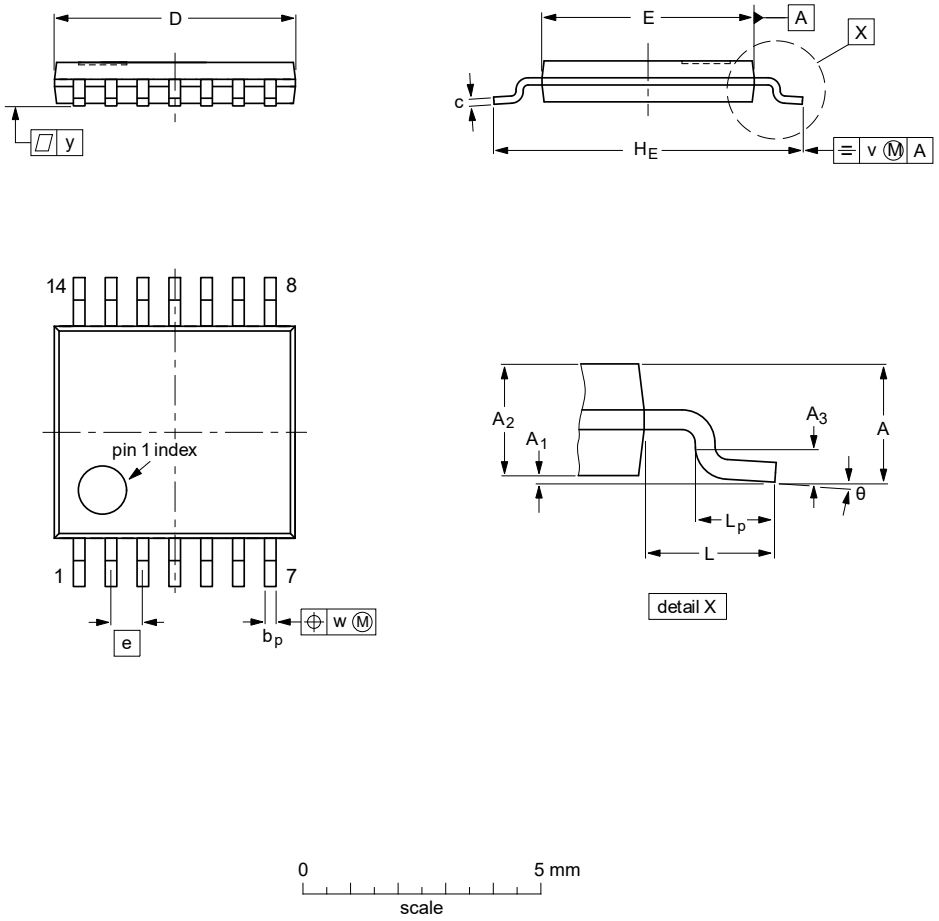
TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.20	0.15	1.05		0.30	0.2	5.1	4.5		6.6		0.75				8°
	nom				0.25					0.65		1		0.2	0.1	0.1	
	min		0.05	0.80		0.19	0.09	4.9	4.3		6.2		0.45				0°

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot402-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~03-02-18~~ 23-10-27

Fig. 9. Package outline SOT402-1 (TSSOP14)

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12. Abbreviations

Table 9. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
CDM	Charged Device Model
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVT04 v.5	20240418	Product data sheet	-	74LVT04 v.4
Modifications:	• Fig. 8, Fig. 9: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153. • Section 2: ESD specification updated according to the latest JEDEC standard.			
74LVT04 v.4	20210812	Product data sheet	-	74LVT04 v.3
Modifications:	• Type number 74LVT04DB (SOT337-1/SSOP14) removed.			
74LVT04 v.3	20210401	Product data sheet	-	74LVT04 v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Section 1 and Section 2 updated. • Section 7: Derating values for P_{tot} total power dissipation updated. • Section 9: Unit of ΔI_{CC} corrected to mA (Errata).			
74LVT04 v.2	20140428	Product data sheet	-	74LVT04_1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Imported the data sheet into the latest template			
74LVT04_1	19960828	Product specification	-	-

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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