1. General description

The 74LVCU04A is a hex unbuffered inverter. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

2. Features and benefits

- Wide supply voltage range from 1.2 V to 3.6 V
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Complies with JEDEC standard:
  - JESD8-7A (1.65 V to 1.95 V)
  - JESD8-5A (2.3 V to 2.7 V)
  - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

<table>
<thead>
<tr>
<th>Type number</th>
<th>Package</th>
<th>Temperature range</th>
<th>Name</th>
<th>Description</th>
<th>Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>74LVCU04AD</td>
<td>SO14</td>
<td>-40 °C to +125 °C</td>
<td>plastic small outline package; 14 leads; body width 3.9 mm</td>
<td>SOT108-1</td>
<td></td>
</tr>
<tr>
<td>74LVCU04APW</td>
<td>TSSOP14</td>
<td>-40 °C to +125 °C</td>
<td>plastic thin shrink small outline package; 14 leads; body width 4.4 mm</td>
<td>SOT402-1</td>
<td></td>
</tr>
<tr>
<td>74LVCU04ABQ</td>
<td>DHVQFN14</td>
<td>-40 °C to +125 °C</td>
<td>plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm</td>
<td>SOT762-1</td>
<td></td>
</tr>
</tbody>
</table>
4. Functional diagram

Fig. 1. Logic symbol

Fig. 2. IEC logic symbol

Fig. 3. Schematic diagram for one inverter
5. Pinning information

5.1. Pinning

D package
SOT108-1 (SO14)

PW package
SOT402-1 (TSSOP14)

BQ package
SOT762-1 (DHVQFN14)

(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

5.2. Pin description

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1A, 2A, 3A, 4A, 5A, 6A</td>
<td>1, 3, 5, 9, 11, 13</td>
<td>data input</td>
</tr>
<tr>
<td>1Y, 2Y, 3Y, 4Y, 5Y, 6Y</td>
<td>2, 4, 6, 8, 10, 12</td>
<td>data output</td>
</tr>
<tr>
<td>GND</td>
<td>7</td>
<td>ground (0 V)</td>
</tr>
<tr>
<td>V_{CC}</td>
<td>14</td>
<td>supply voltage</td>
</tr>
</tbody>
</table>
6. Functional description

Table 3. Function table

<table>
<thead>
<tr>
<th>Input nA</th>
<th>Output nY</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
</tr>
</tbody>
</table>

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>supply voltage</td>
<td></td>
<td>-0.5</td>
<td>+6.5</td>
<td>V</td>
</tr>
<tr>
<td>IK</td>
<td>input clamping current</td>
<td>V&lt;sub&gt;i&lt;/sub&gt; &lt; 0 V</td>
<td>-50</td>
<td>-</td>
<td>mA</td>
</tr>
<tr>
<td>I&lt;sub&gt;f&lt;/sub&gt;</td>
<td>input voltage</td>
<td></td>
<td>[1]</td>
<td>+6.5</td>
<td>V</td>
</tr>
<tr>
<td>I&lt;sub&gt;OK&lt;/sub&gt;</td>
<td>output clamping current</td>
<td>V&lt;sub&gt;O&lt;/sub&gt; &gt; V&lt;sub&gt;CC&lt;/sub&gt; or V&lt;sub&gt;O&lt;/sub&gt; &lt; 0 V</td>
<td>-</td>
<td>±50</td>
<td>mA</td>
</tr>
<tr>
<td>V&lt;sub&gt;O&lt;/sub&gt;</td>
<td>output voltage</td>
<td></td>
<td>[2]</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; + 0.5 V</td>
<td></td>
</tr>
<tr>
<td>IO</td>
<td>output current</td>
<td>V&lt;sub&gt;O&lt;/sub&gt; = 0 V to V&lt;sub&gt;CC&lt;/sub&gt;</td>
<td>-</td>
<td>±50</td>
<td>mA</td>
</tr>
<tr>
<td>ICC</td>
<td>supply current</td>
<td></td>
<td>-</td>
<td>100</td>
<td>mA</td>
</tr>
<tr>
<td>I&lt;sub&gt;GND&lt;/sub&gt;</td>
<td>ground current</td>
<td></td>
<td>-100</td>
<td>-</td>
<td>mA</td>
</tr>
<tr>
<td>T&lt;sub&gt;stab&lt;/sub&gt;</td>
<td>storage temperature</td>
<td>T&lt;sub&gt;amb&lt;/sub&gt; = -40 °C to +125 °C</td>
<td>-65</td>
<td>+150</td>
<td>°C</td>
</tr>
<tr>
<td>P&lt;sub&gt;tot&lt;/sub&gt;</td>
<td>total power dissipation</td>
<td></td>
<td>-</td>
<td>500</td>
<td>mW</td>
</tr>
</tbody>
</table>

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.
[2] The output voltage ratings may be exceeded if the output current ratings are observed.
[3] For SOT402-1 (TSSOP14) package: P<sub>tot</sub> derates linearly with 7.3 mW/K above 81 °C.
For SOT762-1 (DHVQFN14) package: P<sub>tot</sub> derates linearly with 9.6 mW/K above 98 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>supply voltage</td>
<td>functional</td>
<td>1.65</td>
<td>-</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub&gt;f&lt;/sub&gt;</td>
<td>input voltage</td>
<td></td>
<td>0</td>
<td>-</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>IO</td>
<td>output voltage</td>
<td></td>
<td>0</td>
<td>-</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt;</td>
<td>V</td>
</tr>
<tr>
<td>Ta</td>
<td>ambient temperature</td>
<td>in free air</td>
<td>-40</td>
<td>-</td>
<td>+125</td>
<td>°C</td>
</tr>
<tr>
<td>ΔV/ΔV</td>
<td>input transition rise and fall rate</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = 1.65 V to 2.7 V</td>
<td>0</td>
<td>-</td>
<td>20</td>
<td>ns/V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = 2.7 V to 3.6 V</td>
<td>0</td>
<td>-</td>
<td>10</td>
<td>ns/V</td>
</tr>
</tbody>
</table>
# 9. Static characteristics

## Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>(-40 , ^\circ\text{C} \text{ to } +85 , ^\circ\text{C})</th>
<th>(-40 , ^\circ\text{C} \text{ to } +125 , ^\circ\text{C})</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Min</td>
<td>Typ [1]</td>
<td>Max</td>
</tr>
</tbody>
</table>

### HIGH-level input voltage
- \(V_{\text{IH}}\) = 0.5 V; \(I_0 = -100 \, \mu\text{A}\)
- \(V_{\text{CC}} = 1.2 \, \text{V}\)
  - 1.08
  - -
  - 1.12
  - -
  - V
- \(V_{\text{CC}} = 1.65 \text{V to } 1.95 \text{V}\)
  - 1.3
  - -
  - 1.5
  - -
  - V
- \(V_{\text{CC}} = 2.3 \text{V to } 2.7 \text{V}\)
  - 1.8
  - -
  - 2.0
  - -
  - V
- \(V_{\text{CC}} = 3.0 \, \text{V}\)
  - 2.0
  - -
  - 2.4
  - -
  - V
- \(V_{\text{CC}} = 3.6 \, \text{V}\)
  - 2.4
  - -
  - 2.8
  - -
  - V

### LOW-level input voltage
- \(V_{\text{IL}} = V_{\text{OH(min)}} = V_{\text{CC}} - 0.5 \, \text{V}; \)
  - \(I_0 = -100 \, \mu\text{A}\)
- \(V_{\text{CC}} = 1.2 \, \text{V}\)
  - -
  - 0.12
  - -
  - 0.1
  - V
- \(V_{\text{CC}} = 1.65 \text{V to } 1.95 \text{V}\)
  - -
  - 0.6
  - -
  - 0.4
  - V
- \(V_{\text{CC}} = 2.3 \text{V to } 2.7 \text{V}\)
  - -
  - 0.6
  - -
  - 0.5
  - V
- \(V_{\text{CC}} = 3.0 \, \text{V}\)
  - -
  - 1.0
  - -
  - 0.6
  - V
- \(V_{\text{CC}} = 3.6 \, \text{V}\)
  - -
  - 1.2
  - -
  - 0.7
  - V

### HIGH-level output voltage
- \(V_{\text{OH}} = V_{\text{GND}}\)
- \(V_{\text{CC}} = 3.0 \, \text{V}; \ I_0 = -100 \, \mu\text{A}\)
  - 0.2
  - -
  - -
  - 0.3
  - -
  - V
- \(V_{\text{CC}} = 1.65 \text{V}; \ I_0 = -4 \, \text{mA}\)
  - 1.2
  - -
  - 1.05
  - -
  - V
- \(V_{\text{CC}} = 2.3 \text{V}; \ I_0 = -8 \, \text{mA}\)
  - 1.8
  - -
  - 1.65
  - -
  - V
- \(V_{\text{CC}} = 2.7 \text{V}; \ I_0 = -12 \, \text{mA}\)
  - 2.2
  - -
  - 2.05
  - -
  - V
- \(V_{\text{CC}} = 3.0 \, \text{V}; \ I_0 = -18 \, \text{mA}\)
  - 2.4
  - -
  - 2.25
  - -
  - V
- \(V_{\text{CC}} = 3.6 \, \text{V}; \ I_0 = -24 \, \text{mA}\)
  - 2.2
  - -
  - 2.0
  - -
  - V

### LOW-level output voltage
- \(V_{\text{OL}} = V_{\text{CC}}\)
- \(V_{\text{CC}} = 3.0 \, \text{V}; \ I_0 = 100 \, \mu\text{A}\)
  - -
  - 0.20
  - -
  - 0.60
  - V
- \(V_{\text{CC}} = 1.65 \text{V}; \ I_0 = 4 \, \text{mA}\)
  - -
  - 0.45
  - -
  - 0.65
  - V
- \(V_{\text{CC}} = 2.3 \text{V}; \ I_0 = 8 \, \text{mA}\)
  - -
  - 0.60
  - -
  - 0.80
  - V
- \(V_{\text{CC}} = 2.7 \text{V}; \ I_0 = 12 \, \text{mA}\)
  - -
  - 0.40
  - -
  - 0.30
  - V
- \(V_{\text{CC}} = 3.0 \, \text{V}; \ I_0 = 24 \, \text{mA}\)
  - -
  - 0.55
  - -
  - 0.80
  - V

### Input leakage current
- \(I_i\) = \(V_{\text{CC}} = 3.6 \, \text{V}; \ V_i = 5.5 \, \text{V or GND}\)
  - -
  - ±0.1
  - ±5
  - -
  - ±20
  - \(\mu\text{A}\)

### Supply current
- \(I_{\text{CC}}\)
  - \(V_{\text{CC}} = 3.6 \, \text{V}; \ V_i = V_{\text{CC}} \text{ or GND}; \)
  - \(I_0 = 0 \, \text{A}\)
  - -
  - 0.1
  - 10
  - -
  - 40
  - \(\mu\text{A}\)

### Additional supply current
- \(\Delta I_{\text{CC}}\)
  - per input pin:
  - \(V_{\text{CC}} = 2.7 \text{V to } 3.6 \text{V}; \)
  - \(V_i = V_{\text{CC}} - 0.6 \, \text{V}; \ I_0 = 0 \, \text{A}\)
  - -
  - 5
  - 500
  - -
  - 5000
  - \(\mu\text{A}\)

### Input capacitance
- \(C_i\)
  - \(V_{\text{CC}} = 0 \, \text{V to } 3.6 \, \text{V}; \)
  - \(V_i = \text{GND to } V_{\text{CC}}\)
  - -
  - 5.5
  - -
  - -
  - \(\text{pF}\)

---

[1] All typical values are measured at \(V_{\text{CC}} = 3.3 \, \text{V}\) (unless stated otherwise) and \(T_{\text{amb}} = 25 \, ^\circ\text{C}\).
10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 7.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>-40 °C to +85 °C</th>
<th>-40 °C to +125 °C</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Min</td>
<td>Typ [1]</td>
</tr>
<tr>
<td>$t_{pd}$</td>
<td>propagation delay</td>
<td>nA to nY; see Fig. 4 [2]</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{CC} = 1.2$ V</td>
<td>-</td>
<td>6.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{CC} = 1.65$ V to 1.95 V</td>
<td>0.3</td>
<td>3.7</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{CC} = 2.3$ V to 2.7 V</td>
<td>0.5</td>
<td>2.2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{CC} = 2.7$ V</td>
<td>0.5</td>
<td>2.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{CC} = 3.0$ V to 3.6 V</td>
<td>0.5</td>
<td>2.0</td>
</tr>
<tr>
<td>$t_{sk(o)}$</td>
<td>output skew time</td>
<td>$V_{CC} = 3.0$ V to 3.6 V [3]</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>$C_{PD}$</td>
<td>power dissipation capacitance</td>
<td>per inverter; $V_{i} = GND$ to $V_{CC}$ [4]</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{CC} = 1.65$ V to 1.95 V</td>
<td>-</td>
<td>2.3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{CC} = 2.3$ V to 2.7 V</td>
<td>-</td>
<td>5.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{CC} = 3.0$ V to 3.6 V</td>
<td>-</td>
<td>8.4</td>
</tr>
</tbody>
</table>

[1] Typical values are measured at $T_{amb} = 25$ °C and $V_{CC} = 1.2$ V, 1.8 V, 2.5 V, 2.7 V, and 3.3 V respectively.
[2] $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$.
[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
[4] $C_{PD}$ is used to determine the dynamic power dissipation ($P_{D}$ in $\mu$W).

$$P_{D} = C_{PD} \times V_{CC}^2 \times f_{i} \times N + \sum(C_{L} \times V_{CC}^2 \times f_{o})$$

where:

- $f_{i}$ = input frequency in MHz
- $f_{o}$ = output frequency in MHz
- $C_{L}$ = output load capacitance in pF
- $V_{CC}$ = supply voltage in Volts
- $N$ = number of inputs switching
- $\sum(C_{L} \times V_{CC}^2 \times f_{o})$ = sum of the outputs

10.1. Waveforms and test circuit

$V_{M} = 1.5$ V at $V_{CC} \geq 2.7$ V;
$V_{M} = 0.5 \times V_{CC}$ at $V_{CC} < 2.7$ V;
$V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

Fig. 4. Input (nA) to output (nY) propagation delays
\[ g_{fs} = \frac{dI_O}{dV_I}, \text{ at constant } V_O \]
\[ f_i = 1 \text{ kHz at } V_O \text{ is constant} \]

Fig. 5. Test setup for measuring forward transconductance

\[ T_{amb} = 25 \, ^\circ\text{C} \]

Fig. 6. Typical forward transconductance as a function of supply voltage

Test data is given in Table 8. Definitions for test circuit:
\[ R_L = \text{Load resistance}. \]
\[ C_L = \text{Load capacitance including jig and probe capacitance}. \]
\[ R_T = \text{Termination resistance should be equal to output impedance } Z_o \text{ of the pulse generator}. \]

Fig. 7. Test circuit for measuring switching times

<table>
<thead>
<tr>
<th>Supply voltage</th>
<th>Input</th>
<th>( t_r, t_f )</th>
<th>Load</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{CC} )</td>
<td>( V_I )</td>
<td>( \leq 2 \text{ ns} )</td>
<td>( 30 \text{ pF} )</td>
</tr>
<tr>
<td>( 1.2 \text{ V} )</td>
<td>( V_{CC} )</td>
<td>( \leq 2 \text{ ns} )</td>
<td>( 30 \text{ pF} )</td>
</tr>
<tr>
<td>( 1.65 \text{ V to 1.95 V} )</td>
<td>( V_{CC} )</td>
<td>( \leq 2 \text{ ns} )</td>
<td>( 30 \text{ pF} )</td>
</tr>
<tr>
<td>( 2.3 \text{ V to 2.7 V} )</td>
<td>( V_{CC} )</td>
<td>( \leq 2 \text{ ns} )</td>
<td>( 30 \text{ pF} )</td>
</tr>
<tr>
<td>( 2.7 \text{ V} )</td>
<td>( 2.7 \text{ V} )</td>
<td>( \leq 2.5 \text{ ns} )</td>
<td>( 50 \text{ pF} )</td>
</tr>
<tr>
<td>( 3.0 \text{ V to 3.6 V} )</td>
<td>( 2.7 \text{ V} )</td>
<td>( \leq 2.5 \text{ ns} )</td>
<td>( 50 \text{ pF} )</td>
</tr>
</tbody>
</table>
11. Application information

Some applications for the 74LVCU04A are:

- Linear amplifier: see Fig. 8
- Crystal oscillator designs: see Fig. 9
- Astable multivibrator: see Fig. 10

![Linear Amplifier Diagram]

\[ V_{o(p-p)} = V_{CC} - 1.5 \text{ V centered at } 0.5V_{CC} \]

\[ A_u = - \frac{G_{OL}}{1 + \frac{R1}{R2}(1 + G_{OL})} \]

\( G_{OL} \) = loop gain.

\( A_u \) = voltage amplification.

\( R1 \geq 3 \text{ kΩ}, R2 \leq 1 \text{ MΩ} \)

\( Z_L > 10 \text{ kΩ}; A_{OL} = 20 \text{ (typ.)} \)

Typical unity gain bandwidth product is 5 MHz.

Fig. 8. 74LVCU04A used as linear amplifier

![Crystal Oscillator Diagram]

\( R_S \approx 2R \).

The average \( I_{CC} \) is approximately

\[ f = \frac{1}{f} \approx \frac{1}{2.2RC} \]

\[ R_S = 2R. \]

Fig. 9. 74LVCU04A used as crystal oscillator

![Multivibrator Diagram]

\[ f = \frac{1}{f} \approx \frac{1}{3.5 + 0.05 f \text{ (MHz)} \times C \text{ (pF)} [\text{mA}] \text{ at } V_{CC} = 3.0 \text{ V.}} \]

Fig. 10. 74LVCU04A used as astable multivibrator
Fig. 11. Package outline SOT108-1 (SO14)
TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

<table>
<thead>
<tr>
<th>Unit</th>
<th>A</th>
<th>A₁</th>
<th>A₂</th>
<th>A₃</th>
<th>bₚ</th>
<th>c</th>
<th>D⁽¹⁾</th>
<th>E⁽²⁾</th>
<th>e</th>
<th>Hₑ</th>
<th>L</th>
<th>Lₚ</th>
<th>v</th>
<th>w</th>
<th>y</th>
<th>β</th>
</tr>
</thead>
<tbody>
<tr>
<td>mm</td>
<td>max</td>
<td>1.20</td>
<td>0.15</td>
<td>1.05</td>
<td>0.30</td>
<td>0.2</td>
<td>5.1</td>
<td>4.5</td>
<td>6.6</td>
<td>0.75</td>
<td>1.0</td>
<td>0.45</td>
<td>0.2</td>
<td>0.1</td>
<td>0.1</td>
<td>8°</td>
</tr>
<tr>
<td>min</td>
<td>0.05</td>
<td>0.80</td>
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Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

Fig. 12. Package outline SOT402-1 (TSSOP14)
DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;
14 terminals; body 2.5 x 3 x 0.85 mm

Dimensions (mm are the original dimensions)

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Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

Fig. 13. Package outline SOT762-1 (DHVQFN14)
13. Abbreviations

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<td>CDM</td>
<td>Charged Device Model</td>
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<tr>
<td>CMOS</td>
<td>Complementary Metal-Oxide Semiconductor</td>
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<tr>
<td>DUT</td>
<td>Device Under Test</td>
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<tr>
<td>ESD</td>
<td>ElectroStatic Discharge</td>
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<tr>
<td>HBM</td>
<td>Human Body Model</td>
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<td>TTL</td>
<td>Transistor-Transistor Logic</td>
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14. Revision history

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## 15. Legal information

### Data sheet status

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[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term "short data sheet" is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com

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