

74LVC1G384-Q100

Bilateral switch

Rev. 4 — 23 August 2023

Product data sheet

1. General description

The 74LVC1G384-Q100 is a single pole, single throw analog switch. It has two input/output terminals (Y and Z) and an enable pin (\bar{E}). When \bar{E} is HIGH, the analog switch is turned off. Control inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

Schmitt-trigger action at control inputs makes the circuit tolerant of slower input rise and fall times.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and -40 °C to +125 °C
- Wide supply voltage range from 1.65 V to 5.5 V
- Very low ON resistance:
 - 7.5 Ω (typical) at $V_{CC} = 2.7$ V
 - 6.5 Ω (typical) at $V_{CC} = 3.3$ V
 - 6 Ω (typical) at $V_{CC} = 5$ V
- 32 mA continuous switch current
- High noise immunity
- CMOS low power dissipation
- TTL interface compatibility at 3.3 V
- Latch-up performance meets requirements of JESD 78 Class I
- Overvoltage tolerant inputs to 5.5 V
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC1G384GW-Q100	-40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1
74LVC1G384GV-Q100	-40 °C to +125 °C	SC-74A	plastic surface-mounted package; 5 leads	SOT753

4. Marking

Table 2. Marking

Type number	Marking code ^[1]
74LVC1G384GW-Q100	YL
74LVC1G384GV-Q100	YL

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

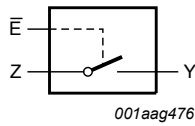


Fig. 1. Logic symbol

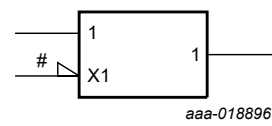


Fig. 2. IEC logic symbol

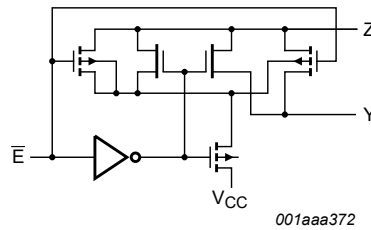
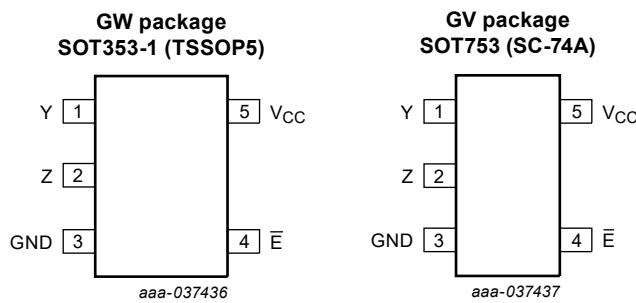


Fig. 3. Logic diagram

6. Pinning information

6.1. Pinning



6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
Y	1	independent input or output
Z	2	independent output or input
GND	3	ground (0 V)
\bar{E}	4	enable input (active LOW)
V_{CC}	5	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level.

Input E	Switch
L	ON-state
H	OFF-state

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
V_I	input voltage	[1]	-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < -0.5 \text{ V}$ or $V_I > V_{CC} + 0.5 \text{ V}$	-50	-	mA
I_{SK}	switch clamping current	$V_I < -0.5 \text{ V}$ or $V_I > V_{CC} + 0.5 \text{ V}$	-	± 50	mA
V_{SW}	switch voltage	enable and disable mode [2]	-0.5	$V_{CC} + 0.5$	V
I_{SW}	switch current	$V_{SW} > -0.5 \text{ V}$ or $V_{SW} < V_{CC} + 0.5 \text{ V}$	-	± 50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40 \text{ °C}$ to $+125 \text{ °C}$ [3]	-	250	mW

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.

[2] The minimum and maximum switch voltage ratings may be exceeded if the switch clamping current rating is observed.

[3] For SOT353-1 (TSSOP5) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.

For SOT753 (SC-74A) package: P_{tot} derates linearly with 3.8 mW/K above 85 °C.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	5.5	V
V_I	input voltage		0	-	5.5	V
V_{SW}	switch voltage	[1]	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65\text{ V to }2.7\text{ V}$	-	-	20	ns/V
		$V_{CC} = 2.7\text{ V to }5.5\text{ V}$	-	-	10	ns/V

- [1] To avoid sinking GND current from terminal Z when switch current flows in terminal Y, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no GND current will flow from terminal Y. In this case, there is no limit for the voltage drop across the switch.

10. Static characteristics

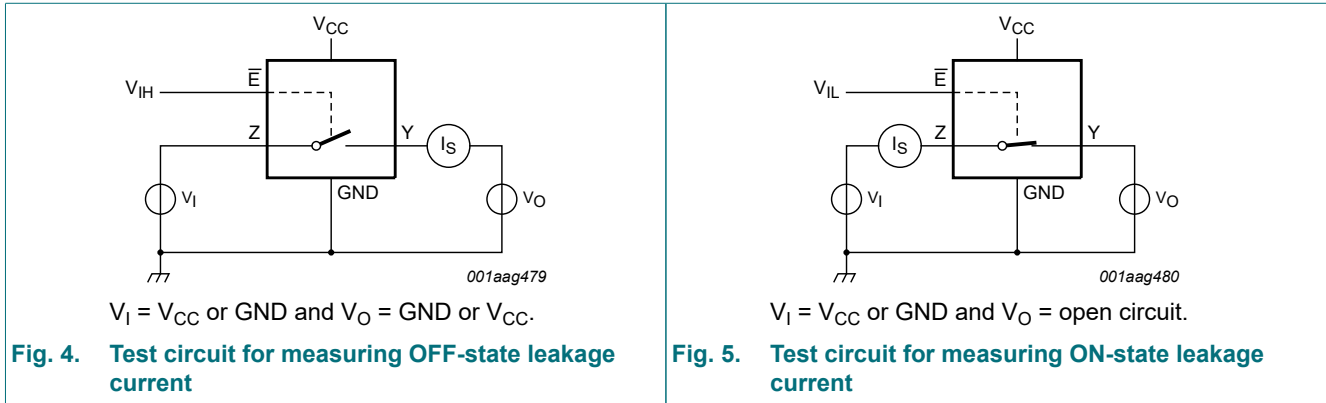
Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.65 \times V_{CC}$	-	-	$0.65 \times V_{CC}$	-	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7	-	-	1.7	-	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2.0	-	-	2.0	-	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$0.7 \times V_{CC}$	-	-	$0.7 \times V_{CC}$	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	-	-	$0.35 \times V_{CC}$	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-	-	0.7	-	0.7	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	-	-	0.8	-	0.8	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	$0.3 \times V_{CC}$	-	$0.3 \times V_{CC}$	V
I_I	input leakage current	pin \bar{E} ; $V_I = 5.5\text{ V or GND}$; $V_{CC} = 0\text{ V to }5.5\text{ V}$ [2]	-	± 0.1	± 1	-	± 1	μA
$I_{S(OFF)}$	OFF-state leakage current	$V_{CC} = 5.5\text{ V}$; see Fig. 4 [2]	-	± 0.1	± 0.2	-	± 0.5	μA
$I_{S(ON)}$	ON-state leakage current	$V_{CC} = 5.5\text{ V}$; see Fig. 5 [2]	-	± 0.1	± 1	-	± 2	μA
I_{CC}	supply current	$V_I = 5.5\text{ V or GND}$; $V_{SW} = \text{GND or }V_{CC}$; $V_{CC} = 1.65\text{ V to }5.5\text{ V}$ [2]	-	0.1	4	-	4	μA
ΔI_{CC}	additional supply current	pin \bar{E} ; $V_I = V_{CC} - 0.6\text{ V}$; $V_{SW} = \text{GND or }V_{CC}$; $V_{CC} = 5.5\text{ V}$ [2]	-	5	500	-	500	μA
C_I	input capacitance		-	2.0	-	-	-	pF
$C_{S(OFF)}$	OFF-state capacitance		-	5.0	-	-	-	pF
$C_{S(ON)}$	ON-state capacitance		-	9.5	-	-	-	pF

- [1] All typical values are measured at $T_{amb} = 25\text{ °C}$.
 [2] These typical values are measured at $V_{CC} = 3.3\text{ V}$.

10.1. Test circuits



10.2. ON resistance

Table 8. ON resistance

At recommended operating conditions; voltages are referenced to GND (ground 0 V); for graphs see Fig. 7 to Fig. 12.

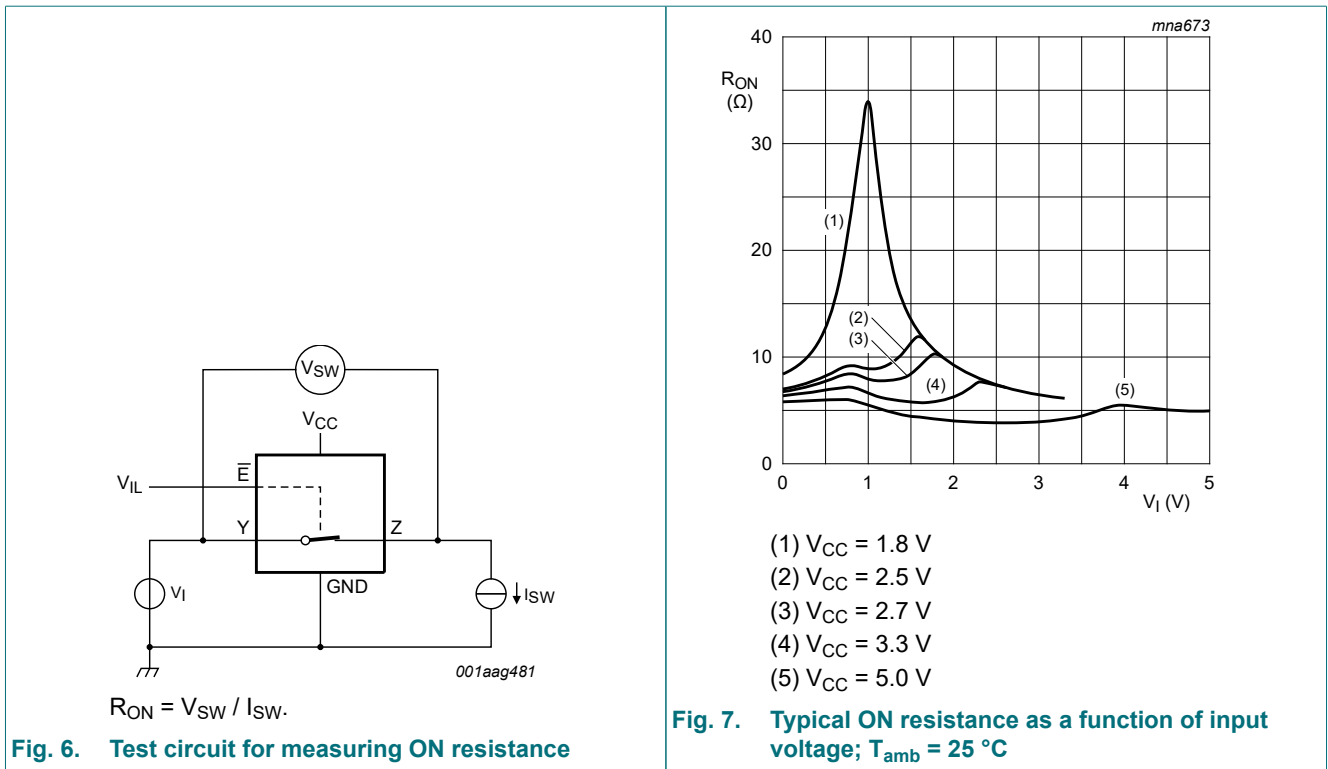
Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
R _{ON(peak)}	ON resistance (peak)	$V_I = GND$ to V_{CC} ; see Fig. 6						
		$I_{SW} = 4 \text{ mA}; V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	-	34.0	130	-	195	Ω
		$I_{SW} = 8 \text{ mA}; V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	-	12.0	30	-	45	Ω
		$I_{SW} = 12 \text{ mA}; V_{CC} = 2.7 \text{ V}$	-	10.4	25	-	38	Ω
		$I_{SW} = 24 \text{ mA}; V_{CC} = 3 \text{ V to } 3.6 \text{ V}$	-	7.8	20	-	30	Ω
		$I_{SW} = 32 \text{ mA}; V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	6.2	15	-	23	Ω
R _{ON(rail)}	ON resistance (rail)	$V_I = GND$; see Fig. 6						
		$I_{SW} = 4 \text{ mA}; V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	-	8.2	18	-	27	Ω
		$I_{SW} = 8 \text{ mA}; V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	-	7.1	16	-	24	Ω
		$I_{SW} = 12 \text{ mA}; V_{CC} = 2.7 \text{ V}$	-	6.9	14	-	21	Ω
		$I_{SW} = 24 \text{ mA}; V_{CC} = 3 \text{ V to } 3.6 \text{ V}$	-	6.5	12	-	18	Ω
		$I_{SW} = 32 \text{ mA}; V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	5.8	10	-	15	Ω
		$V_I = V_{CC}$; see Fig. 6				-		
		$I_{SW} = 4 \text{ mA}; V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	-	10.4	30	-	45	Ω
		$I_{SW} = 8 \text{ mA}; V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	-	7.6	20	-	30	Ω
		$I_{SW} = 12 \text{ mA}; V_{CC} = 2.7 \text{ V}$	-	7.0	18	-	27	Ω
		$I_{SW} = 24 \text{ mA}; V_{CC} = 3 \text{ V to } 3.6 \text{ V}$	-	6.1	15	-	23	Ω
		$I_{SW} = 32 \text{ mA}; V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	4.9	10	-	15	Ω

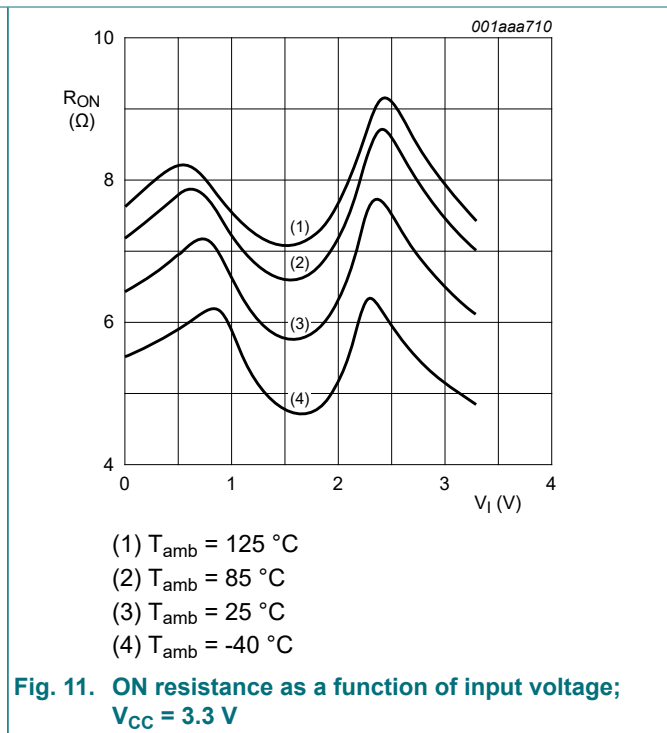
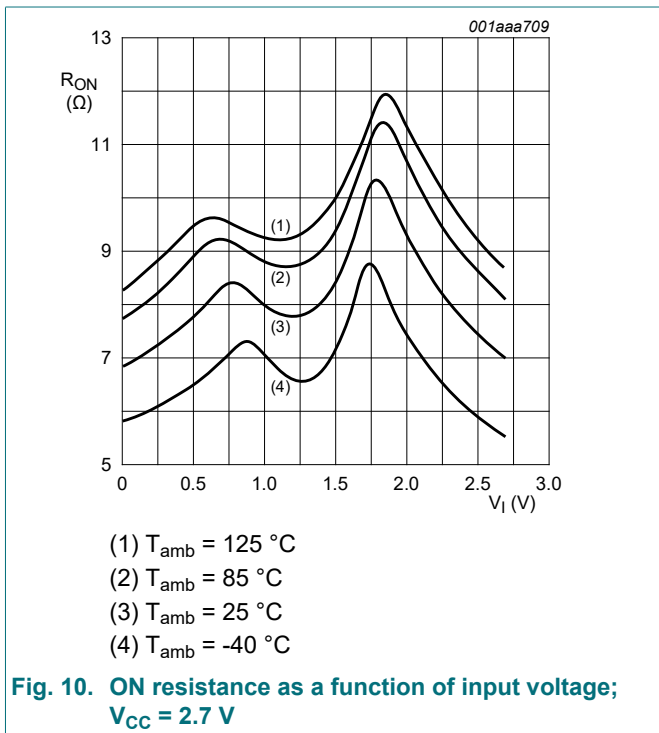
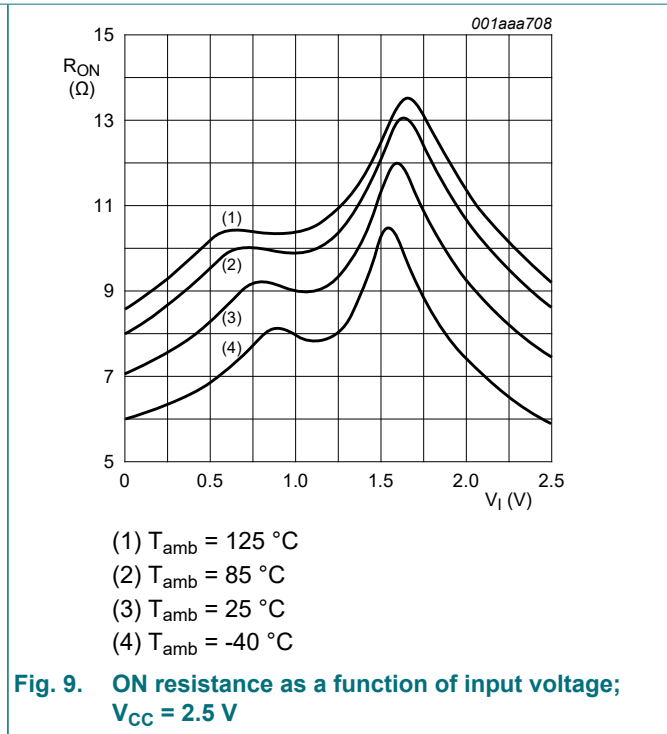
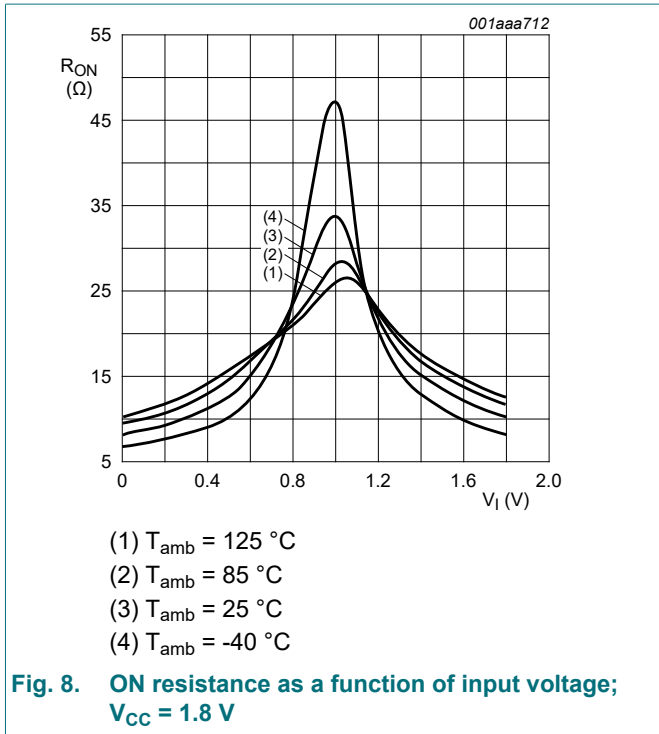
Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
R _{ON(flat)}	ON resistance (flatness)	V _I = GND to V _{CC} [2]						
		I _{SW} = 4 mA; V _{CC} = 1.65 V to 1.95 V	-	26.0	-	-	-	Ω
		I _{SW} = 8 mA; V _{CC} = 2.3 V to 2.7 V	-	5.0	-	-	-	Ω
		I _{SW} = 12 mA; V _{CC} = 2.7 V	-	3.5	-	-	-	Ω
		I _{SW} = 24 mA; V _{CC} = 3 V to 3.6 V	-	2.0	-	-	-	Ω
		I _{SW} = 32 mA; V _{CC} = 4.5 V to 5.5 V	-	1.5	-	-	-	Ω

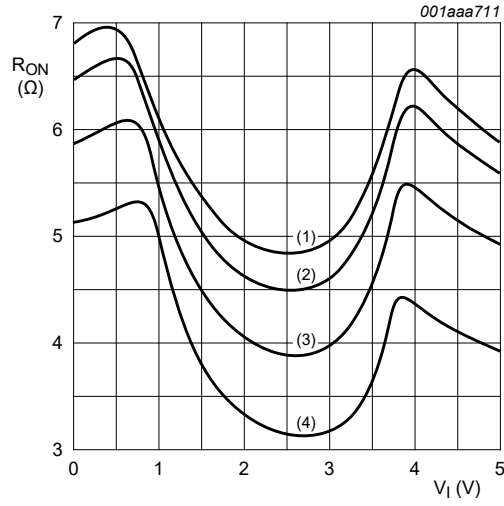
[1] Typical values are measured at T_{amb} = 25 °C and nominal V_{CC}.

[2] Flatness is defined as the difference between the maximum and minimum value of ON resistance measured at identical V_{CC} and temperature.

10.3. ON resistance test circuit and graphs







- (1) $T_{amb} = 125\text{ °C}$
- (2) $T_{amb} = 85\text{ °C}$
- (3) $T_{amb} = 25\text{ °C}$
- (4) $T_{amb} = -40\text{ °C}$

Fig. 12. ON resistance as a function of input voltage; $V_{CC} = 5.0\text{ V}$

11. Dynamic characteristics

Table 9. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 15.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t _{pd}	propagation delay	Y to Z or Z to Y; see Fig. 13 [2][3]						
		V _{CC} = 1.65 V to 1.95 V	-	0.8	2.0	-	3.0	ns
		V _{CC} = 2.3 V to 2.7 V	-	0.4	1.2	-	2.0	ns
		V _{CC} = 2.7 V	-	0.4	1.0	-	1.5	ns
		V _{CC} = 3.0 V to 3.6 V	-	0.3	0.8	-	1.5	ns
		V _{CC} = 4.5 V to 5.5 V	-	0.2	0.6	-	1.0	ns
t _{en}	enable time	\bar{E} to Y or Z; see Fig. 14 [4]						
		V _{CC} = 1.65 V to 1.95 V	1.0	10.0	12.0	1.0	15.5	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	5.7	6.5	1.0	8.5	ns
		V _{CC} = 2.7 V	1.0	5.4	6.0	1.0	8.0	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	4.8	5.0	1.0	6.5	ns
		V _{CC} = 4.5 V to 5.5 V	1.0	3.3	4.2	1.0	5.5	ns
t _{dis}	disable time	\bar{E} to Y or Z; see Fig. 14 [5]						
		V _{CC} = 1.65 V to 1.95 V	1.0	7.4	10.0	1.0	13.0	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	4.1	6.9	1.0	9.0	ns
		V _{CC} = 2.7 V	1.0	4.9	7.5	1.0	9.5	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	5.4	6.5	1.0	8.5	ns
		V _{CC} = 4.5 V to 5.5 V	1.0	3.6	5.0	1.0	6.5	ns
C _{PD}	power dissipation capacitance	C _L = 50 pF; f _i = 10 MHz; V _I = GND to V _{CC} [6]						
		V _{CC} = 2.5 V	-	13.7	-	-	-	pF
		V _{CC} = 3.3 V	-	15.2	-	-	-	pF
		V _{CC} = 5.0 V	-	18.3	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and nominal V_{CC}.

[2] Propagation delay is the calculated RC time constant of the typical ON resistance of the switch and the specified capacitance when driven by an ideal voltage source (zero output impedance).

[3] t_{pd} is the same as t_{PLH} and t_{PHL}.

[4] t_{en} is the same as t_{PZH} and t_{PZL}.

[5] t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[6] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma\{(C_L + C_{S(ON)}) \times V_{CC}^2 \times f_o\} \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

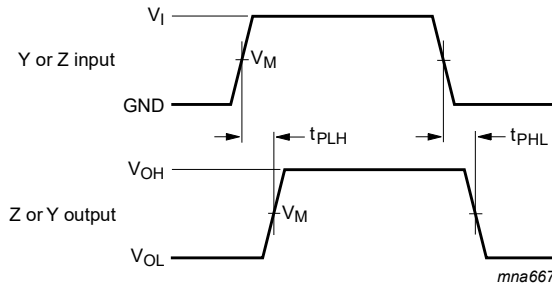
C_{S(ON)} = maximum ON-state switch capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

Σ{(C_L + C_{S(ON)}) × V_{CC}² × f_o} = sum of the outputs.

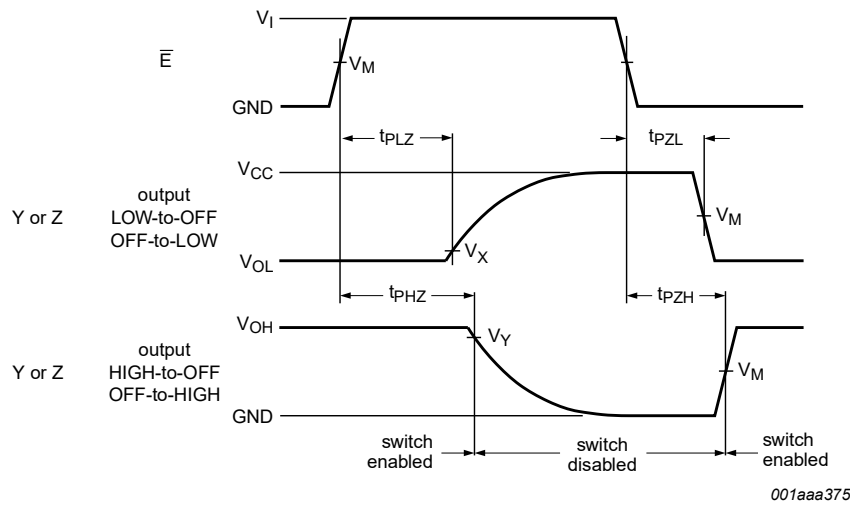
11.1. Waveforms and test circuit



Measurement points are given in [Table 10](#).

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 13. Input (Y or Z) to output (Z or Y) propagation delays



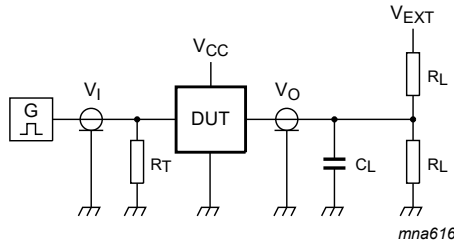
Measurement points are given in [Table 10](#).

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 14. Enable and disable times

Table 10. Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
1.65 V to 1.95 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.3 V to 2.7 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$
3.0 V to 3.6 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$
4.5 V to 5.5 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$



Test data is given in [Table 11](#).

Definitions for test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

C_L = Load capacitance including jig and probe capacitance;

R_L = Load resistance;

V_{EXT} = External voltage for measuring switching times.

Fig. 15. Test circuit for measuring switching times

Table 11. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 k Ω	open	GND	$2 \times V_{CC}$
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	GND	$2 \times V_{CC}$
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6 V
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6 V
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open	GND	$2 \times V_{CC}$

11.2. Additional dynamic characteristics

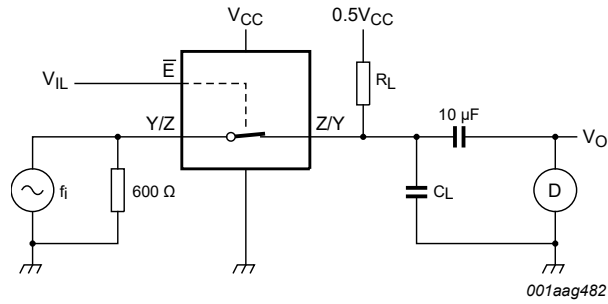
Table 12. Additional dynamic characteristics

At recommended operating conditions; typical values measured at $T_{amb} = 25$ °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
THD	total harmonic distortion	$R_L = 10$ k Ω ; $C_L = 50$ pF; $f_i = 1$ kHz; see Fig. 16					
		$V_{CC} = 1.65$ V	-	0.032	-	%	
		$V_{CC} = 2.3$ V	-	0.008	-	%	
		$V_{CC} = 3.0$ V	-	0.006	-	%	
		$V_{CC} = 4.5$ V	-	0.001	-	%	
		$R_L = 10$ k Ω ; $C_L = 50$ pF; $f_i = 10$ kHz; see Fig. 16					
		$V_{CC} = 1.65$ V	-	0.068	-	%	
		$V_{CC} = 2.3$ V	-	0.009	-	%	
		$V_{CC} = 3.0$ V	-	0.008	-	%	
		$V_{CC} = 4.5$ V	-	0.006	-	%	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{(-3dB)}$	-3 dB frequency response	$R_L = 600 \Omega$; $C_L = 50 \text{ pF}$; see Fig. 17				
		$V_{CC} = 1.65 \text{ V}$	-	135	-	MHz
		$V_{CC} = 2.3 \text{ V}$	-	145	-	MHz
		$V_{CC} = 3.0 \text{ V}$	-	150	-	MHz
		$V_{CC} = 4.5 \text{ V}$	-	155	-	MHz
		$R_L = 50 \Omega$; $C_L = 5 \text{ pF}$; see Fig. 17				
		$V_{CC} = 1.65 \text{ V}$	-	> 500	-	MHz
		$V_{CC} = 2.3 \text{ V}$	-	> 500	-	MHz
		$V_{CC} = 3.0 \text{ V}$	-	> 500	-	MHz
		$V_{CC} = 4.5 \text{ V}$	-	> 500	-	MHz
		$R_L = 50 \Omega$; $C_L = 10 \text{ pF}$; see Fig. 17				
		$V_{CC} = 1.65 \text{ V}$	-	200	-	MHz
		$V_{CC} = 2.3 \text{ V}$	-	350	-	MHz
		$V_{CC} = 3.0 \text{ V}$	-	410	-	MHz
$V_{CC} = 4.5 \text{ V}$	-	440	-	MHz		
α_{iso}	isolation (OFF-state)	$R_L = 600 \Omega$; $C_L = 50 \text{ pF}$; $f_i = 1 \text{ MHz}$; see Fig. 18				
		$V_{CC} = 1.65 \text{ V}$	-	-46	-	dB
		$V_{CC} = 2.3 \text{ V}$	-	-46	-	dB
		$V_{CC} = 3.0 \text{ V}$	-	-46	-	dB
		$V_{CC} = 4.5 \text{ V}$	-	-46	-	dB
		$R_L = 50 \Omega$; $C_L = 5 \text{ pF}$; $f_i = 1 \text{ MHz}$; see Fig. 18				
		$V_{CC} = 1.65 \text{ V}$	-	-37	-	dB
		$V_{CC} = 2.3 \text{ V}$	-	-37	-	dB
		$V_{CC} = 3.0 \text{ V}$	-	-37	-	dB
		$V_{CC} = 4.5 \text{ V}$	-	-37	-	dB
V_{ct}	crosstalk voltage	between digital input and switch; $R_L = 600 \Omega$; $C_L = 50 \text{ pF}$; $f_i = 1 \text{ MHz}$; $t_r = t_f = 2 \text{ ns}$; see Fig. 19				
		$V_{CC} = 1.65 \text{ V}$	-	69	-	mV
		$V_{CC} = 2.3 \text{ V}$	-	87	-	mV
		$V_{CC} = 3.0 \text{ V}$	-	156	-	mV
		$V_{CC} = 4.5 \text{ V}$	-	302	-	mV
Q_{inj}	charge injection	$C_L = 0.1 \text{ nF}$; $V_{gen} = 0 \text{ V}$; $R_{gen} = 0 \Omega$; $f_i = 1 \text{ MHz}$; $R_L = 1 \text{ M}\Omega$; see Fig. 20				
		$V_{CC} = 1.8 \text{ V}$	-	3.3	-	pC
		$V_{CC} = 2.5 \text{ V}$	-	4.1	-	pC
		$V_{CC} = 3.3 \text{ V}$	-	5.0	-	pC
		$V_{CC} = 4.5 \text{ V}$	-	6.4	-	pC
		$V_{CC} = 5.5 \text{ V}$	-	7.5	-	pC

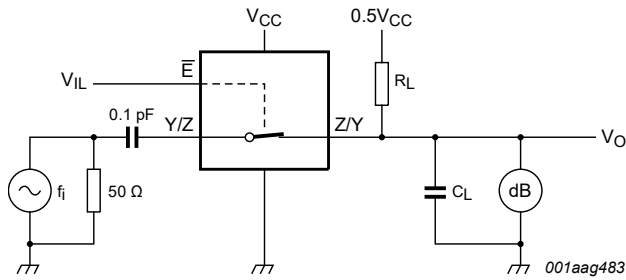
11.3. Test circuits



Test conditions:

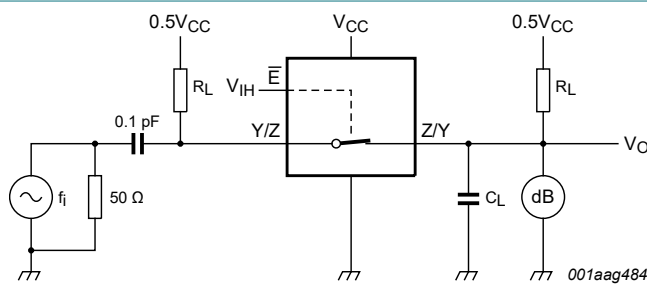
- $V_{CC} = 1.65\text{ V}$: $V_I = 1.4\text{ V (p-p)}$
- $V_{CC} = 2.3\text{ V}$: $V_I = 2\text{ V (p-p)}$
- $V_{CC} = 3\text{ V}$: $V_I = 2.5\text{ V (p-p)}$
- $V_{CC} = 4.5\text{ V}$: $V_I = 4\text{ V (p-p)}$

Fig. 16. Test circuit for measuring total harmonic distortion



Adjust f_i voltage to obtain 0 dBm level at output. Increase f_i frequency until dB meter reads -3 dB.

Fig. 17. Test circuit for measuring the frequency response when switch is in ON-state



Adjust f_i voltage to obtain 0 dBm level at input.

Fig. 18. Test circuit for measuring isolation (OFF-state)

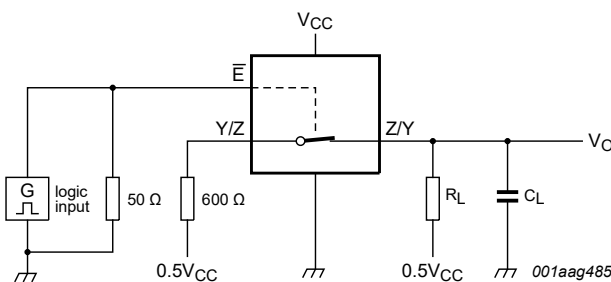
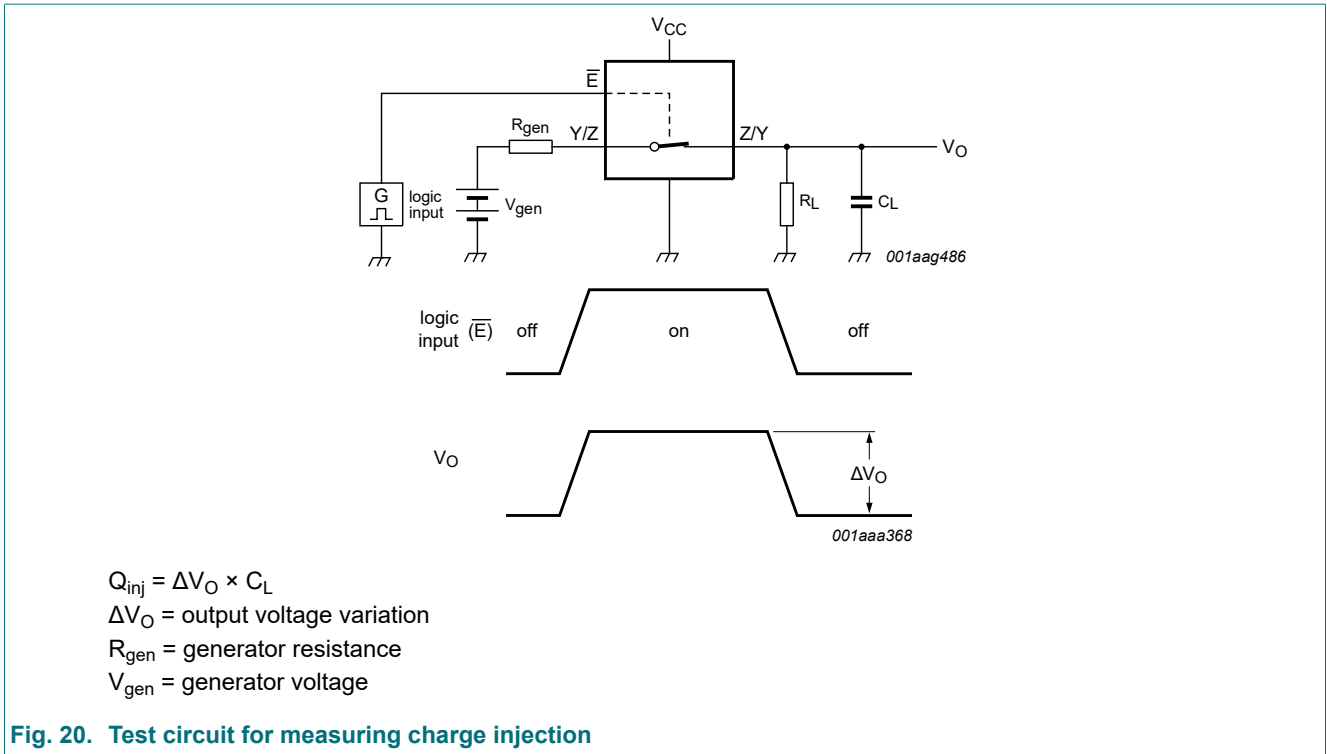


Fig. 19. Test circuit for measuring crosstalk between digital inputs and switch



12. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm

SOT353-1



Fig. 21. Package outline SOT353-1 (TSSOP5)

Plastic surface-mounted package; 5 leads

SOT753

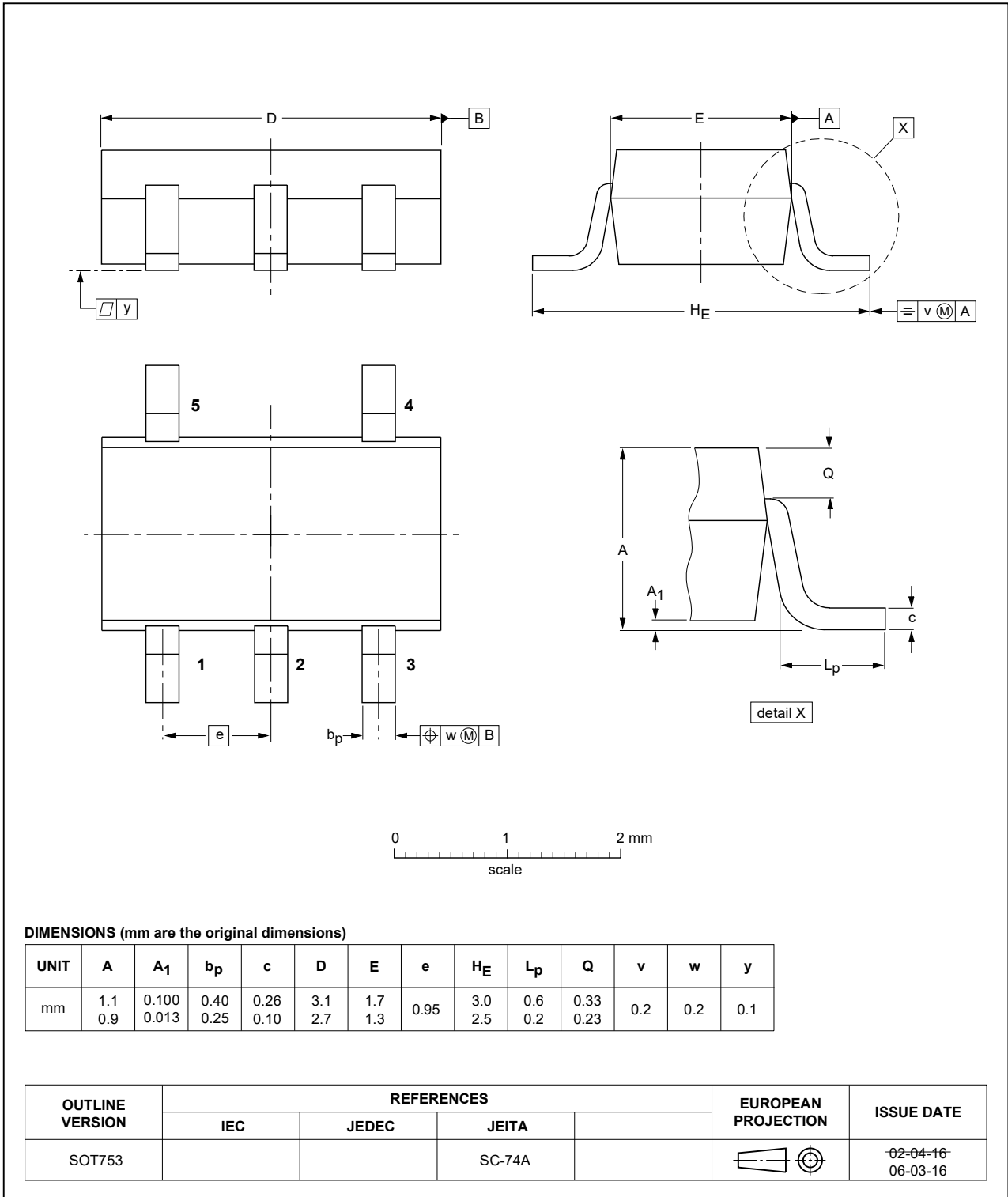


Fig. 22. Package outline SOT753 (SC-74A)

13. Abbreviations

Table 13. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC1G384_Q100 v.4	20230823	Product data sheet	-	74LVC1G384_Q100 v.3
Modifications:	<ul style="list-style-type: none"> • Section 2: ESD specification updated according to the latest JEDEC standard. 			
74LVC1G384_Q100 v.3	20220208	Product data sheet	-	74LVC1G384_Q100 v.2
Modifications:	<ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Section 1 and Section 2 updated. • Table 5: Derating values for P_{tot} total power dissipation updated. • Fig. 21: Package outline drawing SOT353-1 (TSSOP5) has changed. 			
74LVC1G384_Q100 v.2	20161209	Product data sheet	-	74LVC1G384_Q100 v.1
Modifications:	<ul style="list-style-type: none"> • Table 7: The maximum limits for leakage current and supply current have changed. 			
74LVC1G384_Q100 v.1	20130219	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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For sales office addresses, please send an email to: salesaddresses@nexperia.com

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