74LV1T00

2-input single supply translating NAND gate

Rev. 5 — 7 December 2023

Product data sheet

1. General description

The 74LV1T00 is a single, level translating 2-input NAND gate. The low threshold inputs support 1.8 V input logic at V_{CC} = 3.3 V and can be used in 1.8 V to 3.3 V level up translation. In addition, the 5 V tolerant input pins enable level down translation (3.3 V to 2.5 V output at V_{CC} = 2.5 V). The output level is referenced to the supply voltage and supports 1.8 V, 2.5 V, 3.3 V and 5.0 V CMOS levels. The wide V_{CC} range permits the generation of output levels to connect to controllers or processors.

2. Features and benefits

- Single supply voltage translator at 1.8 V, 2.5 V, 3.3 V and 5.0 V
- Up translation
 - 1.2 V to 1.8 V at V_{CC} = 1.8 V
 - 1.5 V to 2.5 V at V_{CC} = 2.5 V
 - 1.8 V to 3.3 V at V_{CC} = 3.3 V
 - 3.3 V to 5.0 V at V_{CC} = 5.0 V
- Down translation
 - 3.3 V to 1.8 V at V_{CC} = 1.8 V
 - 3.3 V to 2.5 V at V_{CC} = 2.5 V
 - 5.0 V to 3.3 V at V_{CC} = 3.3 V
- · 5 V tolerant inputs
- Latch-up performance exceeds 250 mA per JESD 78 Class II
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Applications

- · Portable applications
- PC and notebooks
- Industrial controller
- Telecom



2-input single supply translating NAND gate

4. Ordering information

Table 1. Ordering information

| Type number | Package | Package | | | | | | | |
|-------------|-------------------|---------|--|---------------|--|--|--|--|--|
| | Temperature range | Name | Description | Version | | | | | |
| 74LV1T00GW | -40 °C to +125 °C | TSSOP5 | plastic thin shrink small outline package; 5 leads; body width 1.25 mm | SOT353-1 | | | | | |
| 74LV1T00GV | -40 °C to +125 °C | SC-74A | plastic surface-mounted package; 5 leads | <u>SOT753</u> | | | | | |
| 74LV1T00GX | -40 °C to +125 °C | X2SON5 | plastic thermal enhanced extremely thin small outline package; no leads; 5 terminals; body 0.8 × 0.8 × 0.32 mm | SOT1226-3 | | | | | |

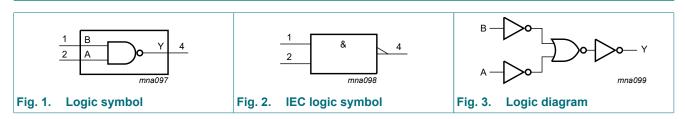
5. Marking

Table 2. Marking

| Type number | Marking code[1] |
|-------------|-----------------|
| 74LV1T00GW | Sa |
| 74LV1T00GV | Sa |
| 74LV1T00GX | Sa |

^[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

6. Functional diagram



2/13

2-input single supply translating NAND gate

7. Pinning information

7.1. Pinning



7.2. Pin description

Table 3. Pin description

| Symbol | Pin | Description |
|-----------------|-----|----------------|
| В | 1 | data input |
| A | 2 | data input |
| GND | 3 | ground (0 V) |
| Υ | 4 | data output |
| V _{CC} | 5 | supply voltage |

8. Functional description

Table 4. Function table

 $H = HIGH \ voltage \ level; \ L = LOW \ voltage \ level.$

| Input | Output | |
|-------|--------|---|
| Α | В | Υ |
| L | L | Н |
| L | Н | Н |
| Н | L | Н |
| Н | Н | L |

2-input single supply translating NAND gate

9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|-------------------------|--|------|-----------------------|------|
| V _{CC} | supply voltage | | -0.5 | +7.0 | V |
| VI | input voltage | [1] | -0.5 | +7.0 | V |
| Vo | output voltage | output HIGH or LOW state [2][3] | -0.5 | V _{CC} + 0.5 | V |
| | | output in power-off state [2] | -0.5 | 4.6 | V |
| I _{IK} | input clamping current | V _I < 0 V | -20 | - | mA |
| I _{OK} | output clamping current | $V_O < 0 \text{ V or } V_O > V_{CC}$ | - | ±20 | mA |
| Io | output current | V _O = 0 V to V _{CC} | - | ±25 | mA |
| I _{CC} | supply current | | - | 50 | mA |
| I _{GND} | ground current | | -50 | - | mA |
| T _{stg} | storage temperature | | -65 | +150 | °C |
| P _{tot} | total power dissipation | $T_{amb} = -40 ^{\circ}\text{C} \text{ to } +125 ^{\circ}\text{C}$ [4] | - | 250 | mW |

^[1] If the input current ratings are observed, the minimum input voltage ratings may be exceeded.

10. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Тур | Max | Unit |
|------------------|-------------------------------------|----------------------------------|-----|-----|-----------------|------|
| V _{CC} | supply voltage | | 1.6 | 5.0 | 5.5 | V |
| VI | input voltage | | 0 | - | 5.5 | V |
| Vo | output voltage | output HIGH or LOW state | 0 | - | V _{CC} | V |
| T _{amb} | ambient temperature | | -40 | +25 | +125 | °C |
| Δt/ΔV | input transition rise and fall rate | V _{CC} = 1.8 V to 5.0 V | - | - | 20 | ns/V |

^[2] If the output current ratings are observed, the output voltage ratings may be exceeded.

^[3] This value is limited to 7 V maximum.

^[4] For SOT353-1 (TSSOP5) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C. For SOT753 (SC-74A) package: P_{tot} derates linearly with 3.8 mW/K above 85 °C. For SOT1226-3 (X2SON5) package: P_{tot} derates linearly with 3.0 mW/K above 67 °C.

2-input single supply translating NAND gate

11. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 25 °C | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|-----------------|--------------------------|--|--------------------------|------|--------------------------|-------|-----------------------|-------|------|
| | | | Min | Max | Min | Max | Min | Max | |
| V _{IH} | HIGH-level | V _{CC} = 1.65 V to 1.8 V | 0.94 | - | 1.0 | - | 1.0 | - | V |
| | input voltage | V _{CC} = 2.0 V | 0.99 | - | 1.03 | - | 1.03 | - | V |
| | | V _{CC} = 2.25 V to 2.5 V | 1.135 | - | 1.18 | - | 1.18 | - | V |
| | | V _{CC} = 2.75 V | 1.21 | - | 1.23 | - | 1.23 | - | V |
| | | V _{CC} = 3.0 V to 3.3 V | 1.35 | - | 1.37 | - | 1.37 | - | V |
| | | V _{CC} = 3.6 V | 1.47 | - | 1.48 | - | 1.48 | - | V |
| | | V _{CC} = 4.5 V to 5.0 V | 2.02 | - | 2.03 | - | 2.03 | - | V |
| | | V _{CC} = 5.5 V | 2.10 | - | 2.11 | - | 2.11 | - | V |
| V _{IL} | LOW-level | V _{CC} = 1.65 V to 2.0 V | - | 0.58 | - | 0.55 | - | 0.55 | V |
| | input voltage | V _{CC} = 2.25 V to 2.75 V | - | 0.75 | - | 0.71 | - | 0.71 | V |
| | | V _{CC} = 3.0 V to 3.6 V | - | 0.80 | - | 0.65 | - | 0.65 | V |
| | | V _{CC} = 4.5 V to 5.5 V | - | 0.80 | - | 0.80 | - | 0.80 | V |
| V _{OH} | HIGH-level | $V_I = V_{IH}$ or V_{IL} ; | | | | | | | |
| | output voltage | V _{CC} = 1.65 V to 5.5 V; I _O = -20 μA | V _{CC} - 0.1 | - | V _{CC} - 0.1 | - | V _{CC} - 0.1 | - | V |
| | | V _{CC} = 1.65 V; I _O = -2 mA | 1.28 | - | 1.21 | - | 1.21 | - | V |
| | | V _{CC} = 1.8 V; I _O = -2 mA | 1.5 | - | 1.45 | - | 1.45 | - | ٧ |
| | | V_{CC} = 2.3 V; I_{O} = -2.3 mA | 2.0 | - | 2.0 | - | 2.0 | - | V |
| | | $V_{CC} = 2.3 \text{ V}; I_{O} = -3 \text{ mA}$ | 2.0 | - | 1.93 | - | 1.93 | - | V |
| | | $V_{CC} = 2.5 \text{ V}; I_{O} = -3 \text{ mA}$ | 2.25 | - | 2.15 | - | 2.15 | - | V |
| | | $V_{CC} = 3.0 \text{ V}; I_{O} = -3 \text{ mA}$ | 2.78 | - | 2.7 | - | 2.7 | - | V |
| | | V _{CC} = 3.0 V; I _O = -5.5 mA | 2.6 | - | 2.49 | - | 2.49 | - | V |
| | | $V_{CC} = 3.3 \text{ V}; I_{O} = -5.5 \text{ mA}$ | 2.9 | - | 2.8 | - | 2.8 | - | V |
| | | V _{CC} = 4.5 V; I _O = -4 mA | 4.2 | - | 4.1 | - | 4.1 | - | V |
| | | $V_{CC} = 4.5 \text{ V}; I_{O} = -8 \text{ mA}$ | 4.1 | - | 3.95 | - | 3.95 | - | V |
| | | V _{CC} = 5.0 V; I _O = -8 mA | 4.6 | - | 4.5 | - | 4.5 | - | V |
| V _{OL} | LOW-level | V _I = V _{IH} or V _{IL} | | | | | | | |
| | output voltage | V _{CC} = 1.65 V to 5.5 V; I _O = 20 μA | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | V _{CC} = 1.65 V; I _O = 2 mA | - | 0.2 | - | 0.25 | - | 0.25 | V |
| | | V _{CC} = 2.3 V; I _O = 2.3 mA | - | 0.1 | - | 0.15 | - | 0.15 | V |
| | | V _{CC} = 2.3 V; I _O = 3 mA | - | 0.15 | - | 0.2 | - | 0.2 | V |
| | | $V_{CC} = 3.0 \text{ V}; I_{O} = 3 \text{ mA}$ | - | 0.1 | - | 0.15 | - | 0.15 | V |
| | | $V_{CC} = 3.0 \text{ V}; I_{O} = 5.5 \text{ mA}$ | - | 0.2 | - | 0.252 | - | 0.252 | V |
| | | V _{CC} = 4.5 V; I _O = 4 mA | - | 0.15 | - | 0.2 | - | 0.2 | V |
| | | V _{CC} = 4.5 V; I _O = 8 mA | - | 0.3 | - | 0.35 | - | 0.35 | V |
| lı | input leakage current | V _I = V _{CC} or GND; V _{CC} = 0 V to 5.5 V | - | ±0.1 | - | ±1 | - | ±1 | μΑ |
| I _{cc} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 1.8 V, 2.5 V, 3.3 V, 5.0 V | - | 1 | - | 10 | - | 10 | μA |

Product data sheet

2-input single supply translating NAND gate

| Symbol | Parameter | Conditions | 25 °C | | -40 °C to | o +85 °C | -40 °C to | Unit | |
|------------------|-----------|---|-------|------|-----------|----------|-----------|------|----|
| | | | Min | Max | Min | Max | Min | Max | |
| Δl _{CC} | | per input pin; V_{CC} = 1.8 V; V_I = 0.3 V or 1.1 V; I_O = 0 A; other pins at V_{CC} or GND | - | 10 | - | 10 | - | 10 | μA |
| | | per input pin; V_{CC} = 5.5 V; V_I = 0.3 V or 3.4 V; I_O = 0 A; other pins at V_{CC} or GND | - | 1.35 | - | 1.5 | - | 1.5 | mA |

12. Dynamic characteristics

Table 8. Dynamic characteristics

GND = 0 V. For test circuit, see Fig. 7.

| Symbol | Parameter | Conditions | 25 °C | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit | |
|-----------------|-----------------------|---|-------|------|------------------|-----|-------------------|-----|------|----|
| | | | Min | Тур | Max | Min | Max | Min | Max | |
| t _{pd} | propagation | A, B to Y; see <u>Fig. 6</u> [1] | | | | | | | | |
| | delay | V _{CC} = 1.8 V; C _L = 15 pF | - | 6.4 | 10.2 | - | 11.5 | - | 12.3 | ns |
| | | V _{CC} = 1.8 V; C _L = 30 pF | - | 7.5 | 12.0 | - | 13.4 | - | 14.4 | ns |
| | | V _{CC} = 2.5 V; C _L = 15 pF | - | 4.5 | 6.9 | - | 7.8 | - | 8.4 | ns |
| | | V _{CC} = 2.5 V; C _L = 30 pF | - | 5.3 | 8.0 | - | 9.1 | - | 9.7 | ns |
| | | V _{CC} = 3.3 V; C _L = 15 pF | - | 3.7 | 5.6 | - | 6.2 | - | 6.6 | ns |
| | | V _{CC} = 3.3 V; C _L = 30 pF | - | 4.3 | 6.4 | - | 7.1 | - | 7.6 | ns |
| | | V _{CC} = 5.0 V; C _L = 15 pF | - | 3.1 | 4.2 | - | 4.6 | - | 4.8 | ns |
| | | V _{CC} = 5.0 V; C _L = 30 pF | - | 3.6 | 4.8 | - | 5.2 | - | 5.5 | ns |
| Cı | input capacitance | $V_I = V_{CC}$ or GND; $V_{CC} = 3.3 \text{ V}$ | - | 1.5 | 10 | - | 10 | - | 10 | pF |
| Co | output capacitance | $V_O = V_{CC}$ or GND; $V_{CC} = 3.3 \text{ V}$ | - | 2.5 | - | - | - | - | - | pF |
| C _{PD} | power dissipation | per buffer; V_I = GND to V_{CC} ; [2] C_L = 30 pF; f = 10 MHz | | | | | | | | |
| | capacitance | V _{CC} = 1.8 V | - | 4.0 | - | - | - | - | - | pF |
| | | V _{CC} = 2.5 V | - | 5.3 | - | - | - | - | - | pF |
| | | V _{CC} = 3.3 V | - | 7.1 | - | - | - | - | - | pF |
| | | V _{CC} = 5.0 V | - | 11.2 | - | - | - | - | - | pF |

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

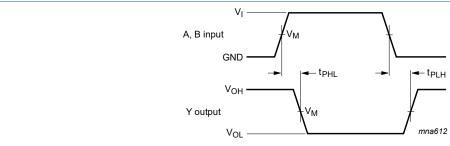
N = number of inputs switching; $\sum (C_L \times V_{CC}^2 \times f_o) = \text{sum of the outputs.}$

6 / 13

 t_{pd} is the same as t_{PLH} and t_{PHL} . C_{PD} is used to determine the dynamic power dissipation (P_D in μ W). $P_D = C_{PD} \times V_{CC}^{\ \ 2} \times f_i \times N + \sum (C_L \times V_{CC}^{\ \ 2} \times f_o)$ where:

2-input single supply translating NAND gate

12.1. Waveforms and test circuit



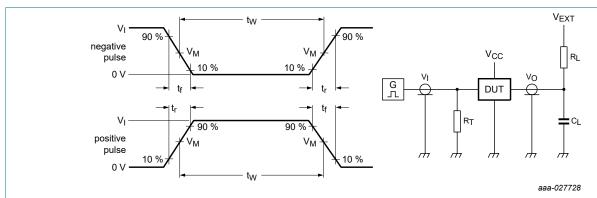
Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 6. The input A, B to output Y propagation delays

Table 9. Measurement points

| Input | Output |
|----------------------|-----------------------|
| V _M | V_{M} |
| 0.5 × V _I | 0.5 × V _{CC} |



Test data is given in Table 10.

Definitions test circuit:

 R_T = Termination resistance should be equal to output impedance Z_0 of the pulse generator;

C_L = Load capacitance including jig and probe capacitance;

R_L = Load resistance;

V_{EXT} = External voltage for measuring switching times.

Fig. 7. Test circuit for measuring switching times

Table 10. Test data

| Supply voltage | Input | | | Load | | V _{EXT} | | |
|-----------------|-----------------|------------|------------------|--------------|----------------|-------------------------------------|-------------------------------------|-------------------------------------|
| V _{CC} | VI | Δt/ΔV [1] | f _{max} | CL | R _L | t _{PLH} , t _{PHL} | t _{PZH} , t _{PHZ} | t _{PZL} , t _{PLZ} |
| 1.8 V | V _{CC} | ≤ 1.0 ns/V | 15 MHz | 15 pF, 30 pF | 1ΜΩ | GND | GND | V _{CC} |
| 2.5 V | V _{CC} | ≤ 1.0 ns/V | 25 MHz | 15 pF, 30 pF | 1ΜΩ | GND | GND | V _{CC} |
| 3.3 V | 3 V | ≤ 1.0 ns/V | 50 MHz | 15 pF, 30 pF | 1ΜΩ | GND | GND | V _{CC} |
| 5.0 V | 3 V | ≤ 1.0 ns/V | 50 MHz | 15 pF, 30 pF | 1ΜΩ | GND | GND | V _{CC} |

[1] $dV/dt \ge 1.0 V/ns$

2-input single supply translating NAND gate

13. Package outline

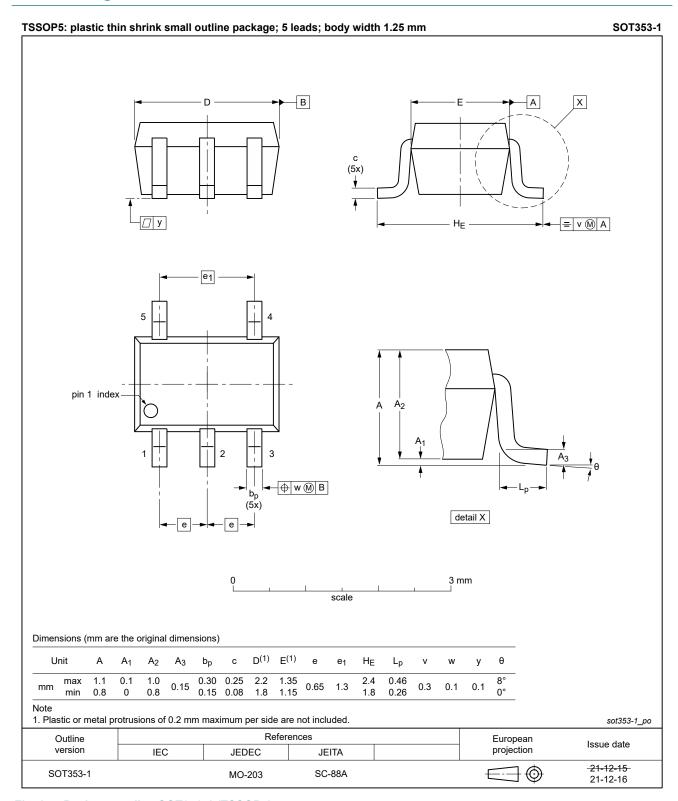


Fig. 8. Package outline SOT353-1 (TSSOP5)

2-input single supply translating NAND gate

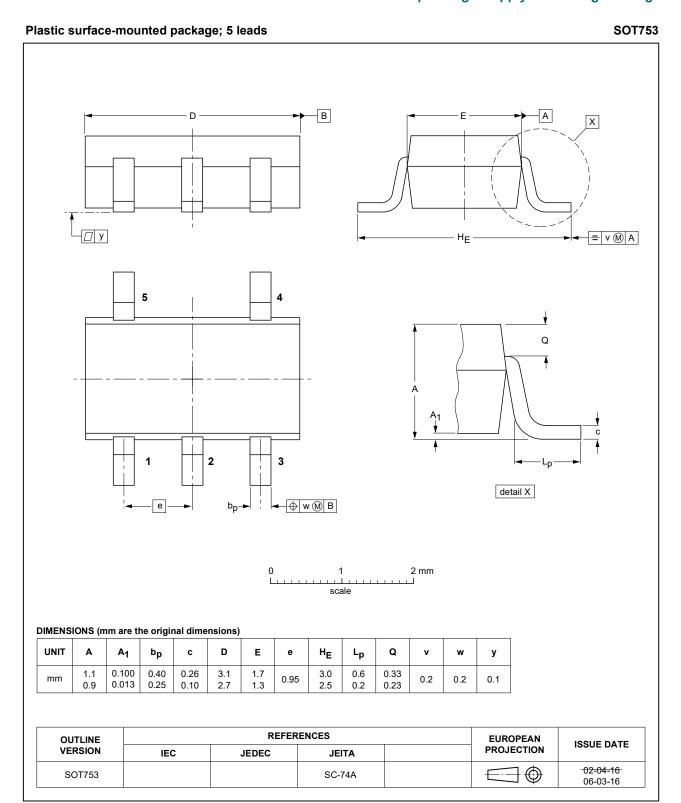


Fig. 9. Package outline SOT753 (SC-74A)

2-input single supply translating NAND gate

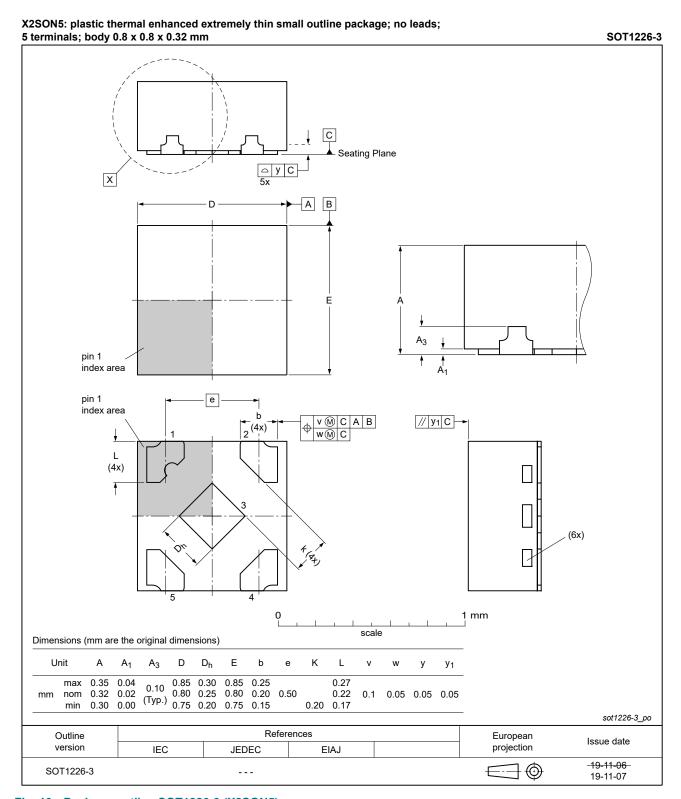


Fig. 10. Package outline SOT1226-3 (X2SON5)

2-input single supply translating NAND gate

14. Abbreviations

Table 11. Abbreviations

| Acronym | Description |
|---------|---|
| CDM | Charge Device Model |
| CMOS | Complementary Metal Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| НВМ | Human Body Model |

15. Revision history

Table 12. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes | | |
|----------------|-----------------------|--|---------------|--------------|--|--|
| 74LV1T00 v.5 | 20231207 | Product data sheet | - | 74LV1T00 v.4 | | |
| Modifications: | <u>Section 2</u> : ES | <u>Section 2</u> : ESD specification updated according to the latest JEDEC standard. | | | | |
| 74LV1T00 v.4 | 20220204 | Product data sheet | - | 74LV1T00 v.3 | | |
| Modifications: | • Fig. 8: Packa | Fig. 8: Package outline drawing for SOT353-1 (TSSOP5) has changed. | | | | |
| 74LV1T00 v.3 | 20210518 | Product data sheet | - | 74LV1T00 v.2 | | |
| Modifications: | • SOT1226 (X2 | SOT1226 (X2SON5) package changed to SOT1226-3 (X2SON5) package. | | | | |
| 74LV1T00 v.2 | 20191203 | Product data sheet | - | 74LV1T00 v.1 | | |
| Modifications: | | Type number 74LV1T00GV (SOT753/SC-74A) added. Table 5: Derating values for P_{tot} total power dissipation updated. | | | | |
| 74LV1T00 v.1 | 20171122 | Product data sheet | - | - | | |

16. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|---------------------------------|-----------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

- Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local Nexperia sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between Nexperia and its customer, unless Nexperia and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the Nexperia product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, Nexperia does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. Nexperia takes no responsibility for the content in this document if provided by an information source outside of Nexperia.

In no event shall Nexperia be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, Nexperia's aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of Nexperia.

Right to make changes — Nexperia reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — Nexperia products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Nexperia product can reasonably be expected to result in personal

2-input single supply translating NAND gate

injury, death or severe property or environmental damage. Nexperia and its suppliers accept no liability for inclusion and/or use of Nexperia products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. Nexperia makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using Nexperia products, and Nexperia accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the Nexperia product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

Nexperia does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using Nexperia products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). Nexperia does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — Nexperia products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nexperia.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Nexperia hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of Nexperia products by sustained.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific Nexperia product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. Nexperia accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without Nexperia's warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond Nexperia's specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies Nexperia for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond Nexperia's standard warranty and Nexperia's product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

74LV1T00

All information provided in this document is subject to legal disclaimers.

© Nexperia B.V. 2023. All rights reserved

2-input single supply translating NAND gate

Contents

| 1. General description | 1 |
|--------------------------------------|----|
| 2. Features and benefits | 1 |
| 3. Applications | 1 |
| 4. Ordering information | 2 |
| 5. Marking | 2 |
| 6. Functional diagram | 2 |
| 7. Pinning information | |
| 7.1. Pinning | |
| 7.2. Pin description | |
| 8. Functional description | |
| 9. Limiting values | |
| 10. Recommended operating conditions | 4 |
| 11. Static characteristics | 5 |
| 12. Dynamic characteristics | 6 |
| 12.1. Waveforms and test circuit | 7 |
| 13. Package outline | 8 |
| 14. Abbreviations | |
| 15. Revision history | 11 |
| 16. Legal information | |
| _ | |

For more information, please visit: http://www.nexperia.com For sales office addresses, please send an email to: salesaddresses@nexperia.com Date of release: 7 December 2023

[©] Nexperia B.V. 2023. All rights reserved