

74LV04AT

Hex inverter

Rev. 2 — 11 January 2024

Product data sheet

1. General description

The 74LV04AT is a hex inverter with TTL inputs.

Designed to operate over a V_{CC} range from 4.5 V to 5.5 V, the inputs are TTL compatible, which allows the device to be used to translate from 3.3 V to 5 V.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial Power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2. Features and benefits

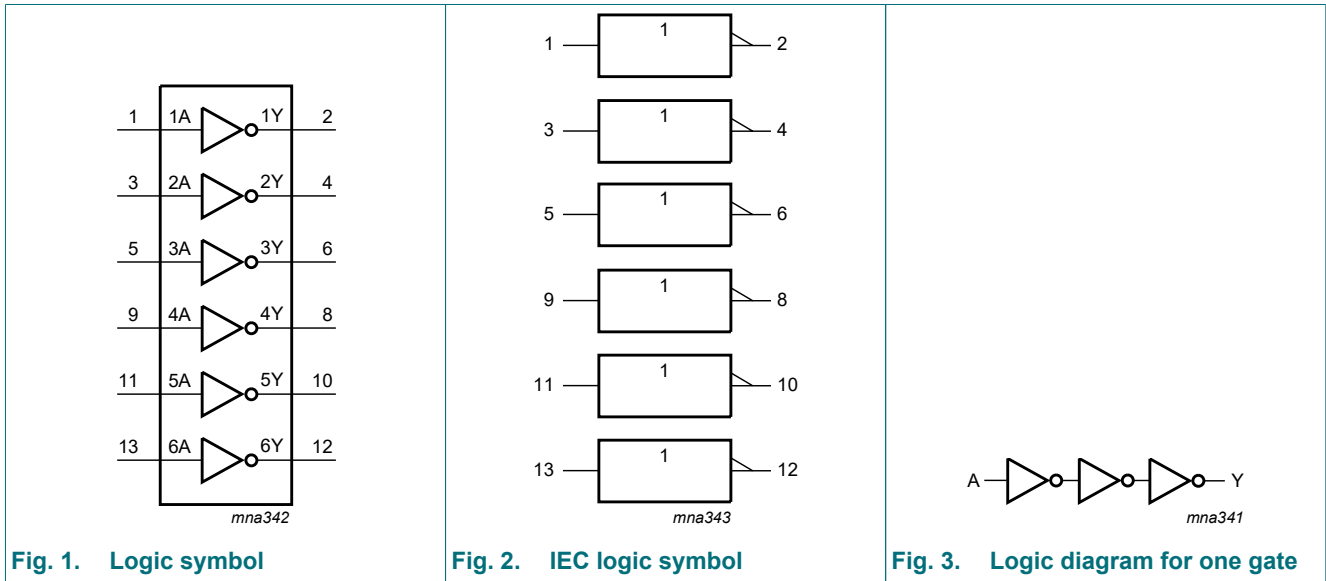
- Direct interface with TTL levels
- Supply voltage range from 4.5 V to 5.5 V
- Typical t_{pd} of 3.3 ns at 5 V
- Typical $V_{OL(p)} < 0.8$ V at $V_{CC} = 5$ V, $T_{amb} = 25$ °C
- Typical $V_{OH(v)} > 2.3$ V at $V_{CC} = 5$ V, $T_{amb} = 25$ °C
- Supports mixed-mode voltage operation on all ports
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 250 mA per JESD 78 Class II
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 3000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 2000 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

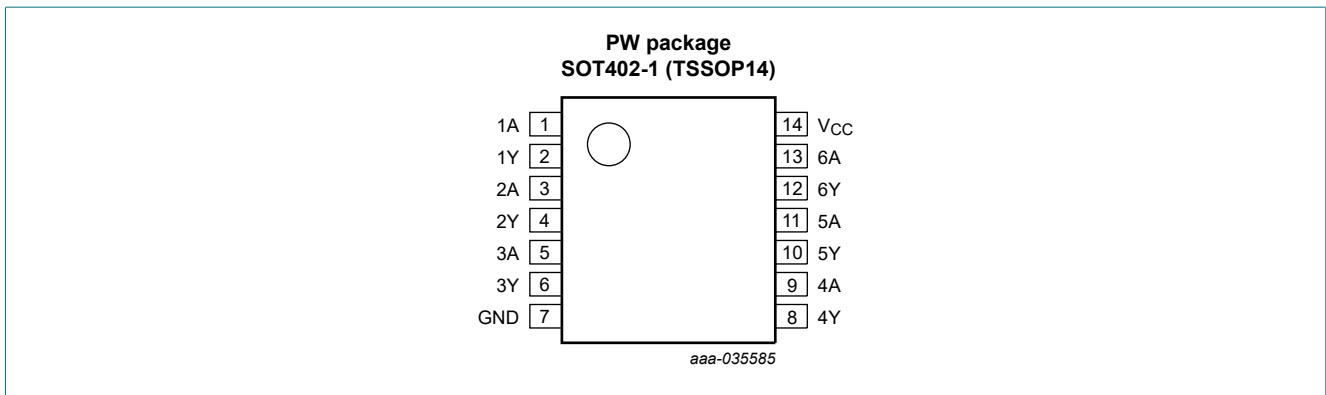
| Type number | Package | | | Version |
|----------------------------|-------------------|---------|--|--------------------------|
| | Temperature range | Name | Description | |
| 74LV04ATPW | -40 °C to +125 °C | TSSOP14 | plastic thin shrink small outline package; 14 leads; body width 4.4 mm | SOT402-1 |

4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|------------------------|--------------------|----------------|
| 1A, 2A, 3A, 4A, 5A, 6A | 1, 3, 5, 9, 11, 13 | data input |
| 1Y, 2Y, 3Y, 4Y, 5Y, 6Y | 2, 4, 6, 8, 10, 12 | data output |
| GND | 7 | ground (0 V) |
| V _{CC} | 14 | supply voltage |

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level

| Input nA | Output nY |
|----------|-----------|
| L | H |
| H | L |

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|-------------------------------|------|----------------|------|
| V_{CC} | supply voltage | | -0.5 | +7.0 | V |
| V_I | input voltage | | -0.5 | +7.0 | V |
| V_O | output voltage | active mode | -0.5 | $V_{CC} + 0.5$ | V |
| | | power-down or 3-state mode | -0.5 | +7.0 | V |
| I_{IK} | input clamping current | $V_I < 0$ V | -20 | - | mA |
| I_{OK} | output clamping current | $V_O < 0$ V | -50 | - | mA |
| I_O | output current | $V_O = 0$ V to V_{CC} | - | ± 35 | mA |
| I_{CC} | supply current | | - | 70 | mA |
| I_{GND} | ground current | | -70 | - | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| P_{tot} | total power dissipation | $T_{amb} = -40$ °C to +125 °C | - | 500 | mW |

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] This value is limited to 7.0 V maximum.

[4] For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---------------------|-------------------------------------|------------------------------|-----|----------|------|
| V_{CC} | supply voltage | | 4.5 | 5.5 | V |
| V_I | input voltage | | 0 | 5.5 | V |
| V_O | output voltage | active mode | 0 | V_{CC} | V |
| | | power-down or 3-state mode | 0 | 5.5 | V |
| T_{amb} | ambient temperature | | -40 | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC} = 5.0$ V \pm 0.5 V | - | 20 | ns/V |

9. Static characteristics

Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|------------------|---------------------------|--|-------|-----|------|------------------|------|-------------------|------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 4.5 V to 5.5 V | 2 | - | - | 2 | - | 2 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 4.5 V to 5.5 V | - | - | 0.8 | - | 0.8 | - | 0.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | | | | | |
| | | I _O = -50 μA | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| | | I _O = -12 mA | 3.8 | - | - | 3.8 | - | 3.8 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | | | | | |
| | | I _O = 50 μA | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 12mA | - | - | 0.55 | - | 0.55 | - | 0.55 | V |
| I _{OFF} | power-off leakage current | V _I or V _O = GND to 5.5 V; V _{CC} = 0 V | - | - | 0.5 | - | 5 | - | 5 | μA |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 0 V to 5.5 V | - | - | ±0.1 | - | ±1 | - | ±1 | μA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V | - | - | 2 | - | 20 | - | 20 | μA |
| ΔI _{CC} | additional supply current | per input pin; V _I = 3.4 V; other pins at V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V | - | - | 1.35 | - | 1.5 | - | 1.5 | mA |

10. Dynamic characteristics

Table 7. Dynamic characteristics

$GND = 0\text{ V}$. For test circuit see Fig. 5.

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|----------|-------------------------------|--|-------|--------|-----|------------------|-----|-------------------|------|------|
| | | | Min | Typ[1] | Max | Min | Max | Min | Max | |
| t_{pd} | propagation delay | nA to nY ; see Fig. 4 [2] | | | | | | | | |
| | | $V_{CC} = 4.5\text{ V}$ to 5.5 V | | | | | | | | |
| | | $C_L = 15\text{ pF}$ | - | 3.3 | 6.3 | 1 | 7.3 | 1 | 8.1 | ns |
| | | $C_L = 50\text{ pF}$ | - | 5.1 | 7.7 | 1 | 8.8 | 1 | 10.4 | ns |
| C_i | input capacitance | $V_i = V_{CC}$ or GND ; $V_{CC} = 5\text{ V}$ | - | 2 | 6 | - | 6 | - | 6 | pF |
| C_o | output capacitance | $V_o = V_{CC}$ or GND ; $V_{CC} = 5\text{ V}$ | - | 5 | - | - | - | - | - | pF |
| C_{PD} | power dissipation capacitance | per buffer; $C_L = 50\text{ pF}$; [3] $f = 10\text{ MHz}$; $V_i = GND$ to V_{CC} | - | 9 | - | - | - | - | - | pF |

[1] Typical values are measured at $T_{amb} = 25\text{ °C}$ and $V_{CC} = 5\text{ V}$.

[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

Table 8. Noise characteristics

$GND = 0\text{ V}$. For test circuit see Fig. 5.

| Symbol | Parameter | Conditions | $T_{amb} = 25\text{ °C}$ | | | Unit |
|--|---------------------------------------|------------|--------------------------|------|-----|------|
| | | | Min | Typ | Max | |
| $V_{CC} = 5\text{ V}$; $C_L = 50\text{ pF}$ | | | | | | |
| $V_{OL(p)}$ | LOW-level output voltage (peak) | | - | 0.2 | 0.8 | V |
| $V_{OL(v)}$ | LOW-level output voltage (valley) | | -0.8 | -0.3 | - | V |
| $V_{OH(v)}$ | HIGH-level output voltage (valley) | | - | 4.5 | - | V |
| $V_{IH(AC)}$ | AC HIGH-level input voltage (dynamic) | | 2 | - | - | V |
| $V_{IL(AC)}$ | AC LOW-level input voltage (dynamic) | | - | - | 0.8 | V |

10.1. Waveforms and test circuit

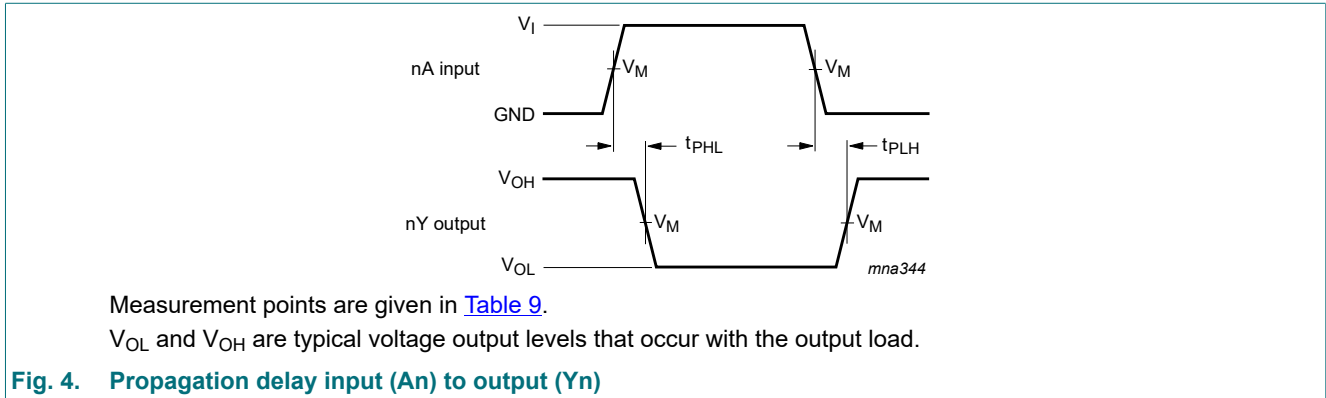


Table 9. Measurement points

| Input | Output | | |
|-------|---------------------|--------------------------|--------------------------|
| V_M | V_M | V_X | V_Y |
| 1.5 V | $0.5 \times V_{CC}$ | $V_{OL} + 0.3 \text{ V}$ | $V_{OH} - 0.3 \text{ V}$ |

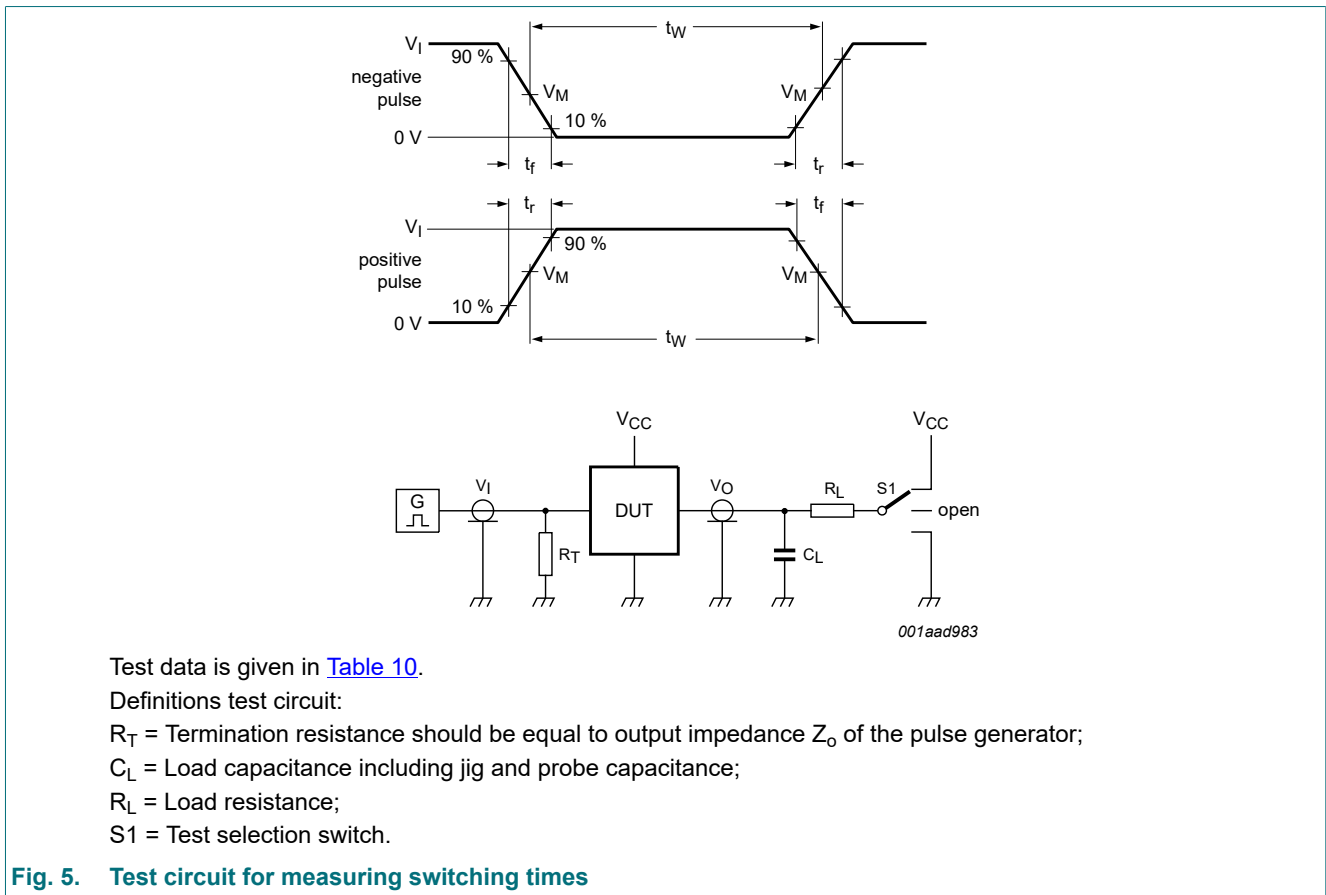


Table 10. Test data

| Input | | Load | | S1 position | | |
|--------------|------------|--------------|--------------|--------------------|--------------------|--------------------|
| V_I | t_r, t_f | C_L | R_L | t_{PHL}, t_{PLH} | t_{PZH}, t_{PHZ} | t_{PZL}, t_{PLZ} |
| GND to 3.0 V | 3.0 ns | 15 pF, 50 pF | 1 k Ω | open | GND | V_{CC} |

11. Package outline

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

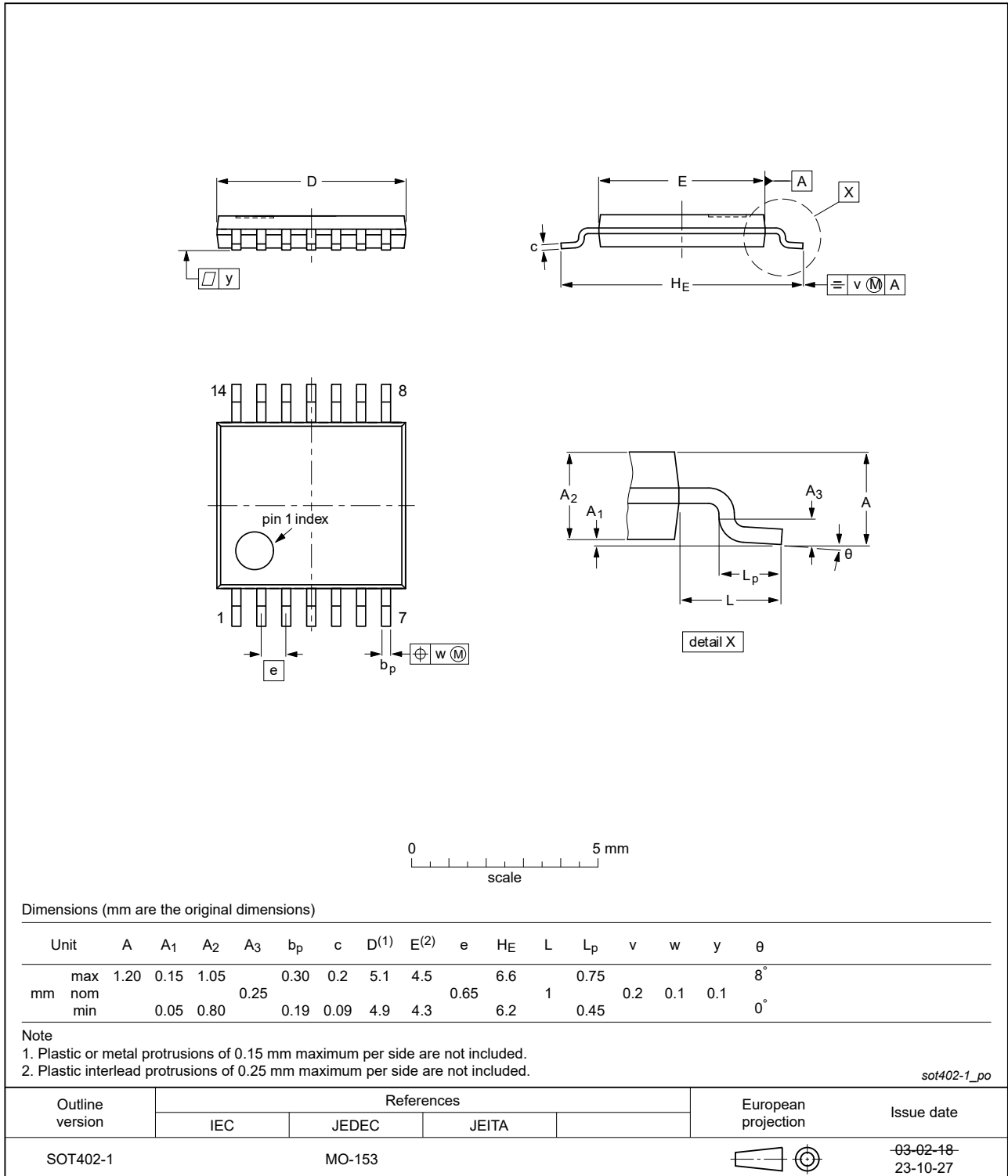


Fig. 6. Package outline SOT402-1 (TSSOP14)

12. Abbreviations

Table 11. Abbreviations

| Acronym | Description |
|---------|-----------------------------|
| CDM | Charge Device Model |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| TTL | Transistor-Transistor Logic |

13. Revision history

Table 12. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|----------------|---|--------------------|---------------|--------------|
| 74LV04AT v.2 | 20240111 | Product data sheet | - | 74LV04AT v.1 |
| Modifications: | <ul style="list-style-type: none"> Section 2: ESD specification updated according to the latest JEDEC standard. Section 7: Derating values for P_{tot} total power dissipation updated. Fig. 6: Aligned TSSOP package outline drawing to JEDEC MO-153 | | | |
| 74LV04AT v.1 | 20170518 | Product data sheet | - | - |

14. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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