

# 74HC374; 74HCT374

Octal D-type flip-flop; positive edge-trigger; 3-state

Rev. 5 — 7 September 2021

Product data sheet

## 1. General description

The 74HC374; 74HCT374 is an octal positive-edge triggered D-type flip-flop with 3-state outputs. The device features a clock (CP) and output enable ( $\overline{OE}$ ) inputs. The flip-flops will store the state of their individual D-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH clock (CP) transition. A HIGH on  $\overline{OE}$  causes the outputs to assume a high-impedance OFF-state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops. Inputs also include clamp diodes, this enables the use of current limiting resistors to interface inputs to voltages in excess of  $V_{CC}$ .

## 2. Features and benefits

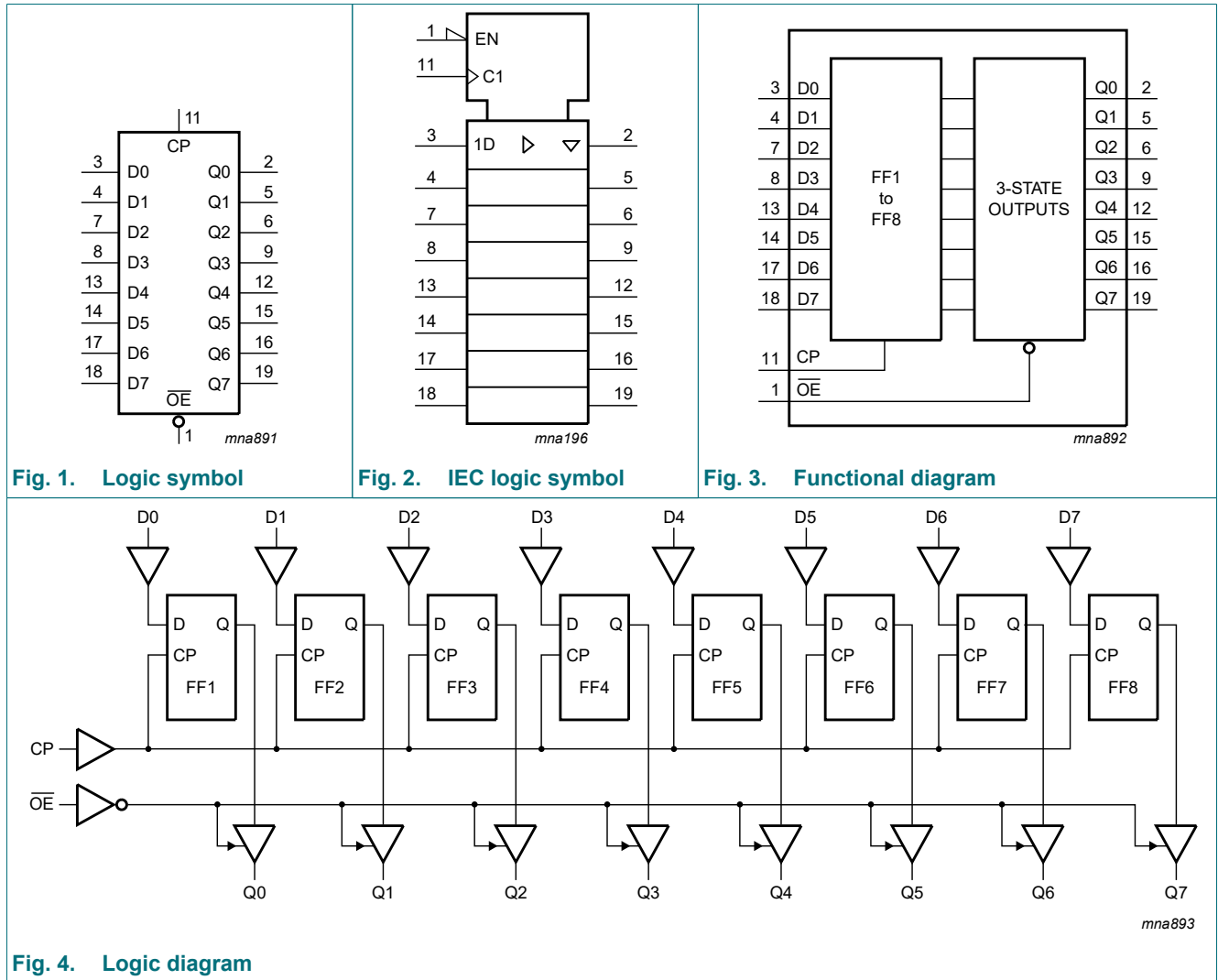
- Wide supply voltage range from 2.0 to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Input levels:
  - For 74HC374: CMOS level
  - For 74HCT374: TTL level
- Octal bus interface
- Non-inverting 3-state outputs
- 8-bit positive, edge-triggered register
- Common 3-state output enable input
- Independent register and 3-state buffer operation
- Complies with JEDEC standards
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

## 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC374D	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74HCT374D				
74HC374PW	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74HCT374PW				

### 4. Functional diagram



## 5. Pinning information

### 5.1. Pinning

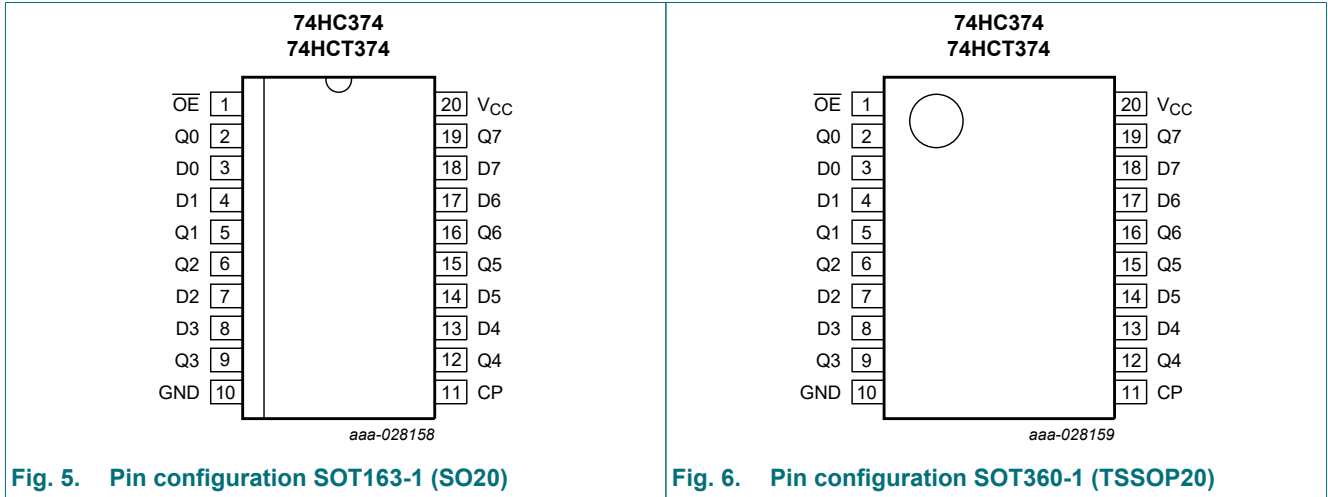


Fig. 5. Pin configuration SOT163-1 (SO20)

Fig. 6. Pin configuration SOT360-1 (TSSOP20)

### 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
D0, D1, D2, D3, D4, D5, D6, D7	3, 4, 7, 8, 13, 14, 17, 18	data inputs
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	2, 5, 6, 9, 12, 15, 16, 19	data outputs
$\overline{OE}$	1	output enable input (active LOW)
CP	11	clock pulse input (active rising edge)
GND	10	ground (0 V)
V <sub>CC</sub>	20	supply voltage

## 6. Functional description

Table 3. Function table

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;

L = LOW voltage level; l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;

Z = high-impedance OFF-state;  $\uparrow$  = LOW-to-HIGH clock transition.

Operating mode	Input			Internal flip-flops	Output Qn
	$\overline{OE}$	CP	Dn		
Load and read register	L	$\uparrow$	l	L	L
	L	$\uparrow$	h	H	H
Load register and disable outputs	H	$\uparrow$	l	L	Z
	H	$\uparrow$	h	H	Z

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	$\pm 20$	mA
$I_{OK}$	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	-	$\pm 20$	mA
$I_O$	output current	$-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$	-	$\pm 35$	mA
$I_{CC}$	supply current		-	70	mA
$I_{GND}$	ground current		-70	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	[1]	-	500	mW

- [1] For SOT163-1 (SO20) package:  $P_{tot}$  derates linearly with 12.3 mW/K above 109 °C.  
For SOT360-1 (TSSOP20) package:  $P_{tot}$  derates linearly with 10.0 mW/K above 100 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	74HC374			74HCT374			Unit
			Min	Typ	Max	Min	Typ	Max	
$V_{CC}$	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
$V_I$	input voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$V_O$	output voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	-	-	-	ns/V
$T_{amb}$	ambient temperature		-40	+25	+125	-40	+25	+125	°C

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T <sub>amb</sub> (°C)						Unit	
			25			-40 to +85		-40 to +125		
			Min	Typ	Max	Min	Max	Min		Max
<b>74HC374</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V <sub>CC</sub> = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V <sub>CC</sub> = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V <sub>CC</sub> = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I <sub>O</sub> = -6.0 mA; V <sub>CC</sub> = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
I <sub>O</sub> = -7.8 mA; V <sub>CC</sub> = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V		
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 6.0 mA; V <sub>CC</sub> = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
I <sub>O</sub> = 7.8 mA; V <sub>CC</sub> = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V		
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 6.0 V; V <sub>O</sub> = V <sub>CC</sub> or GND	-	-	±0.5	-	±5.0	-	±10	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 6.0 V	-	-	8.0	-	80	-	160	μA
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	-	-	pF

Symbol	Parameter	Conditions	T <sub>amb</sub> (°C)						Unit	
			25			-40 to +85		-40 to +125		
			Min	Typ	Max	Min	Max	Min		Max
<b>74HCT374</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = -20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -6 mA	3.98	4.32	-	3.84	-	3.7	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = 20 µA	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 6.0 mA	-	0.16	0.26	-	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 5.5 V; V <sub>O</sub> = V <sub>CC</sub> or GND	-	-	±0.5	-	±5.0	-	±10	µA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V; I <sub>O</sub> = 0 A	-	-	8.0	-	80	-	160	µA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>I</sub> = V <sub>CC</sub> - 2.1 V; other inputs at V <sub>CC</sub> or GND; V <sub>CC</sub> = 4.5 V to 5.5 V; I <sub>O</sub> = 0 A								
		$\overline{\text{OE}}$ input	-	125	450	-	563	-	613	µA
		CP input	-	90	324	-	405	-	441	µA
		Dn inputs	-	35	126	-	158	-	172	µA
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	-	-	pF

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 9.

Symbol	Parameter	Conditions	T <sub>amb</sub> (°C)						Unit	
			25			-40 to +85		-40 to +125		
			Min	Typ	Max	Min	Max	Min		Max
<b>74HC374</b>										
t <sub>pd</sub>	propagation delay	CP to Qn; see Fig. 7 [1]								
		V <sub>CC</sub> = 2.0 V	-	50	165	-	205	-	250	ns
		V <sub>CC</sub> = 4.5 V	-	18	33	-	41	-	50	ns
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	15	-	-	-	-	-	ns
		V <sub>CC</sub> = 6.0 V	-	14	28	-	35	-	43	ns
t <sub>en</sub>	enable time	OE to Qn; see Fig. 8 [2]								
		V <sub>CC</sub> = 2.0 V	-	41	150	-	190	-	225	ns
		V <sub>CC</sub> = 4.5 V	-	15	30	-	38	-	45	ns
		V <sub>CC</sub> = 6.0 V	-	12	26	-	33	-	38	ns
t <sub>dis</sub>	disable time	OE to Qn; see Fig. 8 [3]								
		V <sub>CC</sub> = 2.0 V	-	50	150	-	190	-	225	ns
		V <sub>CC</sub> = 4.5 V	-	18	30	-	38	-	45	ns
		V <sub>CC</sub> = 6.0 V	-	14	26	-	33	-	38	ns
t <sub>t</sub>	transition time	Qn; see Fig. 7 [4]								
		V <sub>CC</sub> = 2.0 V	-	14	60	-	75	-	90	ns
		V <sub>CC</sub> = 4.5 V	-	5	12	-	15	-	18	ns
		V <sub>CC</sub> = 6.0 V	-	4	10	-	13	-	15	ns
t <sub>w</sub>	pulse width	CP; HIGH or LOW; see Fig. 7								
		V <sub>CC</sub> = 2.0 V	80	19	-	100	-	120	-	ns
		V <sub>CC</sub> = 4.5 V	16	7	-	20	-	24	-	ns
		V <sub>CC</sub> = 6.0 V	14	6	-	17	-	20	-	ns
t <sub>su</sub>	set-up time	Dn to CP; see Fig. 7								
		V <sub>CC</sub> = 2.0 V	60	14	-	75	-	90	-	ns
		V <sub>CC</sub> = 4.5 V	12	5	-	15	-	18	-	ns
		V <sub>CC</sub> = 6.0 V	10	4	-	13	-	15	-	ns
t <sub>h</sub>	hold time	Dn to CP; see Fig. 7								
		V <sub>CC</sub> = 2.0 V	5	-6	-	5	-	5	-	ns
		V <sub>CC</sub> = 4.5 V	5	-2	-	5	-	5	-	ns
		V <sub>CC</sub> = 6.0 V	5	-2	-	5	-	5	-	ns
f <sub>max</sub>	maximum frequency	CP; see Fig. 7								
		V <sub>CC</sub> = 2.0 V	6.0	23	-	4.8	-	4.0	-	MHz
		V <sub>CC</sub> = 4.5 V	30	70	-	24	-	20	-	MHz
		V <sub>CC</sub> = 5 V; C <sub>L</sub> = 15 pF	-	77	-	-	-	-	-	MHz
		V <sub>CC</sub> = 6.0 V	35	83	-	28	-	24	-	MHz
C <sub>PD</sub>	power dissipation capacitance	per flip-flop; V <sub>I</sub> = GND to V <sub>CC</sub> [5]	-	17	-			-	-	pF

## Octal D-type flip-flop; positive edge-trigger; 3-state

Symbol	Parameter	Conditions	T <sub>amb</sub> (°C)						Unit	
			25			-40 to +85		-40 to +125		
			Min	Typ	Max	Min	Max	Min		Max
<b>74HCT374</b>										
t <sub>pd</sub>	propagation delay	CP to Qn; see Fig. 7 [1]								
		V <sub>CC</sub> = 4.5 V	-	16	32	-	40	-	48	ns
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	13	-	-	-	-	-	ns
t <sub>en</sub>	enable time	OE to Qn; V <sub>CC</sub> = 4.5 V; see Fig. 8 [2]	-	16	30	-	38	-	45	ns
t <sub>dis</sub>	disable time	OE to Qn; V <sub>CC</sub> = 4.5 V; see Fig. 8 [3]	-	18	28	-	35	-	42	ns
t <sub>t</sub>	transition time	Qn; V <sub>CC</sub> = 4.5 V; see Fig. 7 [4]	-	5	12	-	15	-	18	ns
t <sub>W</sub>	pulse width	CP; HIGH or LOW; V <sub>CC</sub> = 4.5 V; see Fig. 7	19	11	-	24	-	29	-	ns
t <sub>su</sub>	set-up time	Dn to CP; V <sub>CC</sub> = 4.5 V; see Fig. 7	12	7	-	15	-	18	-	ns
t <sub>h</sub>	hold time	Dn to CP; V <sub>CC</sub> = 4.5 V; see Fig. 7	5	-3	-	5	-	5	-	ns
f <sub>max</sub>	maximum frequency	CP; V <sub>CC</sub> = 4.5 V; see Fig. 7	26	44	-	21	-	17	-	MHz
		CP; V <sub>CC</sub> = 5 V; C <sub>L</sub> = 15 pF	-	48	-	-	-	-	-	MHz
C <sub>PD</sub>	power dissipation capacitance	per flip-flop; V <sub>I</sub> = GND to V <sub>CC</sub> - 1.5 V [5]	-	17	-			-	-	pF

[1] t<sub>pd</sub> is the same as t<sub>PHL</sub> and t<sub>PLH</sub>.

[2] t<sub>en</sub> is the same as t<sub>PZH</sub> and t<sub>PZL</sub>.

[3] t<sub>dis</sub> is the same as t<sub>PHZ</sub> and t<sub>PLZ</sub>.

[4] t<sub>t</sub> is the same as t<sub>THL</sub> and t<sub>TLH</sub>.

[5] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

C<sub>L</sub> = output load capacitance in pF;

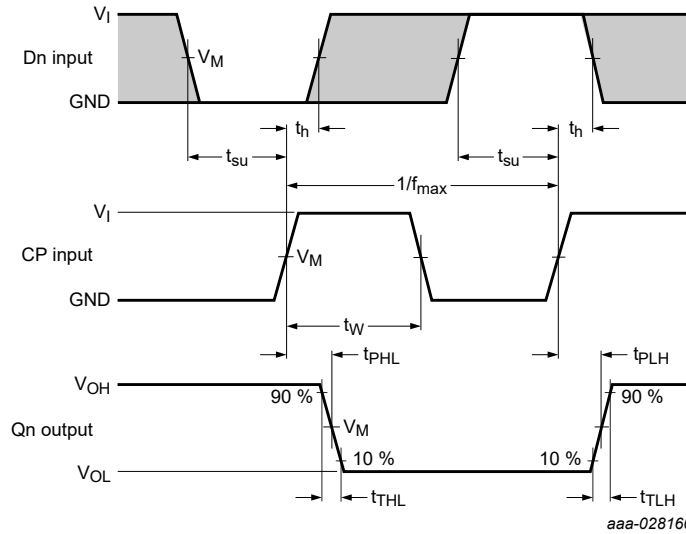
V<sub>CC</sub> = supply voltage in V;

N = number of inputs switching;

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs.

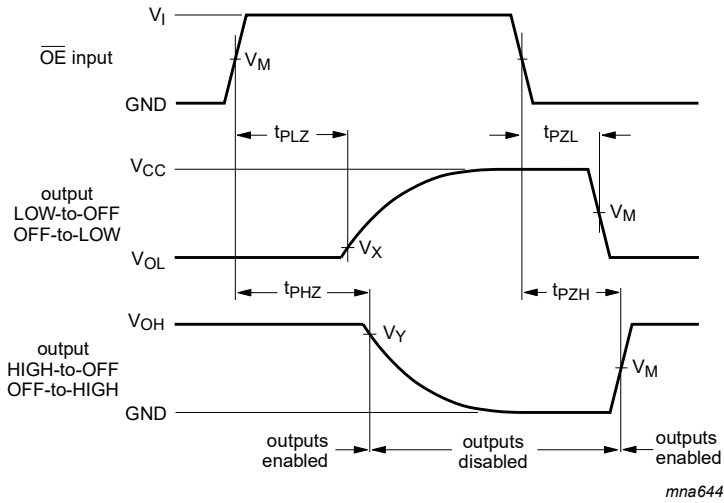


10.1. Waveforms and test circuit



Measurement points are given in [Table 8](#).  
 The shaded areas indicate when the input is permitted to change for predictable output performance.  
 $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig. 7. Clock input (CP) to output (Qn) propagation delay, clock pulse width, data (Dn) to clock (CP) set-up and hold times, output transition times (Qn) and maximum clock frequency**

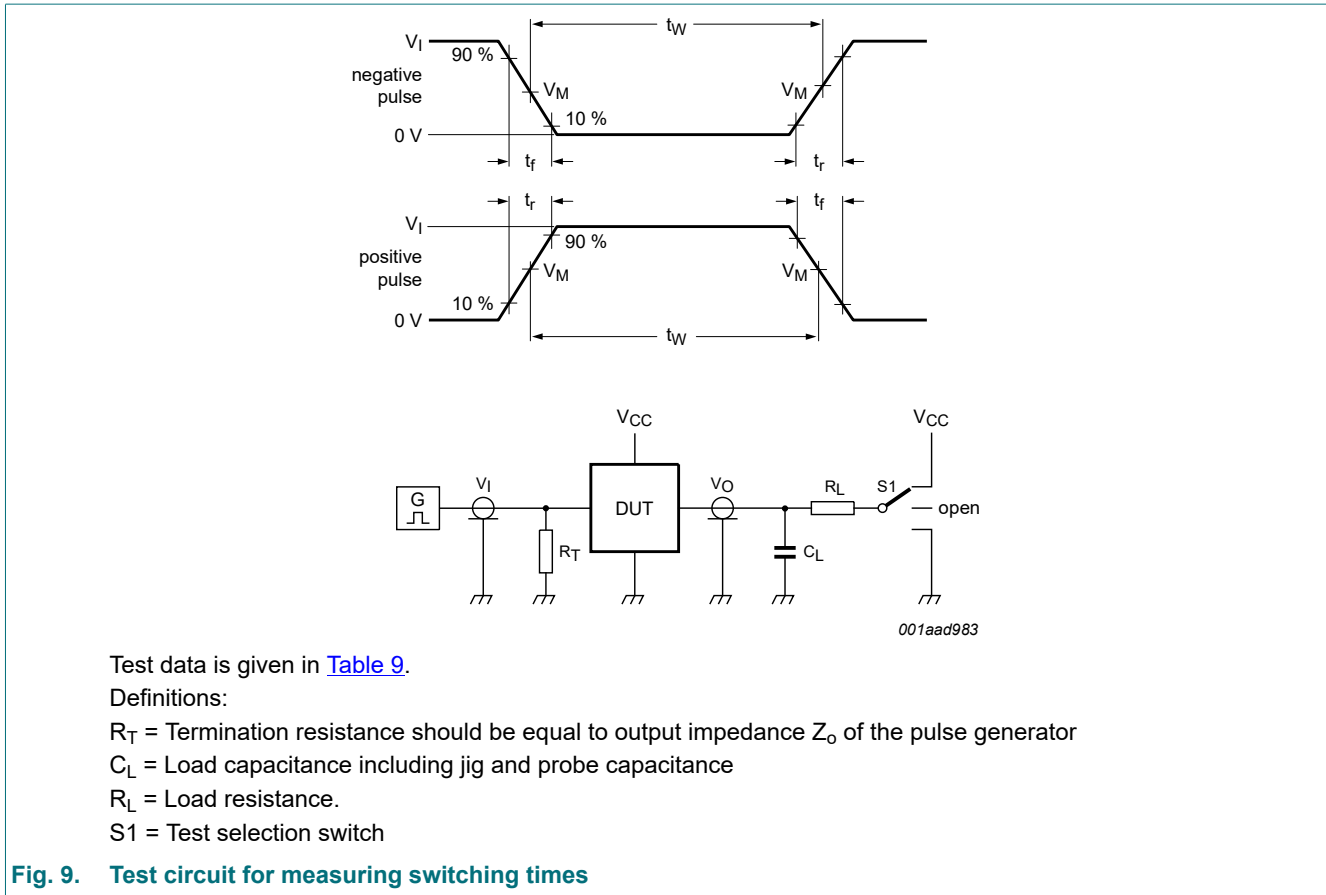


Measurement points are given in [Table 8](#).  
 $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig. 8. 3-state enable and disable times**

**Table 8. Measurement points**

Type	Input		Output		
	$V_I$	$V_M$	$V_M$	$V_X$	$V_Y$
74HC374	GND to $V_{CC}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$0.1 \times V_{CC}$	$0.9 \times V_{CC}$
74HCT374	GND to 3 V	1.3 V	1.3 V	$0.1 \times V_{CC}$	$0.9 \times V_{CC}$



**Table 9. Test data**

Type	Input		Load		S1 position		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
74HC374	GND to $V_{CC}$	6 ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$
74HCT374	GND to 3 V	6 ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$

11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



Fig. 10. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

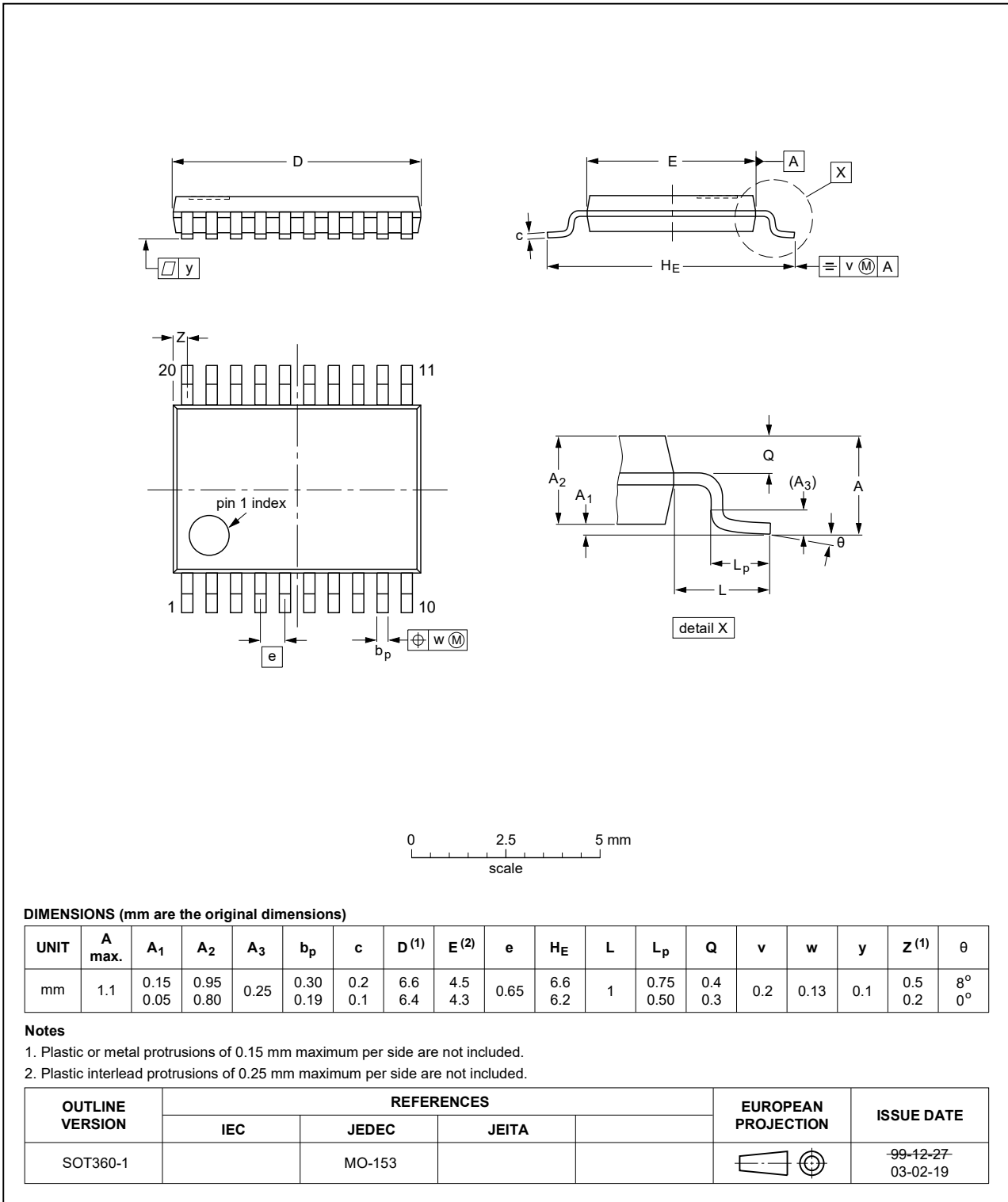


Fig. 11. Package outline SOT360-1 (TSSOP20)

## 12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT374 v.5	20210907	Product data sheet	-	74HC_HCT374 v.4
Modifications:	<ul style="list-style-type: none"> <li>Types 74HC374 and 74HCT374 (SOT339-1/SSOP20) removed</li> </ul>			
74HC_HCT374 v.4	20210302	Product data sheet	-	74HC_HCT374 v.3
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Section 2</a> updated.</li> <li><a href="#">Section 7</a>: Derating values for <math>P_{tot}</math> total power dissipation updated.</li> </ul>			
74HC_HCT374 v.3	20180220	Product data sheet	-	74HC_HCT374 v.2
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>			
74HC_HCT374 v.2	19901201	Product specification	-	-

## Octal D-type flip-flop; positive edge-trigger; 3-state

## 14. Legal information

## Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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Date of release: 7 September 2021