

1. General description

The 74HC280; 74HCT280 is a 9-bit parity generator or checker. Both even and odd parity outputs are available. The even parity output (PE) is HIGH when an even number of data inputs (I0 to I8) is HIGH. The odd parity output (PO) is HIGH when an odd number of data inputs are HIGH. Expansion to larger word sizes is accomplished by tying the even outputs (PE) of up to nine parallel devices to the final stage data inputs. Inputs include clamp diodes. It enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Word-length easily expanded by cascading
- · Generates either odd or even parity for nine data bits
- Wide supply voltage range from 2.0 to 6.0 V
- Input levels:
 - For 74HC280: CMOS level
 - For 74HCT280: TTL level
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards
 - JESD8C (2.7 V to 3.6 V)
 - JESD7A (2.0 V to 6.0 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

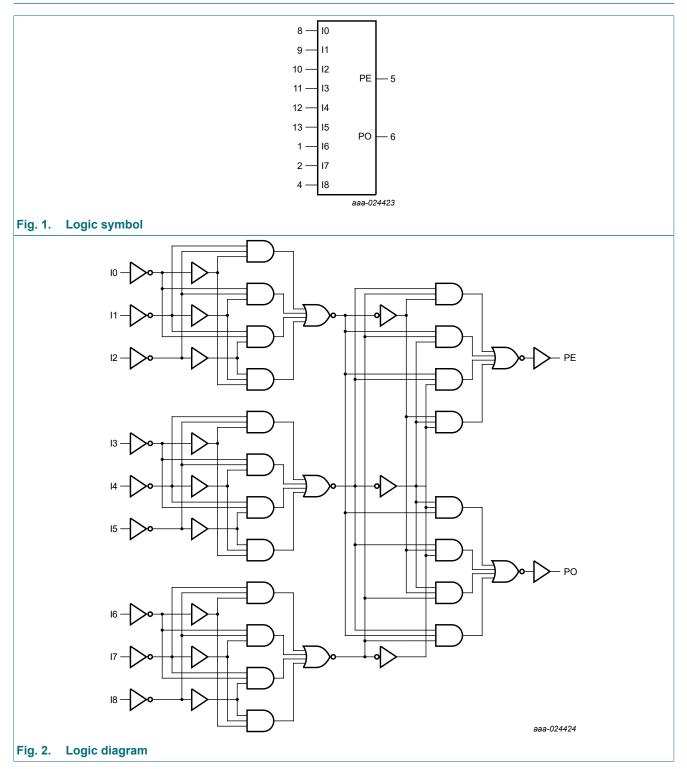
3. Ordering information

Table 1. Ordering information							
Type number	Temperature range	Name	Description	Version			
74HC280D 74HCT280D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	<u>SOT108-1</u>			
74HCT280PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	<u>SOT402-1</u>			

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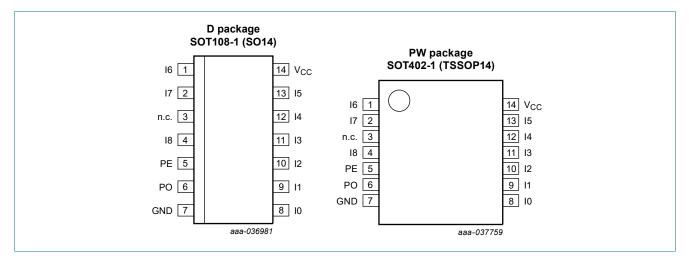
9-bit odd/even parity generator/checker

4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description					
10, 11, 12, 13, 14, 15, 16, 17, 18	8, 9, 10, 11, 12, 13, 1, 2, 4	data input					
GND	7	ground (0 V)					
PE	5	even parity output					
PO	6	odd parity output					
V _{CC}	14	supply voltage					

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level

Inputs	Outputs					
number of HIGH data inputs (I0 to I8)	PE	РО				
even	Н	L				
odd	L	Н				

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CC}	supply voltage			-0.5	+7	V
I _{IK}	input clamping current	V_{I} < -0.5 V or V_{I} > V_{CC} + 0.5 V	[1]	-	±20	mA
I _{OK}	output clamping current	$V_{\rm O}$ < -0.5 V or $V_{\rm O}$ > $V_{\rm CC}$ + 0.5 V	[1]	-	±20	mA
I _O	output current	$-0.5 V < V_O < V_{CC} + 0.5 V$		-	±25	mA
I _{CC}	supply current			-	50	mA
I _{GND}	ground current			-50	-	mA
T _{stg}	storage temperature			-65	+150	°C
P _{tot}	total power dissipation		[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.

For SOT402-1 (TSSOP14) package: Ptot derates linearly with 7.3 mW/K above 81 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions		74HC280		74HCT280			Unit
			Min	Тур	Max	Min	Тур	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
VI	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
Vo	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		-40 °C t	o +85 °C	-40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Мах	Min	Max	1
74HC28	0									
V _{IH}	HIGH-level	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
	input voltage	V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
	input voltage	V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level	V _I = V _{IH} or V _{IL}								
	output voltage	I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = -4.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I _O = -5.2 mA; V _{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V _{OL}	LOW-level	V _I = V _{IH} or V _{IL}								1
	output voltage	I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
	I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V	
l _l	input leakage current	$V_{I} = V_{CC}$ or GND; $V_{CC} = 6.0 V$	-	-	±0.1	-	±1.0	-	±1.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	8.0	-	80	-	160	μA
CI	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT2	80			I	I					-
V _{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level	$V_{I} = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 V$								
	output voltage	I _O = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level	$V_{I} = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 V$								-
	output voltage	I _O = 20 μA	-	0	0.1	_	0.1	-	0.1	V
		I _O = 4.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
I	input leakage current	$V_{I} = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	±0.1	-	±1.0	-	±1.0	μA
I _{CC}		$V_{I} = V_{CC}$ or GND; $V_{CC} = 5.5$ V; $I_{O} = 0$ A	-	-	8.0	-	80	-	160	μA

9-bit odd/even parity generator/checker

Symbol	bol Parameter Conditions			25 °C		-40 °C to	o +85 °C	5 °C -40 °C to +125 °C		Unit
			Min	Тур	Мах	Min	Max	Min	Мах	
ΔI _{CC}	additional supply current	per input pin; V _I = V _{CC} - 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V; I _O = 0 A								
		In inputs	-	100	360	-	450	-	490	μA
CI	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see Fig. 4.

Symbol	Parameter	Conditions		25 °C		-40 °C to	• +85 °C	-40 °C to	+125 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
74HC28	0									
t _{pd}	propagation	In to PE; see <u>Fig. 3</u> [1]								
	delay	V _{CC} = 2.0 V	-	55	200	-	250	-	300	ns
		V _{CC} = 4.5 V	-	20	40	-	50	-	60	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	17	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	16	34	-	43	-	51	ns
		In to PO; see <u>Fig. 3</u>								
		V _{CC} = 2.0 V	-	63	200	-	250	-	300	ns
		V _{CC} = 4.5 V	-	23	40	-	50	-	60	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	20	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	18	34	-	43	-	51	ns
t _t	transition	see <u>Fig. 3</u> [2]								
	time	V _{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V _{CC} = 6.0 V	-	6	13	-	16	-	19	ns
C _{PD}	power dissipation capacitance	per package; V _I = GND to V _{CC} [3]	-	65	-	-	-	-	-	pF

9-bit odd/even parity generator/checker

Symbol	Parameter	Conditions		25 °C		-40 °C to	o +85 °C	-40 °C to	+125 °C	Unit
			Mir	Тур	Max	Min	Max	Min	Max	
74HCT2	80									
t _{pd}	propagation	In to PE; see Fig. 3 [1]							
	delay	V _{CC} = 4.5 V	-	21	42	-	53	-	63	ns
	V _{CC} = 5.0 V; C _L = 15 pF	-	18	-	-	-	-	-	ns	
		In to PO; see <u>Fig. 3</u>								
		V _{CC} = 4.5 V	-	26	45	-	56	-	68	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	22	-	-	-	-	-	ns
t _t	transition	see <u>Fig. 3</u> [2]							
	time	V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
C _{PD}	power dissipation capacitance	per package; [3 V _I = GND to V _{CC} - 1.5 V] -	65	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH} .

[2]

[3]

f_o = output frequency in MHz;

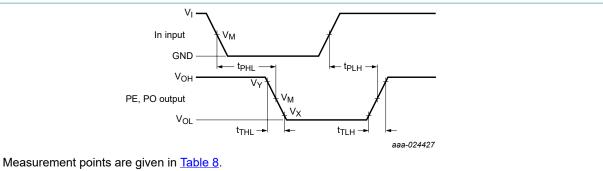
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

 $\sum (C_L \times V_{CC}^2 \times f_o) = \text{sum of outputs.}$

10.1. Waveforms and test circuit



 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Input (In) to output (PE, PO) propagation delays and output transition times Fig. 3.

Table 8. Measurement points

Туре	Input	Output					
	V _M	V _M	V _X	V _Y			
74HC280	0.5 × V _{CC}	0.5 × V _{CC}	0.1 × V _{CC}	0.9 × V _{CC}			
74HCT280	1.3 V	1.3 V	0.1 × V _{CC}	$0.9 \times V_{CC}$			

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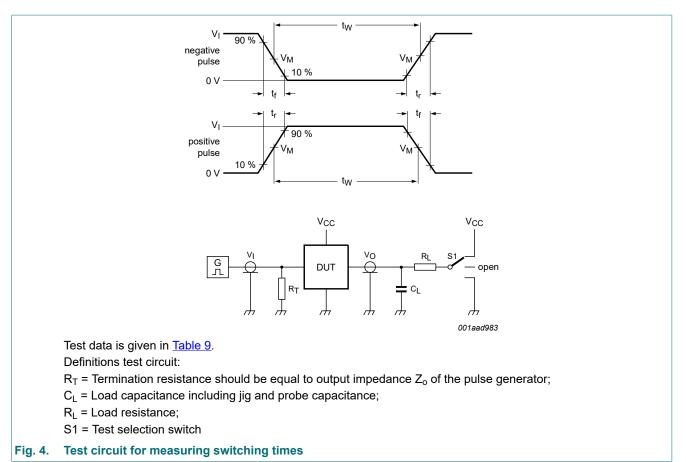
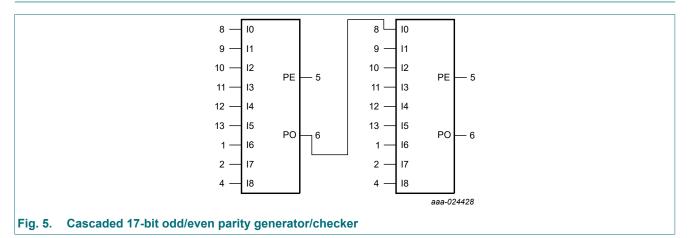


Table 9. Test data

Туре	Input L		Load	Load		
	VI	t _r , t _f	CL	RL	t _{PHL} , t _{PLH}	
74HC280	V _{CC}	6 ns	15 pF, 50 pF	1 kΩ	open	
74HCT280	3 V	6 ns	15 pF, 50 pF	1 kΩ	open	

11. Application information



74HC_HCT280

12. Package outline

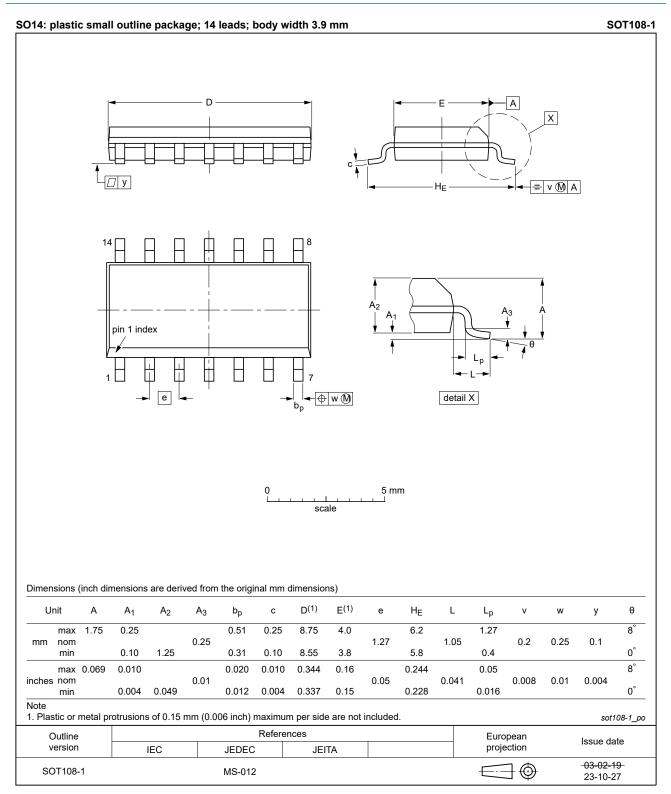


Fig. 6. Package outline SOT108-1 (SO14)

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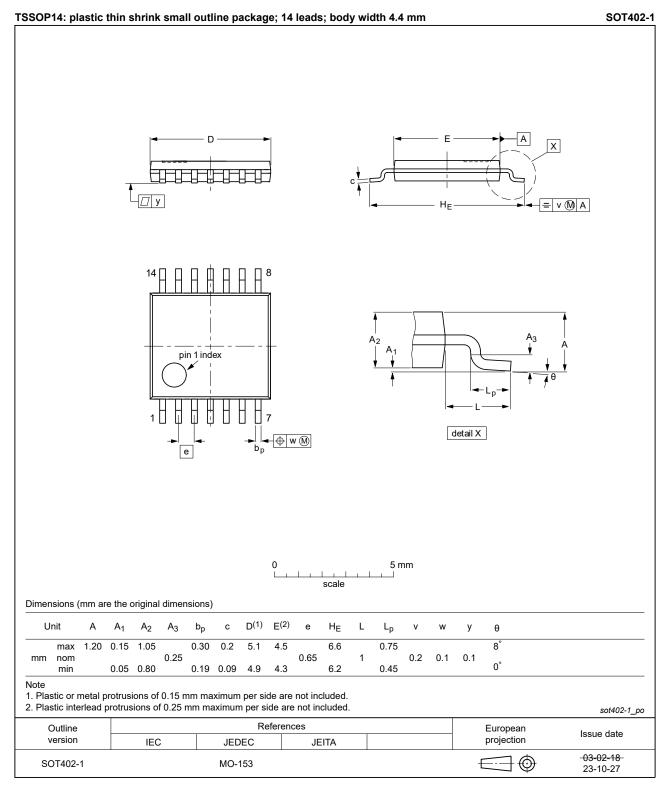


Fig. 7. Package outline SOT402-1 (TSSOP14)

13. Abbreviations

Table 10. Abbreviations						
Acronym	Description					
CDM	Charged Device Model					
CMOS	Complementary Metal-Oxide Semiconductor					
DUT	Device Under Test					
ESD	ElectroStatic Discharge					
НВМ	Human Body Model					
TTL	Transistor-Transistor Logic					

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes		
74HC_HCT280 v.5	20240115	Product data sheet	-	74HC_HCT280 v.4		
Modifications:		 <u>Section 2</u>: ESD specification updated according to the latest JEDEC standard. <u>Fig. 6</u>, <u>Fig. 7</u>: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153 				
74HC_HCT280 v.4	20210816	Product data sheet	-	74HC_HCT280 v.3		
Modifications:	guidelines c Legal texts Type numbe Type numbe	 The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Type number 74HCT280DB (SOT337-1/SSOP14) removed. Type number 74HCT280PW (SOT402-1/TSSOP14) added. Section 7: Derating values for P_{tot} total power dissipation updated. 				
74HC_HCT280 v.3	20160915	Product data sheet	-	74HC_HCT280 v.2		
Modifications:	guidelines o Legal texts	 The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. Type numbers 74HC280N, 74HCT280N removed. 				
74HC_HCT280 v.2	19901201	Product specification	-	-		

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

 Please consult the most recently issued document before initiating or completing a design.

- [2] The term 'short data sheet' is explained in section "Definitions".
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