

74HCS74

Dual D-type flip-flop with Schmitt-trigger inputs; set and reset; positive edge-trigger

Rev. 1 — 27 June 2025

Product data sheet

1. General description

The 74HCS74 is a dual positive edge triggered D-type flip-flop. They have individual data (nD), clock (nCP), set (nSD) and reset (nRD) inputs, and complementary nQ and nQ outputs. Data at the nD-input, that meets the set-up and hold time requirements on the LOW-to-HIGH clock transition, is stored in the flip-flop and appears at the nQ output. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

All inputs are Schmitt-trigger inputs, capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

2. Features and benefits

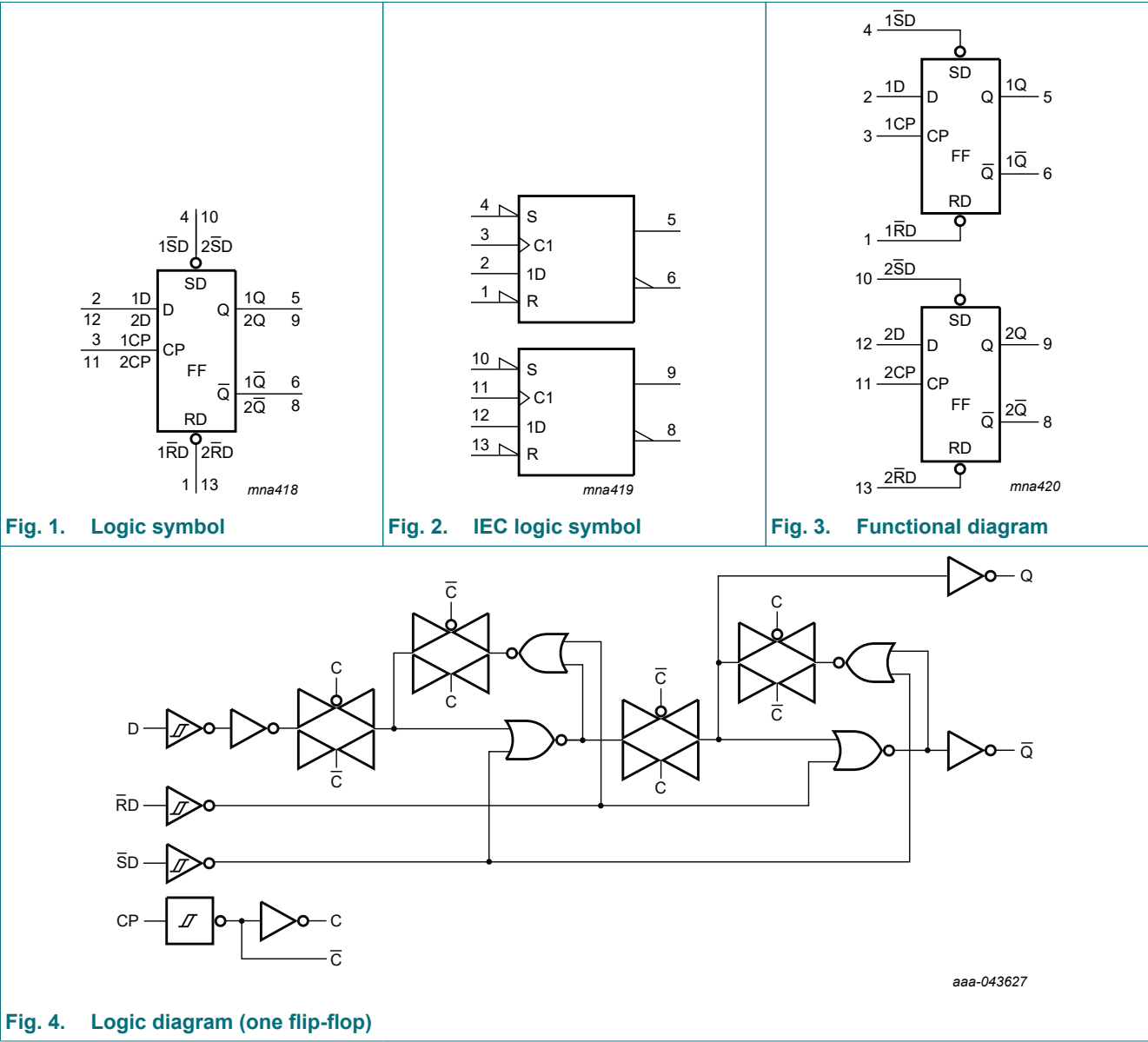
- Wide supply voltage range from 2.0 V to 6.0 V
- Schmitt-trigger inputs
- Low power consumption
 - Typical supply current (I_{CC}) of 100 nA
 - Typical input leakage current (I_I) of ± 10 nA
- ± 7.8 mA output drive at 6 V
- Symmetrical output impedance
- Balanced propagation delays
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
 - JESD7A (2.0 V to 6.0 V)
- ESD protection:
 - HBM ANSI/ESDA/JEDEC JS-001 class 3A exceeds 4000 V
 - CDM ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1500 V
- Multiple package options
- Specified from -40 °C to $+85$ °C and from -40 °C to $+125$ °C

3. Ordering information

Table 1. Ordering information

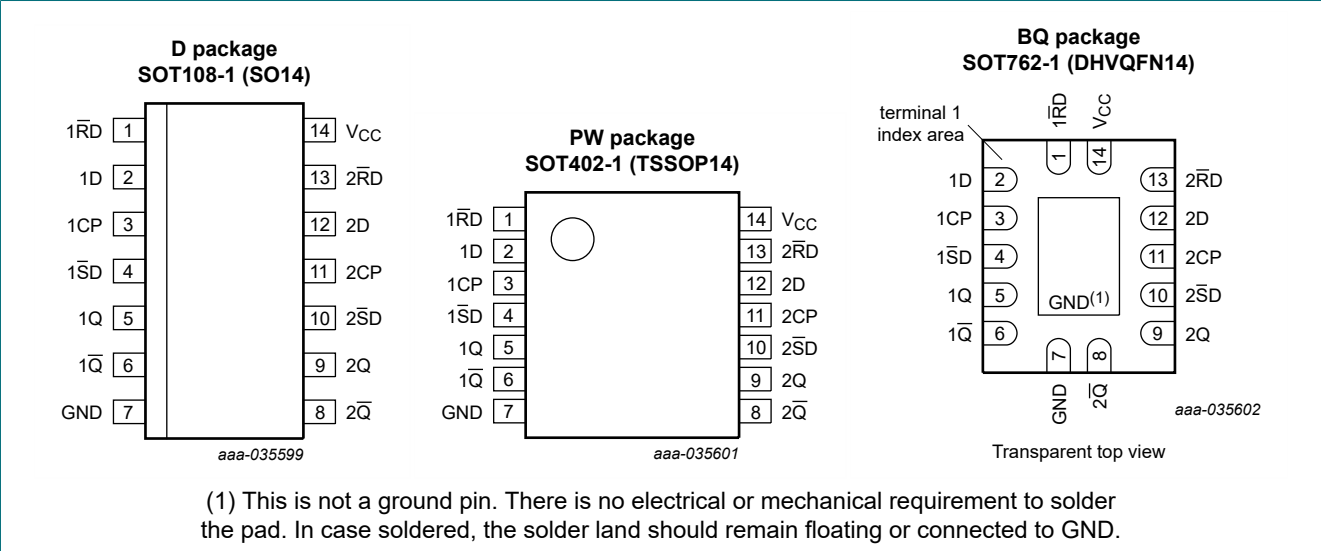
Type number	Package			
	Temperature range	Name	Description	Version
74HCS74D	-40 °C to $+125$ °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HCS74PW	-40 °C to $+125$ °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74HCS74BQ	-40 °C to $+125$ °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body $2.5 \times 3 \times 0.85$ mm	SOT762-1

4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1RD	1	asynchronous reset-direct input (active LOW)
1D	2	data input
1CP	3	clock input (LOW-to-HIGH, edge-triggered)
1SD	4	asynchronous set-direct input (active LOW)
1Q	5	output
1Q	6	complement output
GND	7	ground (0 V)
2Q	8	complement output
2Q	9	output
2SD	10	asynchronous set-direct input (active LOW)
2CP	11	clock input (LOW-to-HIGH, edge-triggered)
2D	12	data input
2RD	13	asynchronous reset-direct input (active LOW)
VCC	14	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Input				Output	
nSD	nRD	nCP	nD	nQ	nQ̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care;
↑ = LOW-to-HIGH transition; Q_{n+1} = state after the next LOW-to-HIGH CP transition.

Input				Output	
nSD	nRD	nCP	nD	nQ _{n+1}	nQ̄ _{n+1}
H	H	↑	L	L	H
H	H	↑	H	H	L

7. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V [1]	-	±20	mA
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V [1]	-	±20	mA
I _O	output current	V _O = 0 V to V _{CC}	-	±35	mA
I _{CC}	supply current		-	70	mA
I _{GND}	ground current		-70	-	mA
T _j	junction temperature	[2]	-	+150	°C
T _{stg}	storage temperature		-65	+150	°C
V _{ESD}	electrostatic discharge	HBM ANSI/ESDA/JEDEC JS-001 class 3A exceeds 4000 V	-	±4000	V
		CDM ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1500 V	-	±1500	V
P _{tot}	total power dissipation	[3]	-	500	mW

- [1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- [2] Guaranteed by design.
- [3] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.
For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.
For SOT762-1 (DHVQFN14) package: P_{tot} derates linearly with 9.6 mW/K above 98 °C.

8. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		2.0	5.0	6.0	V
V _I	input voltage		0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	°C

9. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V _{T+}	positive-going threshold voltage	see Fig. 5 and Fig. 6								
		V _{CC} = 2.0 V	0.7	-	1.5	0.7	1.5	0.7	1.5	V
		V _{CC} = 4.5 V	1.7	-	3.15	1.7	3.15	1.7	3.15	V
		V _{CC} = 6 V	2.1	-	4.2	2.1	4.2	2.1	4.2	V
		V _{CC} = 3.0 V to 3.6 V	0.4V _{CC}	-	0.7V _{CC}	0.4V _{CC}	0.7V _{CC}	0.4V _{CC}	0.7V _{CC}	V
		V _{CC} = 4.5 V to 5.5 V	0.38V _{CC}	-	0.7V _{CC}	0.38V _{CC}	0.7V _{CC}	0.38V _{CC}	0.7V _{CC}	V
V _{T-}	negative-going threshold voltage	see Fig. 5 and Fig. 6								
		V _{CC} = 2.0 V	0.3	-	1.0	0.3	1.0	0.3	1.0	V
		V _{CC} = 4.5 V	0.9	-	2.2	0.9	2.2	0.9	2.2	V
		V _{CC} = 6 V	1.2	-	3.0	1.2	3.0	1.2	3.0	V
		V _{CC} = 3.0 V to 3.6 V	0.2V _{CC}	-	0.5V _{CC}	0.2V _{CC}	0.5V _{CC}	0.2V _{CC}	0.5V _{CC}	V
		V _{CC} = 4.5 V to 5.5 V	0.2V _{CC}	-	0.49V _{CC}	0.2V _{CC}	0.49V _{CC}	0.2V _{CC}	0.49V _{CC}	V
V _H	hysteresis voltage[1]	see Fig. 5 and Fig. 6								
		V _{CC} = 2.0 V	0.2	0.52	1.0	0.2	1.0	0.2	1.0	V
		V _{CC} = 4.5 V	0.4	0.85	1.4	0.4	1.4	0.4	1.4	V
		V _{CC} = 6 V	0.6	1.1	1.6	0.6	1.6	0.6	1.6	V
		V _{CC} = 3.0 V to 3.6 V	0.1V _{CC}	0.72	0.38V _{CC}	0.1V _{CC}	0.38V _{CC}	0.1V _{CC}	0.38V _{CC}	V
		V _{CC} = 4.5 V to 5.5 V	0.09V _{CC}	0.94	0.29V _{CC}	0.09V _{CC}	0.29V _{CC}	0.09V _{CC}	0.29V _{CC}	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _{OH} = -20 µA; V _{CC} = 2.0 V to 6 V	V _{CC} -0.1	V _{CC} -0.002	-	V _{CC} -0.1	-	V _{CC} -0.1	-	V
		I _{OH} = -4 mA; V _{CC} = 3.0 V	2.7	2.85	-	2.7	-	2.7	-	V
		I _{OH} = -6 mA; V _{CC} = 4.5 V	4.0	4.3	-	4.0	-	4.0	-	V
		I _{OH} = -7.8 mA; V _{CC} = 6.0 V	5.48	5.75	-	5.4	-	5.4	-	V

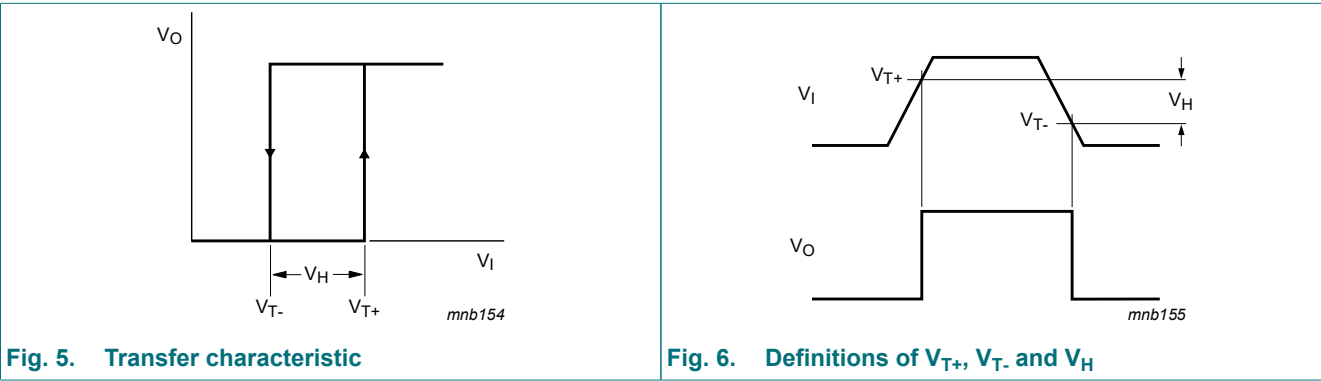
Dual D-type flip-flop with Schmitt-trigger inputs; set and reset; positive edge-trigger

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _{OL} = 20 µA; V _{CC} = 2.0 V to 6 V	-	0.002	0.1	-	0.1	-	0.1	V
		I _{OL} = 4 mA; V _{CC} = 3.0 V	-	0.14	0.25	-	0.25	-	0.25	V
		I _{OL} = 6 mA; V _{CC} = 4.5 V	-	0.18	0.26	-	0.30	-	0.30	V
		I _{OL} = 7.8 mA; V _{CC} = 6.0 V	-	0.22	0.26	-	0.33	-	0.33	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	±0.01	±0.1	-	±0.25	-	±1.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	0.1	-	-	0.5	-	2.0	µA

[1] Guaranteed by design.

9.1. Transfer characteristic waveforms and graphs

9.1.1. For inputs



Dual D-type flip-flop with Schmitt-trigger inputs; set and reset; positive edge-trigger

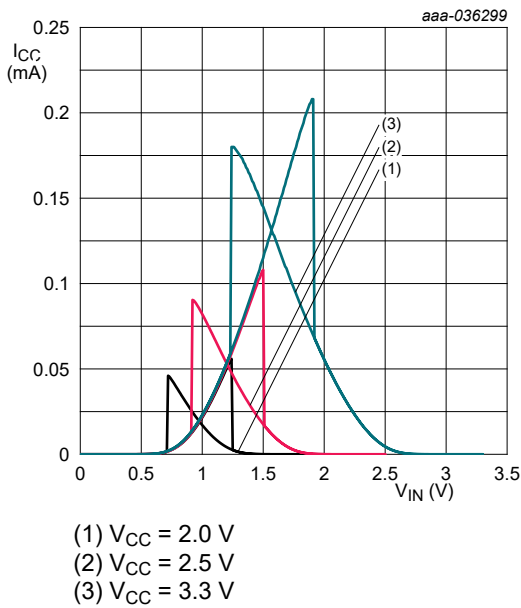


Fig. 7. Typical supply current vs the input voltage

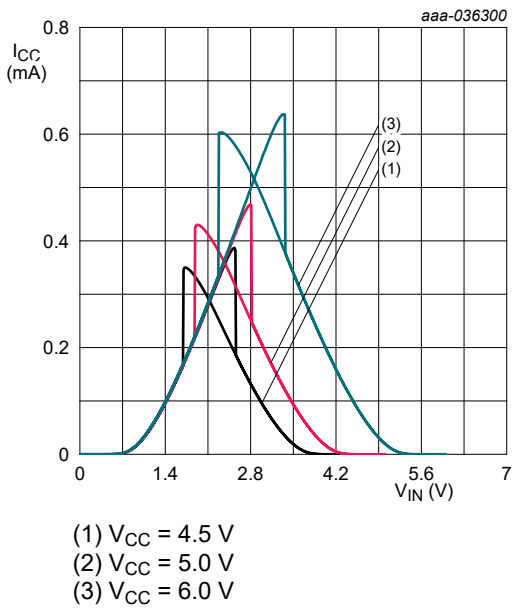


Fig. 8. Typical supply current vs the input voltage

9.1.2. For outputs

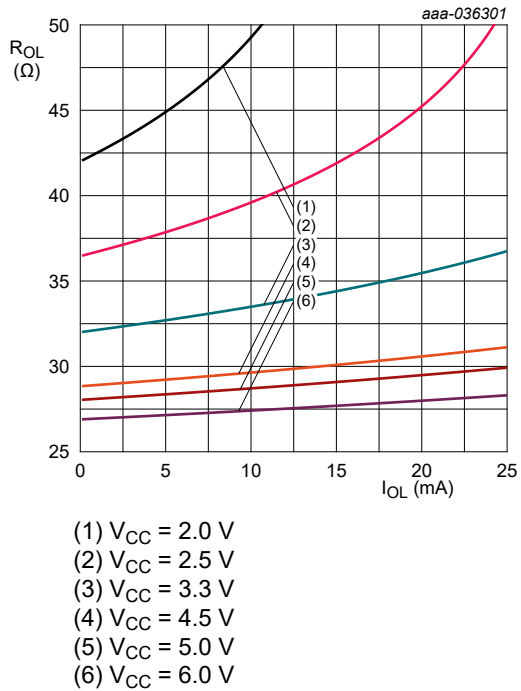


Fig. 9. Typical LOW-level output resistance as function of the output current

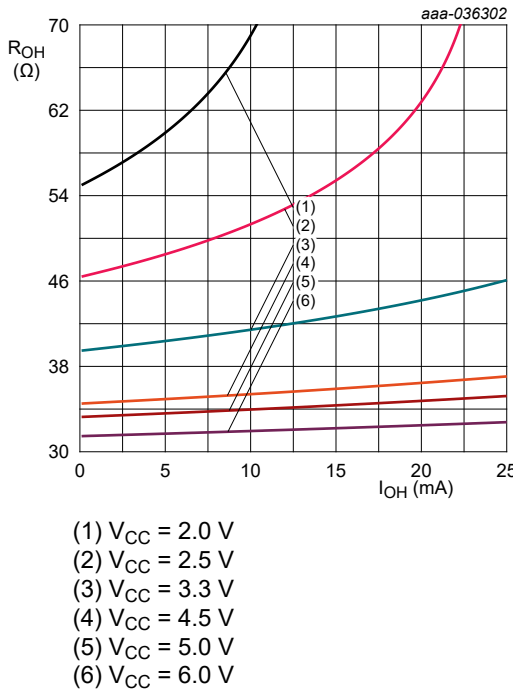


Fig. 10. Typical HIGH-level output resistance as function of the output current

10. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see [Section 10.1](#).

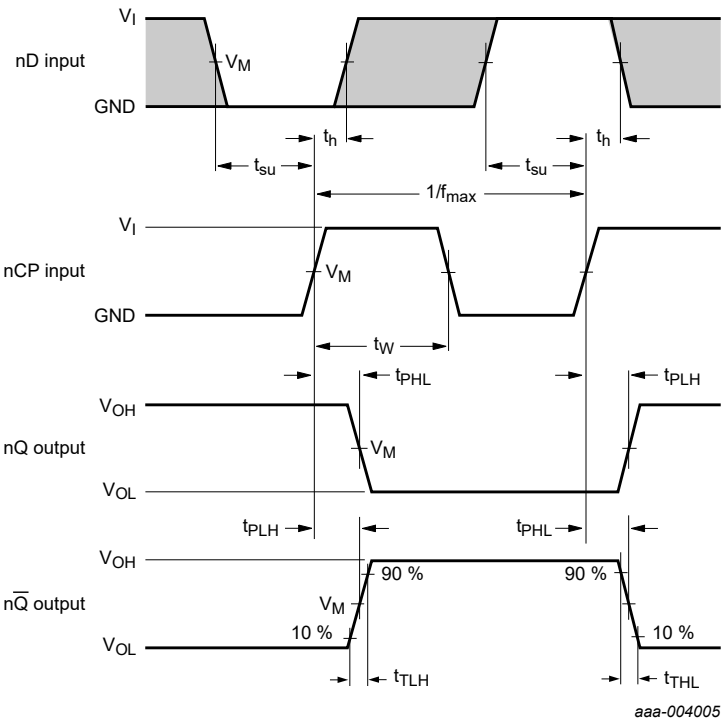
Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
t _{pd}	propagation delay	nCP to nQ, n \overline{Q} ; see Fig. 11 [2]								
		V _{CC} = 2 V	-	19	33	-	39	-	42	ns
		V _{CC} = 4.5 V	-	8	16	-	18	-	19	ns
		V _{CC} = 6 V	-	7	13	-	14	-	15	ns
		V _{CC} = 3.0 V to 3.6 V	-	10	22	-	26	-	28	ns
		V _{CC} = 4.5 V to 5.5 V	-	8	16	-	18	-	19	ns
		n \overline{SD} to nQ, n \overline{Q} ; see Fig. 12								
		V _{CC} = 2 V	-	19	33	-	39	-	42	ns
		V _{CC} = 4.5 V	-	8	16	-	18	-	19	ns
		V _{CC} = 6 V	-	7	13	-	14	-	15	ns
		V _{CC} = 3.0 V to 3.6 V	-	10	22	-	26	-	28	ns
		V _{CC} = 4.5 V to 5.5 V	-	8	16	-	18	-	19	ns
		n \overline{RD} to nQ, n \overline{Q} ; see Fig. 12								
		V _{CC} = 2 V	-	19	33	-	39	-	42	ns
		V _{CC} = 4.5 V	-	8	16	-	18	-	19	ns
		V _{CC} = 6 V	-	7	13	-	14	-	15	ns
		V _{CC} = 3.0 V to 3.6 V	-	10	22	-	26	-	28	ns
		V _{CC} = 4.5 V to 5.5 V	-	8	16	-	18	-	19	ns
t _w	pulse width	nCP HIGH or LOW; see Fig. 11								
		V _{CC} = 2 V	12	-	-	14	-	14	-	ns
		V _{CC} = 4.5 V	10	-	-	12	-	12	-	ns
		V _{CC} = 6 V	9	-	-	11	-	11	-	ns
		V _{CC} = 3.0 V to 3.6 V	11	-	-	13	-	13	-	ns
		V _{CC} = 4.5 V to 5.5 V	10	-	-	12	-	12	-	ns
		n \overline{SD} , n \overline{RD} LOW; see Fig. 12								
		V _{CC} = 2 V	11	-	-	11	-	11	-	ns
		V _{CC} = 4.5 V	11	-	-	11	-	11	-	ns
		V _{CC} = 6 V	11	-	-	11	-	11	-	ns
		V _{CC} = 3.0 V to 3.6 V	11	-	-	11	-	11	-	ns
		V _{CC} = 4.5 V to 5.5 V	11	-	-	11	-	11	-	ns
t _{rec}	recovery time	n \overline{SD} , n \overline{RD} ; see Fig. 12								
		V _{CC} = 2 V	7	-	-	7	-	7	-	ns
		V _{CC} = 4.5 V	5	-	-	5	-	5	-	ns
		V _{CC} = 6 V	5	-	-	5	-	5	-	ns
		V _{CC} = 3.0 V to 3.6 V	6	-	-	6	-	6	-	ns
		V _{CC} = 4.5 V to 5.5 V	5	-	-	5	-	5	-	ns

Dual D-type flip-flop with Schmitt-trigger inputs; set and reset; positive edge-trigger

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
t _{su}	set-up time	nD to nCP; see Fig. 11								
		V _{CC} = 2 V	19	-	-	22	-	24	-	ns
		V _{CC} = 4.5 V	8	-	-	9	-	9	-	ns
		V _{CC} = 6 V	5	-	-	6	-	6	-	ns
		V _{CC} = 3.0 V to 3.6 V	11	-	-	13	-	14	-	ns
		V _{CC} = 4.5 V to 5.5 V	8	-	-	9	-	9	-	ns
t _h	hold time	nD to nCP; see Fig. 11								
		V _{CC} = 2 V	0	-	-	0	-	0	-	ns
		V _{CC} = 4.5 V	0	-	-	0	-	0	-	ns
		V _{CC} = 6 V	0	-	-	0	-	0	-	ns
		V _{CC} = 3.0 V to 3.6 V	0	-	-	0	-	0	-	ns
		V _{CC} = 4.5 V to 5.5 V	0	-	-	0	-	0	-	ns
f _{max}	maximum frequency	nCP; see Fig. 11								
		V _{CC} = 2 V	-	31	-	20	-	18	-	MHz
		V _{CC} = 4.5 V	-	95	-	50	-	45	-	MHz
		V _{CC} = 6 V	-	105	-	72	-	65	-	MHz
		V _{CC} = 3.0 V to 3.6 V	-	81	-	37	-	30	-	MHz
		V _{CC} = 4.5 V to 5.5 V	-	100	-	50	-	45	-	MHz
t _t	transition time	nQ, nQ̄; see Fig. 11 [3]								
		V _{CC} = 2 V	-	9	13	-	15	-	16	ns
		V _{CC} = 4.5 V	-	5	7	-	8	-	8	ns
		V _{CC} = 6 V	-	4	6	-	7	-	7	ns
		V _{CC} = 3.0 V to 3.6 V	-	5	8	-	9	-	10	ns
		V _{CC} = 4.5 V to 5.5 V	-	4	7	-	8	-	8	ns
C _I	input capacitance		-	1.5	-	-	5	-	5	pF
C _{PD}	power dissipation capacitance	f _i = 1 MHz; C _L = 0 pF; V _I = GND to V _{CC} ; V _{CC} = 2.0 V to 6.0 V [4]	-	10	-	-	-	-	-	pF

[1] Typical values are measured at nominal supply voltage.
[2] t_{pd} is the same as t_{PHL} and t_{PLH}.
[3] t_t is the same as t_{THL} and t_{TLH}.
[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
P_D = C_{PD} × V_{CC}² × f_i + Σ(C_L × V_{CC}² × f_o) where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
Σ(C_L × V_{CC}² × f_o) = sum of outputs;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V.

10.1. Waveforms and test circuit



Measurement points are given in [Table 9](#).
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 11. Propagation delay input (nCP) to output (nQ, nQ̄), output transition time, clock input (nCP) pulse width, set-up and hold and the maximum frequency (nCP)

Dual D-type flip-flop with Schmitt-trigger inputs; set and reset; positive edge-trigger

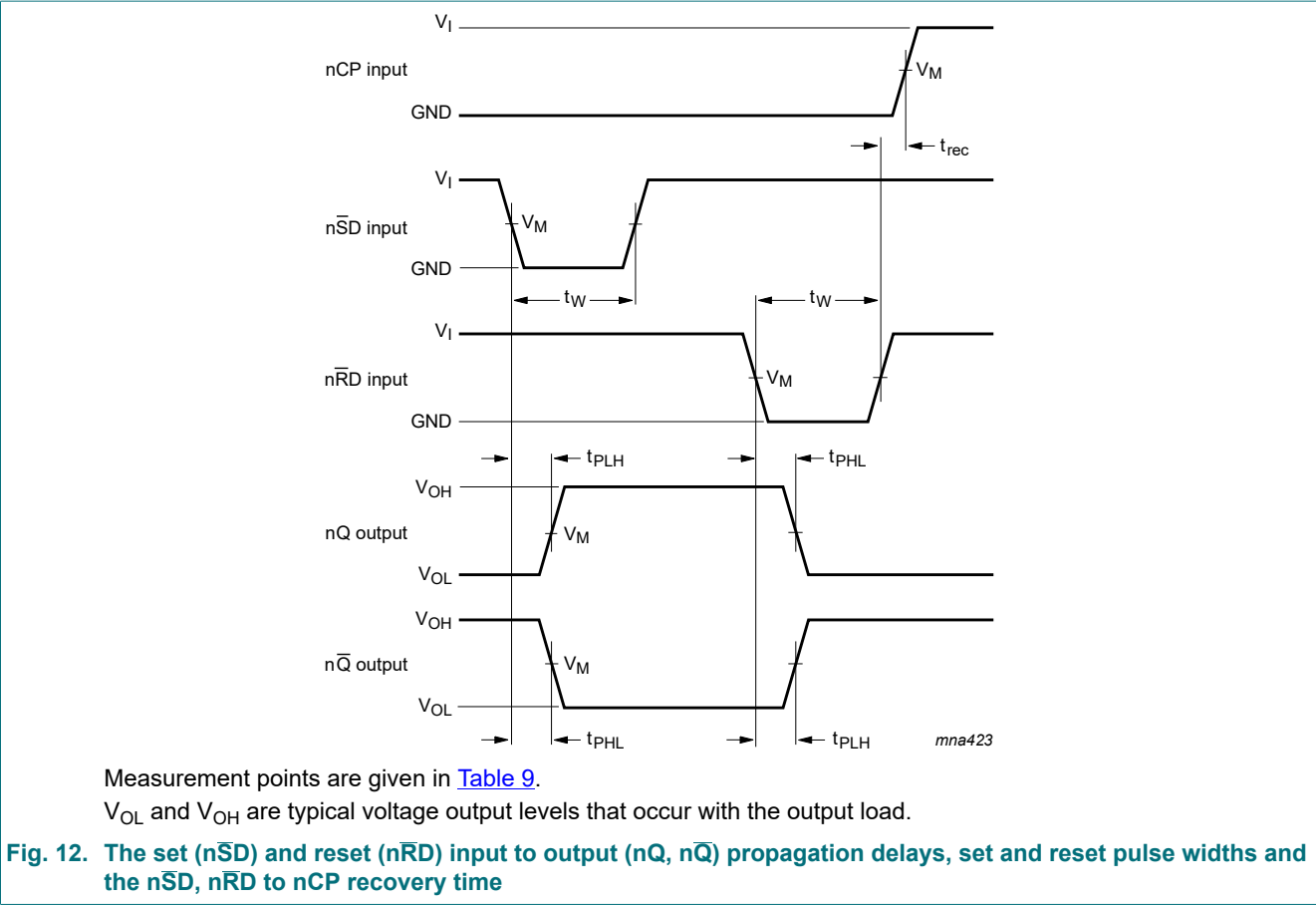


Table 9. Measurement points

Input	Output
V _M	V _M
0.5V _{CC}	0.5V _{CC}

Dual D-type flip-flop with Schmitt-trigger inputs; set and reset; positive edge-trigger

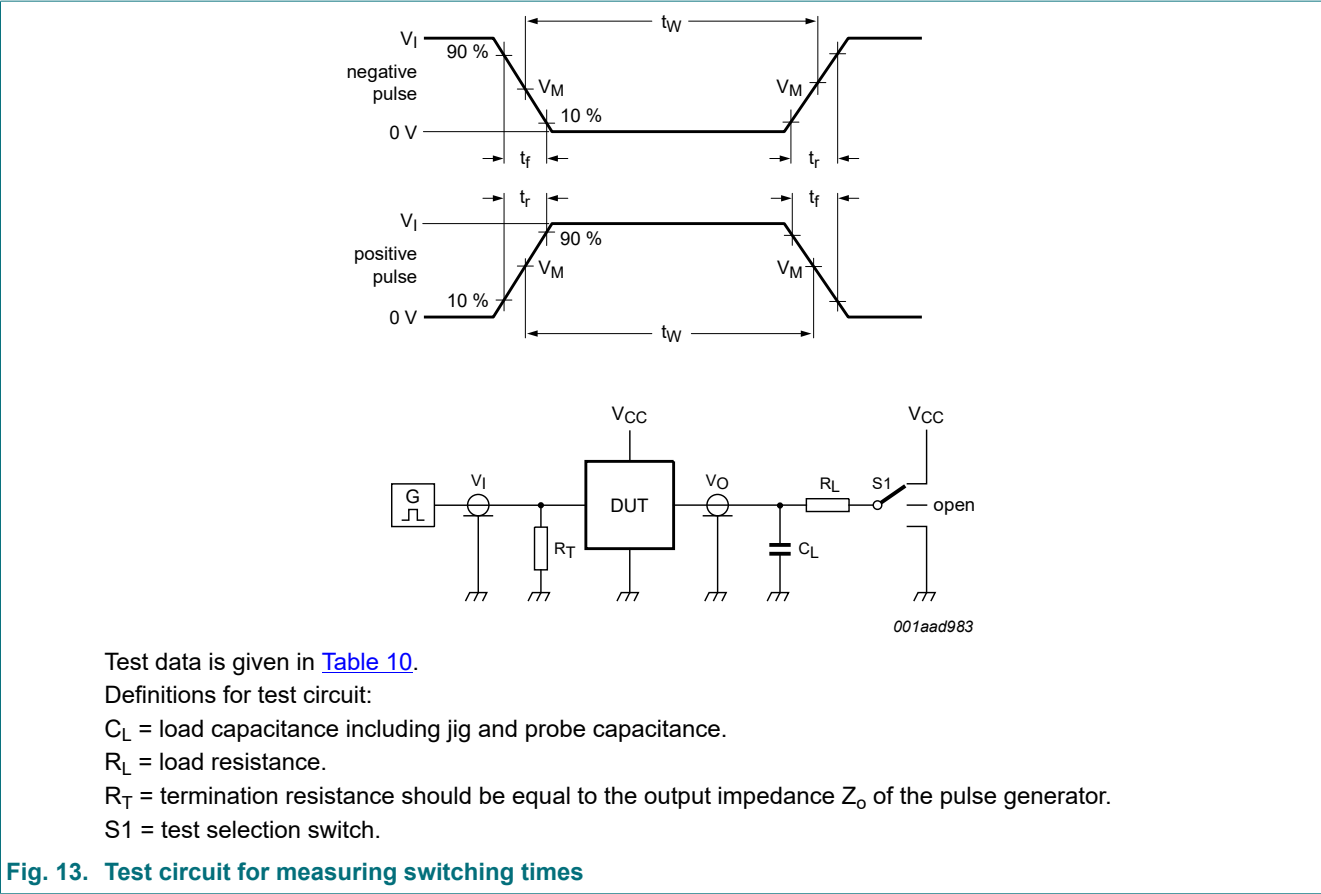


Fig. 13. Test circuit for measuring switching times

Table 10. Test data

Input		Load		S1 position		
V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
V_{CC}	2.5 ns	50 pF	1 kΩ	open	GND	V_{CC}

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

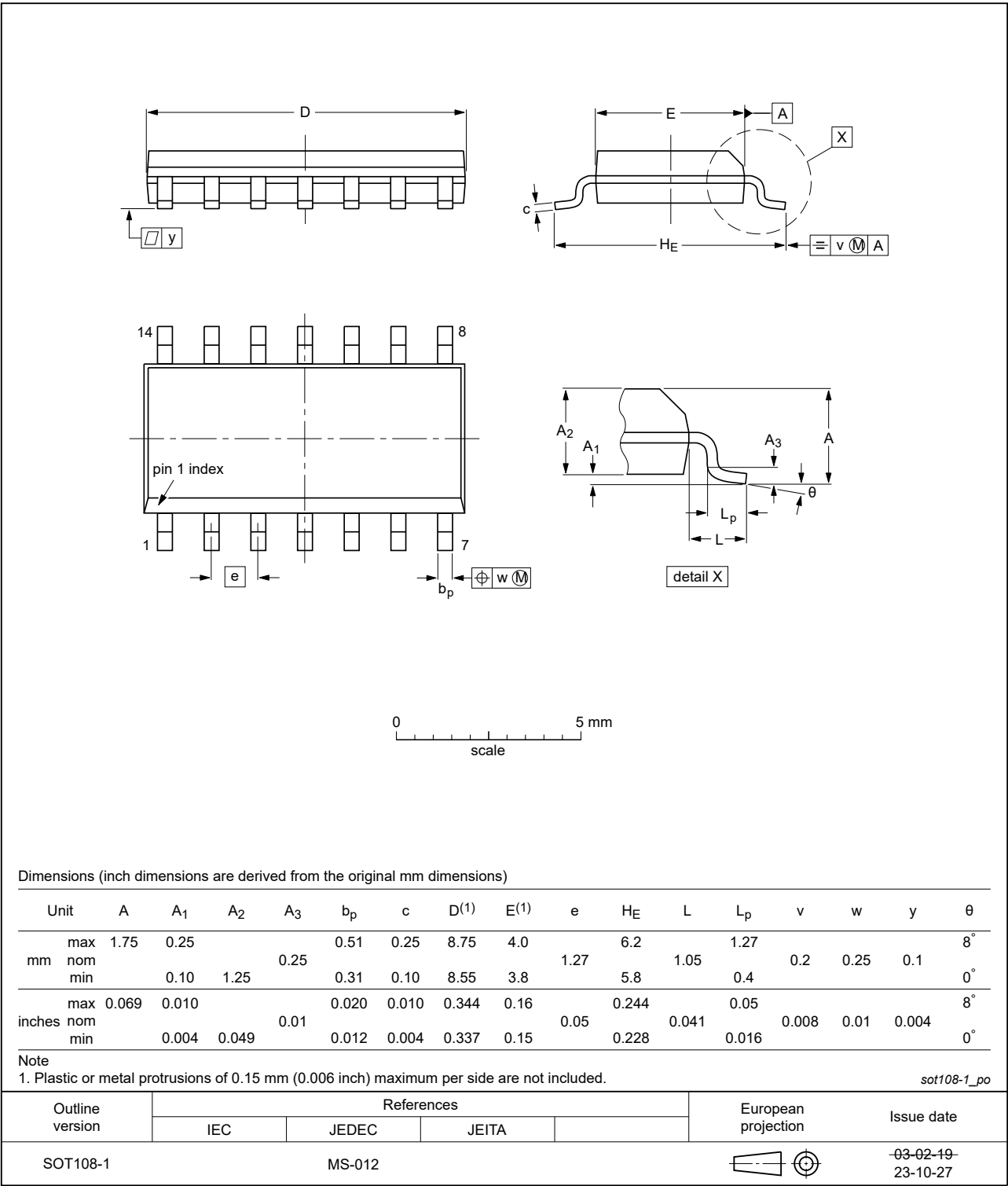


Fig. 14. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

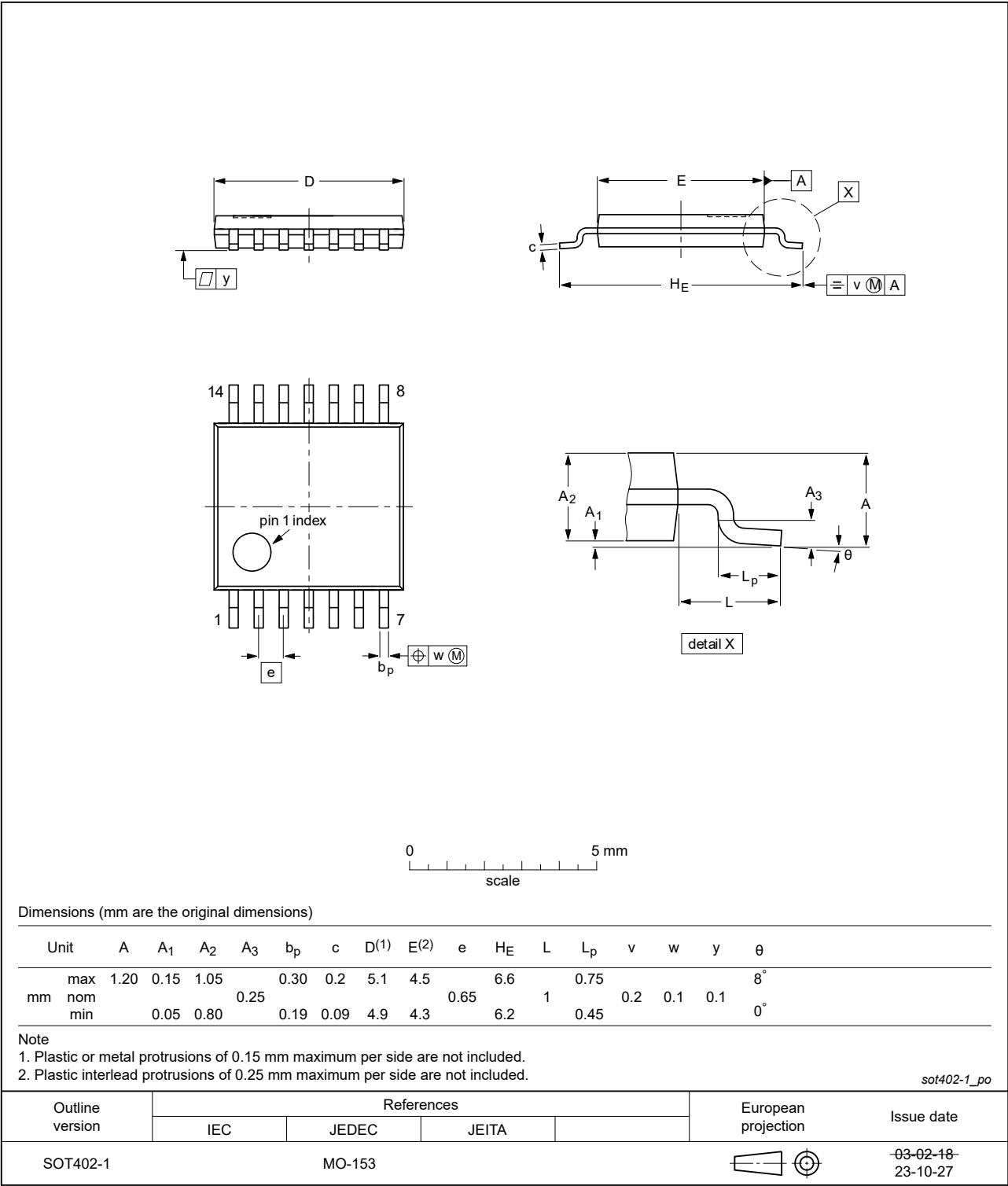


Fig. 15. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;
14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

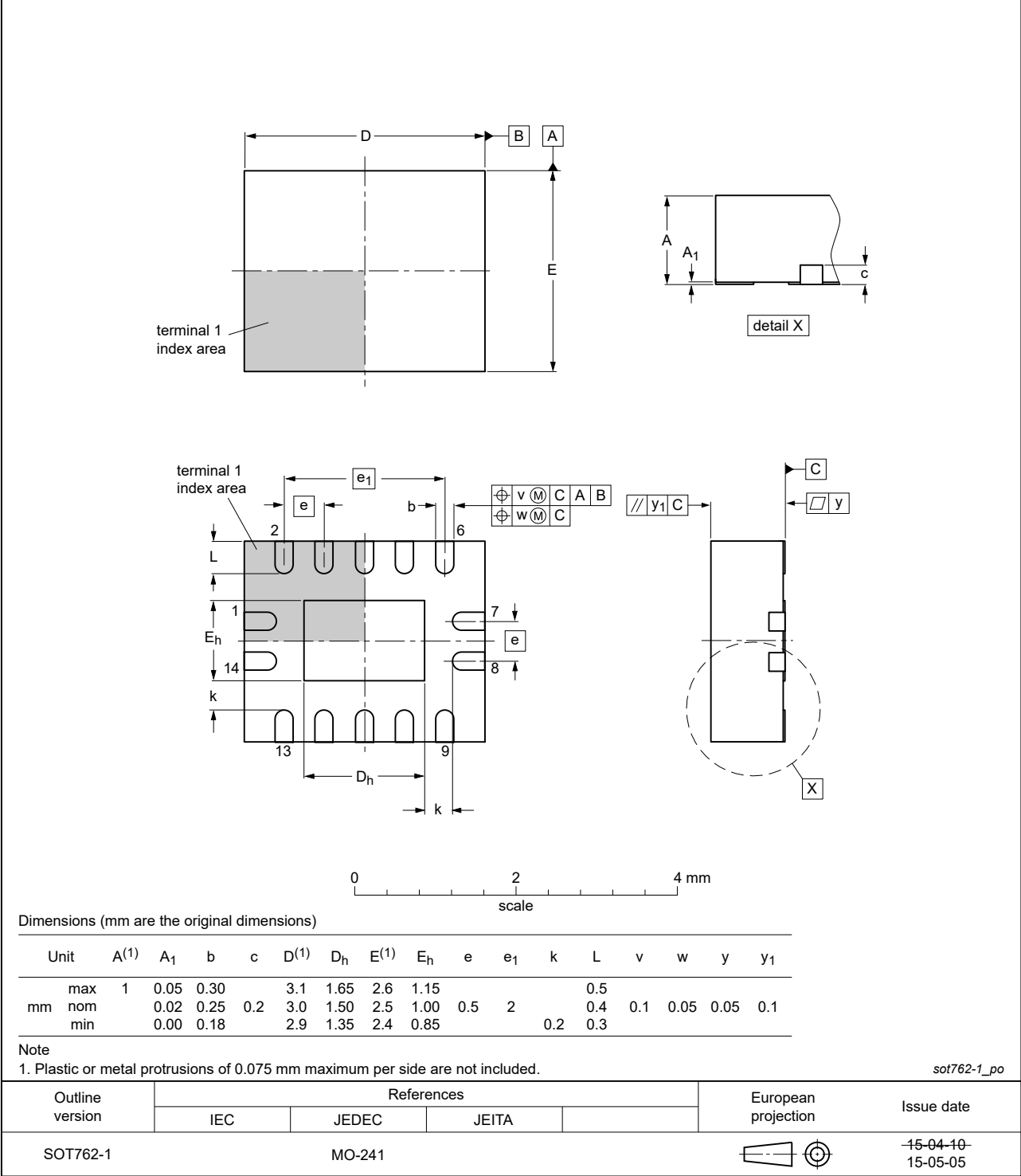


Fig. 16. Package outline SOT762-1 (DHVQFN14)

12. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charge Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

13. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HCS74 v.1	20250627	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 27 June 2025