



74HCS264

8-bit serial-in, parallel-out shift register with Schmitt-trigger inputs and inverting outputs

Rev. 1 — 5 June 2025

Product data sheet

1. General description

The 74HCS264 is an 8-bit serial-in/parallel-out shift register. The device features two serial data inputs (DSA and DSB), eight parallel inverting data outputs ($\overline{Q0}$ to $\overline{Q7}$). Data is entered serially through DSA or DSB and either input can be used as an active HIGH enable for data entry through the other input. Data is shifted on the LOW-to-HIGH transitions of the clock (CP) input. A LOW on the master reset input (\overline{MR}) clears the register and forces all outputs HIGH, independently of other inputs. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

All inputs are Schmitt-trigger inputs, capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- Schmitt-trigger inputs
- Low power consumption
 - Typical supply current (I_{CC}) of 100 nA
 - Typical input leakage current (I_I) of ± 10 nA
- ± 7.8 mA output drive at 6 V
- 8-bit serial input and 8-bit serial or parallel output
- Storage register with 3-state outputs
- Shift register with direct clear
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
 - JESD7A (2.0 V to 6.0 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 3A exceeds 4000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1500 V
- Multiple package options
- Specified from -40 °C to $+85$ °C and from -40 °C to $+125$ °C

3. Applications

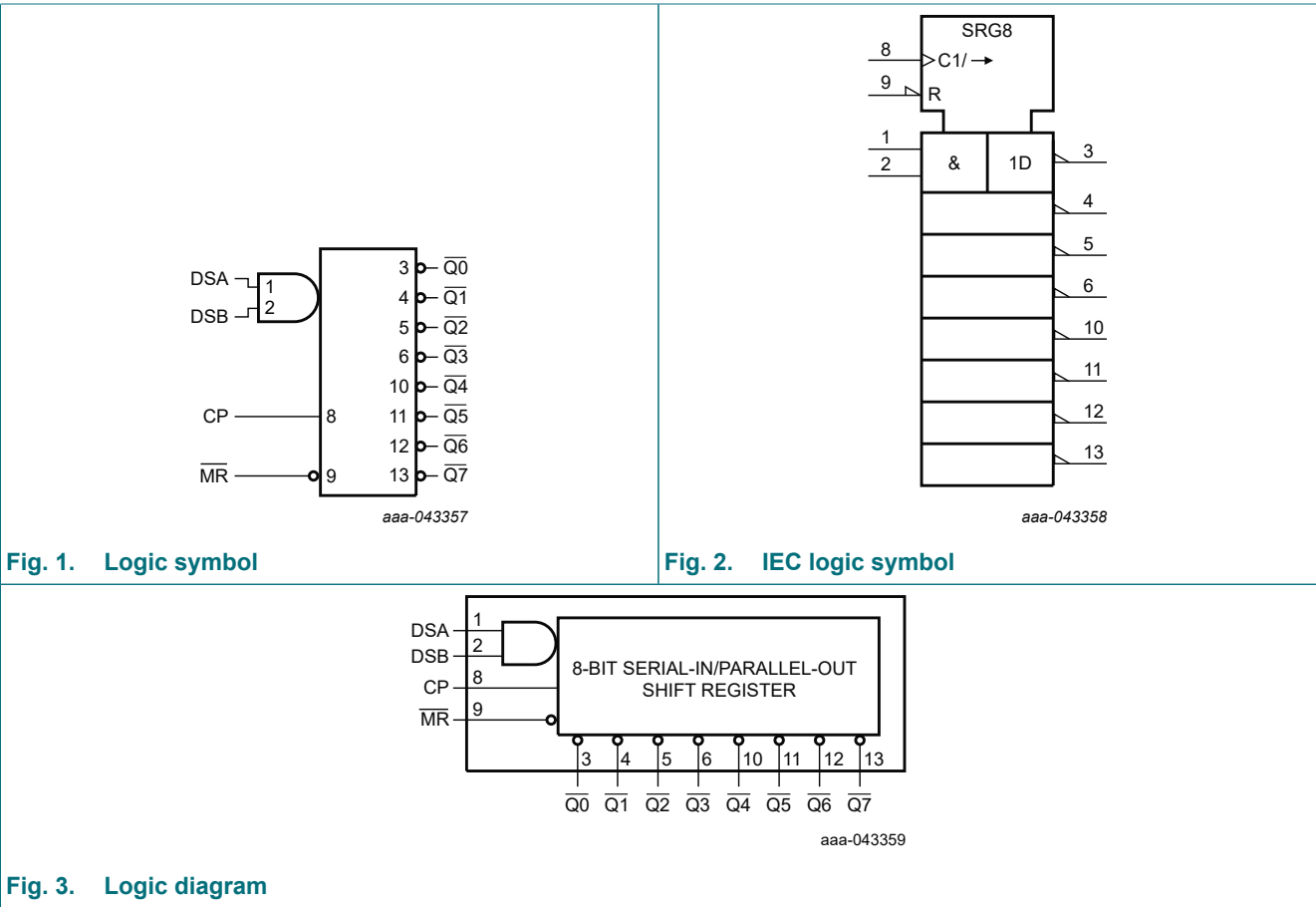
- Serial-to-parallel data conversion
- Remote control holding register
- Output expansion
- LED matrix control
- 7-segment display control
- 8-bit data storage

4. Ordering information

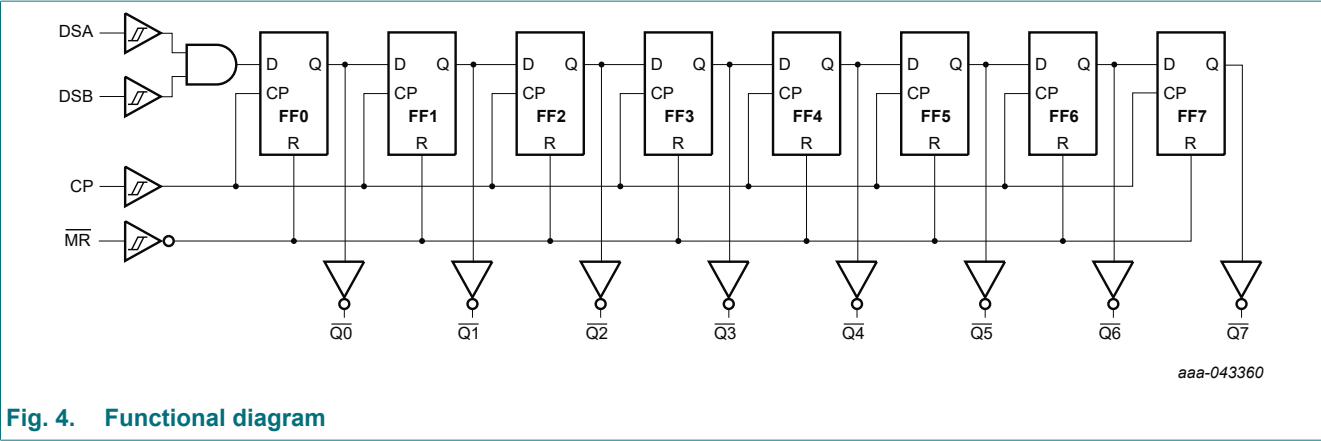
Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HCS264D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HCS264PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74HCS264BQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

5. Functional diagram

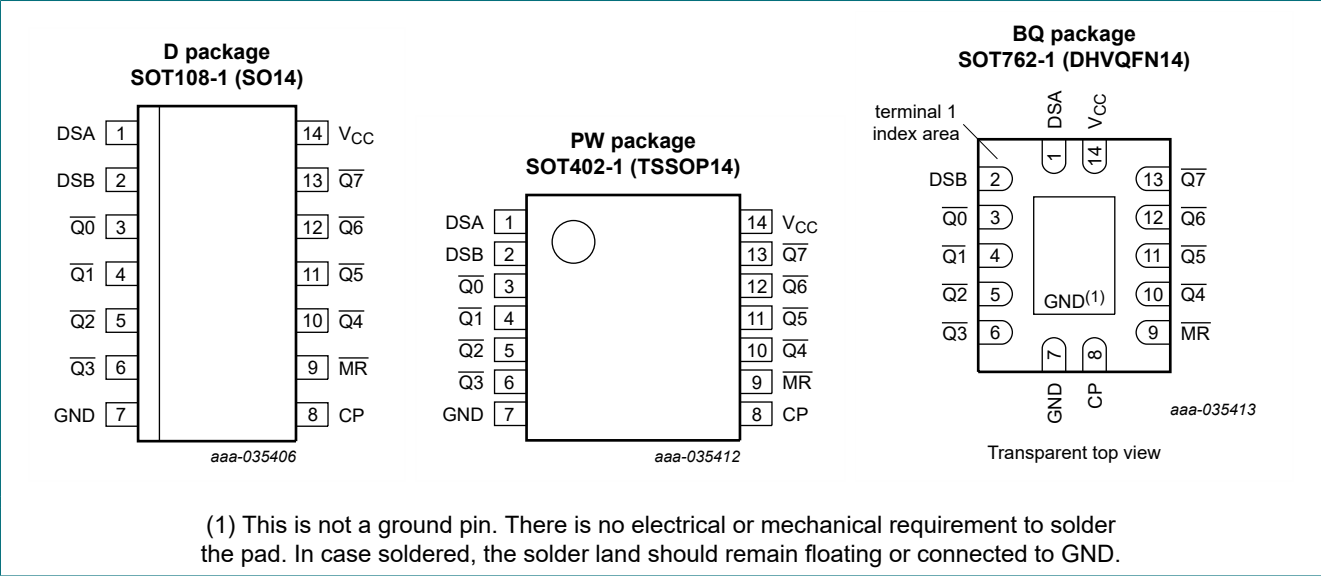


8-bit serial-in, parallel-out shift register with Schmitt-trigger inputs and inverting outputs



6. Pinning information

6.1. Pinning



6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
DSA	1	serial data input A
DSB	2	serial data input B
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	3, 4, 5, 6, 10, 11, 12, 13	parallel output (inverting)
GND	7	ground (0 V)
CP	8	clock input (LOW-to-HIGH, edge-triggered)
MR	9	master reset input (active LOW)
V _{CC}	14	positive supply voltage

7. Functional description

Table 3. Function table

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
L = LOW voltage level; l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
q = lower case letters indicate the state of the referenced input one set-up time prior to the LOW-to-HIGH clock transition
↑ = LOW-to-HIGH clock transition; X = don't care

Operating modes	Input				Output	
	MR	CP	DSA	DSB	Q0	Q1 to Q7
Reset (clear)	L	X	X	X	H	H to H
Shift	H	↑	l	l	H	q0 to q6
	H	↑	l	h	H	q0 to q6
	H	↑	h	l	H	q0 to q6
	H	↑	h	h	L	q0 to q6

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V [1]	-	±20	mA
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V [1]	-	±20	mA
I _O	output current	V _O = 0 V to V _{CC}	-	±35	mA
I _{CC}	supply current		-	70	mA
I _{GND}	ground current		-70	-	mA
T _j	junction temperature	[2]	-	+150	°C
T _{stg}	storage temperature		-65	+150	°C
V _{ESD}	electrostatic discharge	HBM: ANSI/ESDA/JEDEC JS-001 class 3A exceeds 4000 V	-	±4000	V
		CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1500 V	-	±1500	V
P _{tot}	total power dissipation	[3]	-	500	mW

- [1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] Guaranteed by design.
[3] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.
For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.
For SOT762-1 (DHVQFN14) package: P_{tot} derates linearly with 9.6 mW/K above 98 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		2.0	5.0	6.0	V
V _I	input voltage		0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	°C

10. Static characteristics

Table 6. Static characteristics

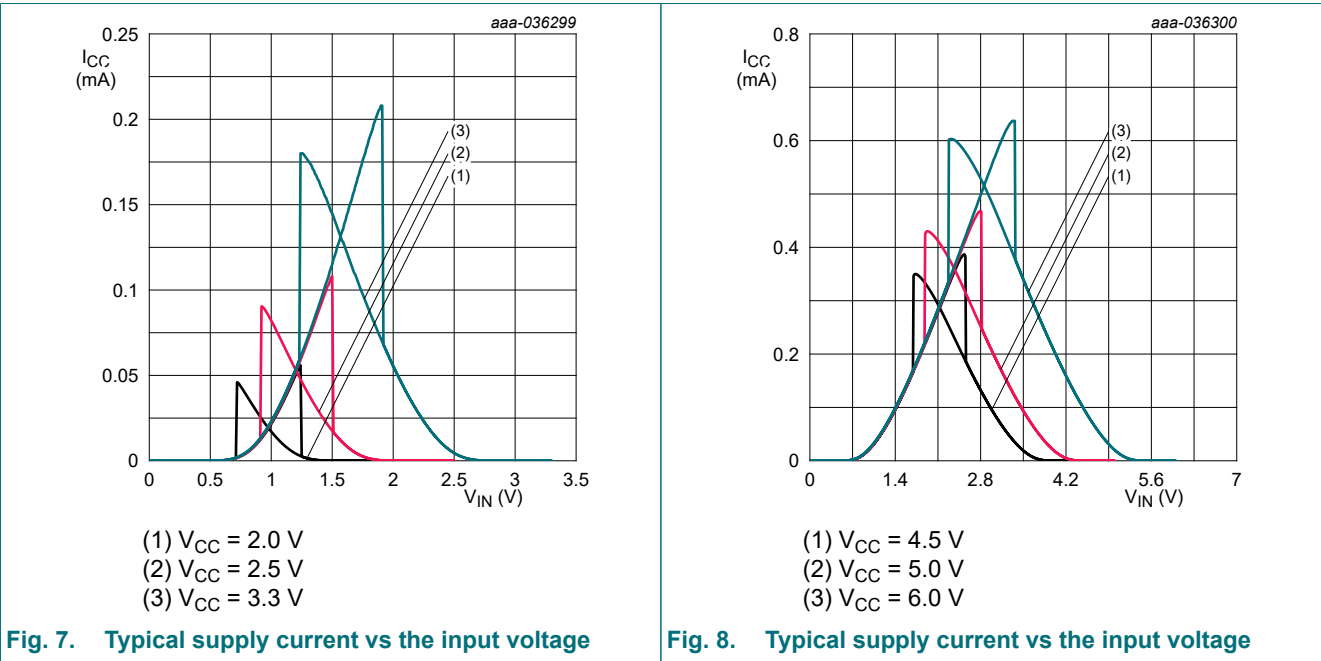
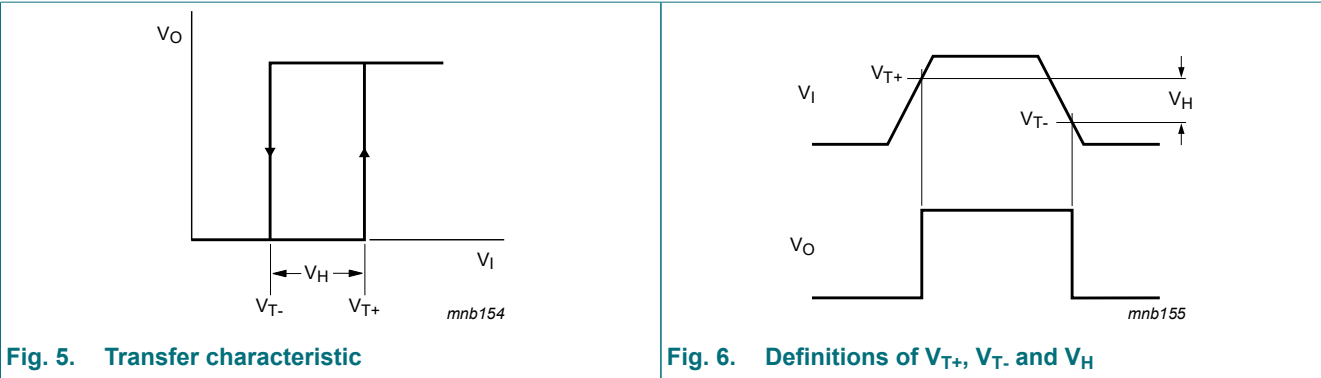
At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V _{T+}	positive-going threshold voltage	see Fig. 5 and Fig. 6								
		V _{CC} = 2.0 V	0.7	-	1.5	0.7	1.5	0.7	1.5	V
		V _{CC} = 4.5 V	1.7	-	3.15	1.7	3.15	1.7	3.15	V
		V _{CC} = 6 V	2.1	-	4.2	2.1	4.2	2.1	4.2	V
		V _{CC} = 3.0 V to 3.6 V	0.4V _{CC}	-	0.7V _{CC}	0.4V _{CC}	0.7V _{CC}	0.4V _{CC}	0.7V _{CC}	V
		V _{CC} = 4.5 V to 5.5 V	0.38V _{CC}	-	0.7V _{CC}	0.38V _{CC}	0.7V _{CC}	0.38V _{CC}	0.7V _{CC}	V
V _{T-}	negative-going threshold voltage	see Fig. 5 and Fig. 6								
		V _{CC} = 2.0 V	0.3	-	1.0	0.3	1.0	0.3	1.0	V
		V _{CC} = 4.5 V	0.9	-	2.2	0.9	2.2	0.9	2.2	V
		V _{CC} = 6 V	1.2	-	3.0	1.2	3.0	1.2	3.0	V
		V _{CC} = 3.0 V to 3.6 V	0.2V _{CC}	-	0.5V _{CC}	0.2V _{CC}	0.5V _{CC}	0.2V _{CC}	0.5V _{CC}	V
		V _{CC} = 4.5 V to 5.5 V	0.2V _{CC}	-	0.49V _{CC}	0.2V _{CC}	0.49V _{CC}	0.2V _{CC}	0.49V _{CC}	V
V _H	hysteresis voltage[1]	see Fig. 5 and Fig. 6								
		V _{CC} = 2.0 V	0.2	0.52	1.0	0.2	1.0	0.2	1.0	V
		V _{CC} = 4.5 V	0.4	0.85	1.4	0.4	1.4	0.4	1.4	V
		V _{CC} = 6 V	0.6	1.1	1.6	0.6	1.6	0.6	1.6	V
		V _{CC} = 3.0 V to 3.6 V	0.1V _{CC}	0.72	0.38V _{CC}	0.1V _{CC}	0.38V _{CC}	0.1V _{CC}	0.38V _{CC}	V
		V _{CC} = 4.5 V to 5.5 V	0.09V _{CC}	0.94	0.29V _{CC}	0.09V _{CC}	0.29V _{CC}	0.09V _{CC}	0.29V _{CC}	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _{OH} = -20 µA; V _{CC} = 2.0 V to 6 V	V _{CC} -0.1	V _{CC} -0.002	-	V _{CC} -0.1	-	V _{CC} -0.1	-	V
		I _{OH} = -4 mA; V _{CC} = 3.0 V	2.7	2.85	-	2.7	-	2.7	-	V
		I _{OH} = -6 mA; V _{CC} = 4.5 V	4.0	4.3	-	4.0	-	4.0	-	V
		I _{OH} = -7.8 mA; V _{CC} = 6.0 V	5.48	5.75	-	5.4	-	5.4	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _{OL} = 20 µA; V _{CC} = 2.0 V to 6 V	-	0.002	0.1	-	0.1	-	0.1	V
		I _{OL} = 4 mA; V _{CC} = 3.0 V	-	0.14	0.25	-	0.25	-	0.25	V
		I _{OL} = 6 mA; V _{CC} = 4.5 V	-	0.18	0.26	-	0.30	-	0.30	V
		I _{OL} = 7.8 mA; V _{CC} = 6.0 V	-	0.22	0.26	-	0.33	-	0.33	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	±0.01	±0.1	-	±0.25	-	±1.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	0.1	-	-	0.5	-	2.0	µA

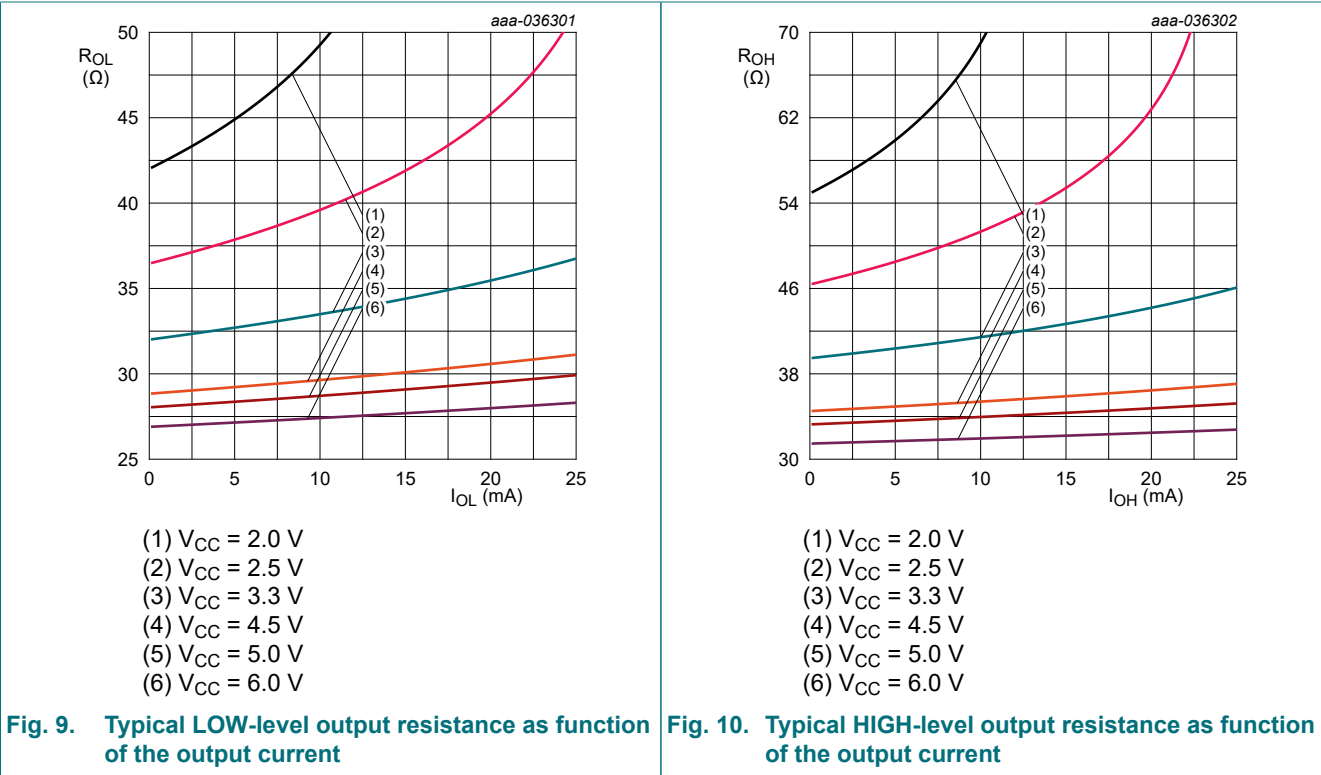
[1] Guaranteed by design.

10.1. Transfer characteristic waveforms and graphs

10.1.1. For inputs



10.1.2. For outputs



11. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see [Section 11.1](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
t_{pd}	propagation delay	CP to \overline{Qn} ; see Fig. 11 [2]								
		$V_{CC} = 2\text{ V}$	-	20	26	-	39	-	42	ns
		$V_{CC} = 4.5\text{ V}$	-	8	12	-	15	-	16	ns
		$V_{CC} = 6\text{ V}$	-	7	11	-	14	-	14	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	-	8	16	-	20	-	21	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	7	12	-	15	-	16	ns
t_{PLH}	LOW to HIGH propagation delay	MR to \overline{Qn} ; see Fig. 12								
		$V_{CC} = 2\text{ V}$	-	20	25	-	39	-	42	ns
		$V_{CC} = 4.5\text{ V}$	-	8	12	-	17	-	18	ns
		$V_{CC} = 6\text{ V}$	-	7	11	-	14	-	15	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	-	10	15	-	22	-	23	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	8	12	-	17	-	18	ns

8-bit serial-in, parallel-out shift register with Schmitt-trigger inputs and inverting outputs

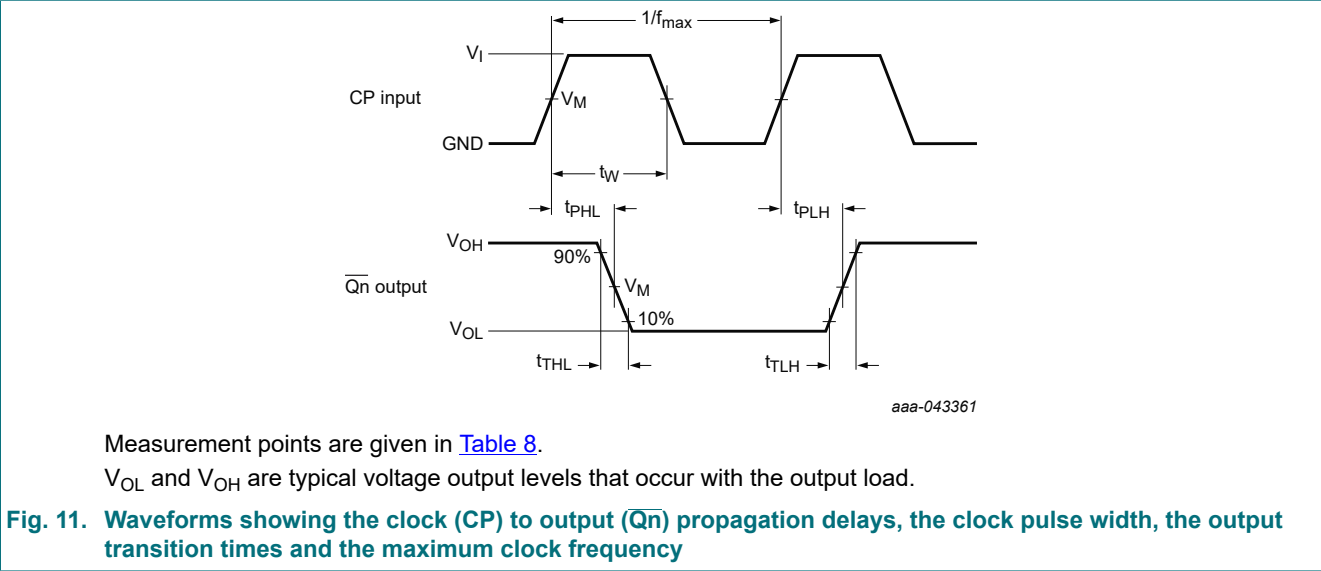
Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
t_t	transition time	\overline{Qn} , see Fig. 11 [3]								
		$V_{CC} = 2\text{ V}$	-	9	13	-	15	-	16	ns
		$V_{CC} = 4.5\text{ V}$	-	5	7	-	8	-	8	ns
		$V_{CC} = 6\text{ V}$	-	4	6	-	7	-	7	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	-	5	8	-	9	-	10	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	4	7	-	8	-	8	ns
t_W	pulse width	CP HIGH or LOW; see Fig. 11								
		$V_{CC} = 2\text{ V}$	8	-	-	11	-	12	-	ns
		$V_{CC} = 4.5\text{ V}$	6	-	-	7	-	7	-	ns
		$V_{CC} = 6\text{ V}$	6	-	-	7	-	7	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	7	-	-	9	-	9	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	6	-	-	7	-	7	-	ns
		MR LOW; see Fig. 12								
		$V_{CC} = 2\text{ V}$	7	-	-	11	-	12	-	ns
		$V_{CC} = 4.5\text{ V}$	6	-	-	7	-	7	-	ns
		$V_{CC} = 6\text{ V}$	6	-	-	7	-	7	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	7	-	-	8	-	9	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	6	-	-	7	-	7	-	ns
t_{rec}	recovery time	MR to CP; see Fig. 12								
		$V_{CC} = 2\text{ V}$	6	-	-	8	-	9	-	ns
		$V_{CC} = 4.5\text{ V}$	3	-	-	4	-	4	-	ns
		$V_{CC} = 6\text{ V}$	3	-	-	4	-	4	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	5	-	-	6	-	6	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	3	-	-	4	-	4	-	ns
t_{su}	set-up time	DSA, and DSB to CP; see Fig. 13								
		$V_{CC} = 2\text{ V}$	11	-	-	17	-	17	-	ns
		$V_{CC} = 4.5\text{ V}$	4	-	-	6	-	6	-	ns
		$V_{CC} = 6\text{ V}$	4	-	-	6	-	6	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	6	-	-	8	-	9	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	4	-	-	6	-	6	-	ns
t_h	hold time	DSA, and DSB to CP; see Fig. 13								
		$V_{CC} = 2\text{ V}$	0	-	-	0	-	0	-	ns
		$V_{CC} = 4.5\text{ V}$	0	-	-	0	-	0	-	ns
		$V_{CC} = 6\text{ V}$	0	-	-	0	-	0	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	0	-	-	0	-	0	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	0	-	-	0	-	0	-	ns

8-bit serial-in, parallel-out shift register with Schmitt-trigger inputs and inverting outputs

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
f _{max}	maximum frequency	CP, see Fig. 11								
		V _{CC} = 2 V	28	-	-	16	-	15	-	MHz
		V _{CC} = 4.5 V	68	-	-	55	-	50	-	MHz
		V _{CC} = 6 V	97	-	-	75	-	62	-	MHz
		V _{CC} = 3.0 V to 3.6 V	47	-	-	41	-	27	-	MHz
		V _{CC} = 4.5 V to 5.5 V	68	-	-	55	-	50	-	MHz
C _I	input capacitance		-	1.5	-	-	5	-	5	pF
C _{PD}	power dissipation capacitance	f _i = 1 MHz; C _L = 0 pF; V _I = GND to V _{CC} ; V _{CC} = 2 V to 6 V [4][5]	-	40	-	-	-	-	-	pF

- [1] Typical values are measured at nominal supply voltage.
- [2] t_{pd} is the same as t_{PHL} and t_{PLH}.
- [3] t_i is the same as t_{THL} and t_{TLH}.
- [4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V.
- [5] All 9 outputs switching.

11.1. Waveforms and test circuit



8-bit serial-in, parallel-out shift register with Schmitt-trigger inputs and inverting outputs

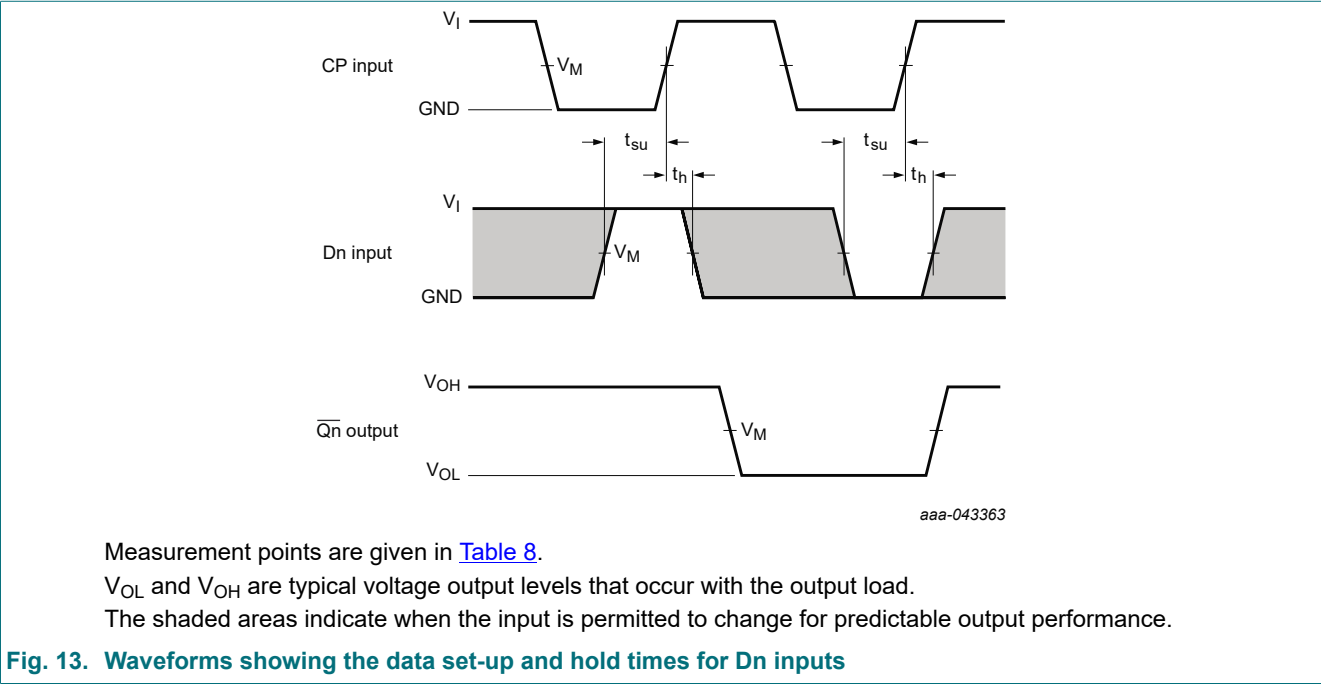
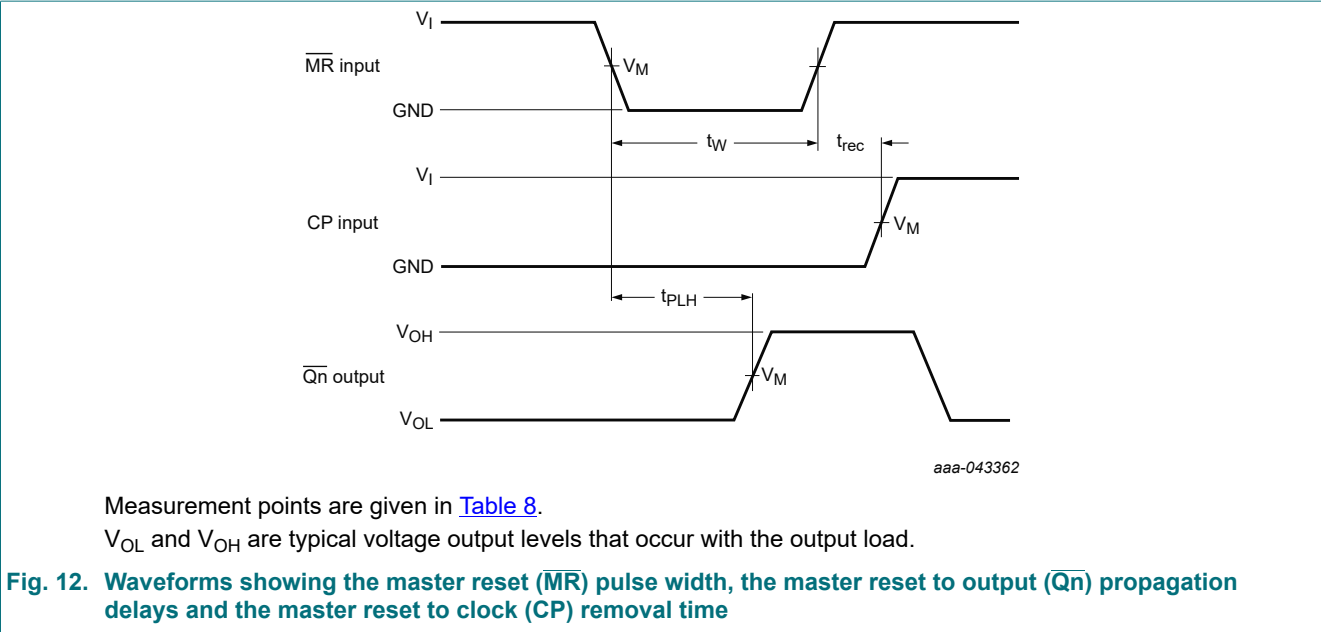


Table 8. Measurement points

Input	Output
V_M	V_M
$0.5V_{CC}$	$0.5V_{CC}$

8-bit serial-in, parallel-out shift register with Schmitt-trigger inputs and inverting outputs

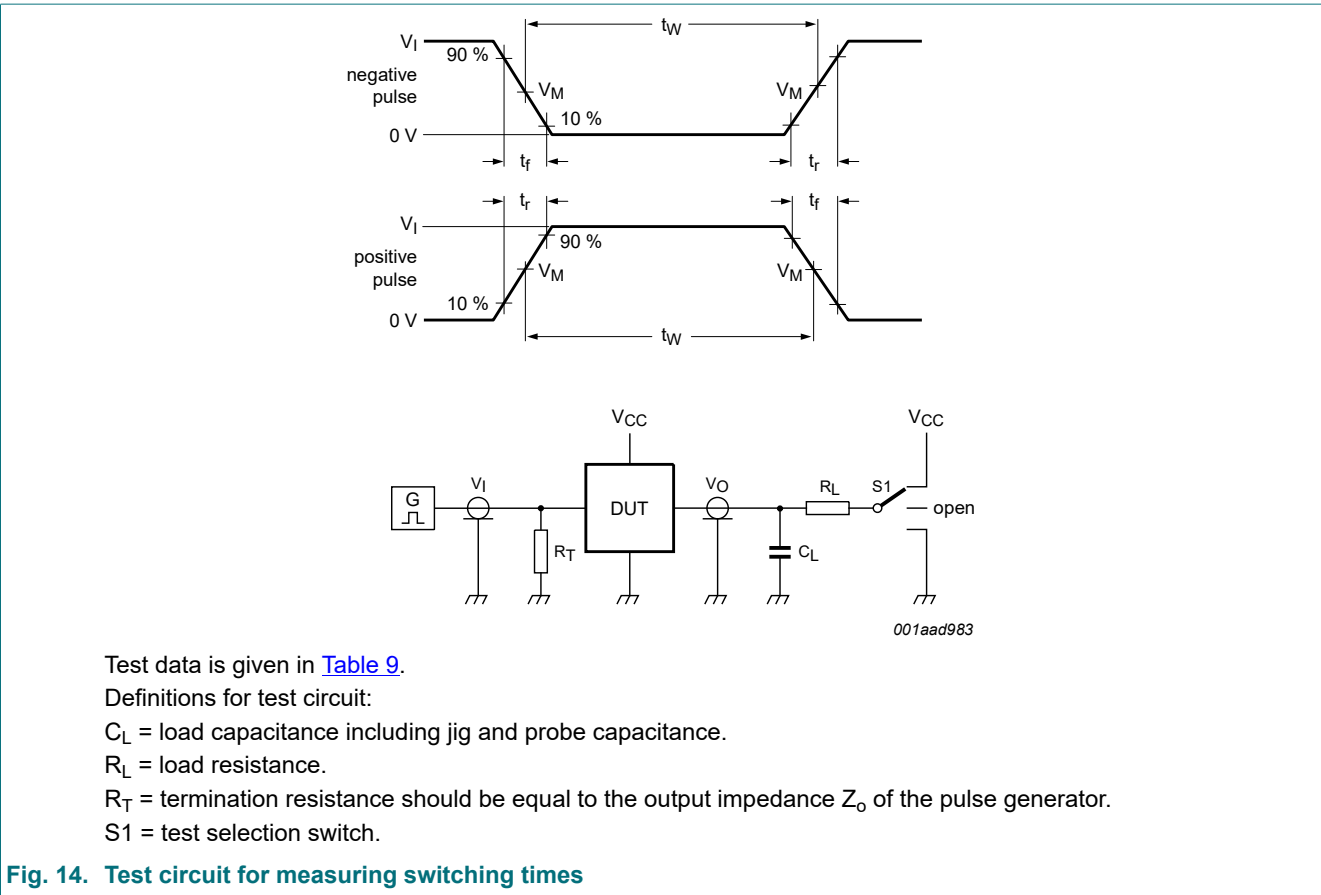


Table 9. Test data

Input		Load		S1 position		
V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
V_{CC}	2.5 ns	50 pF	1 kΩ	open	GND	V_{CC}

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

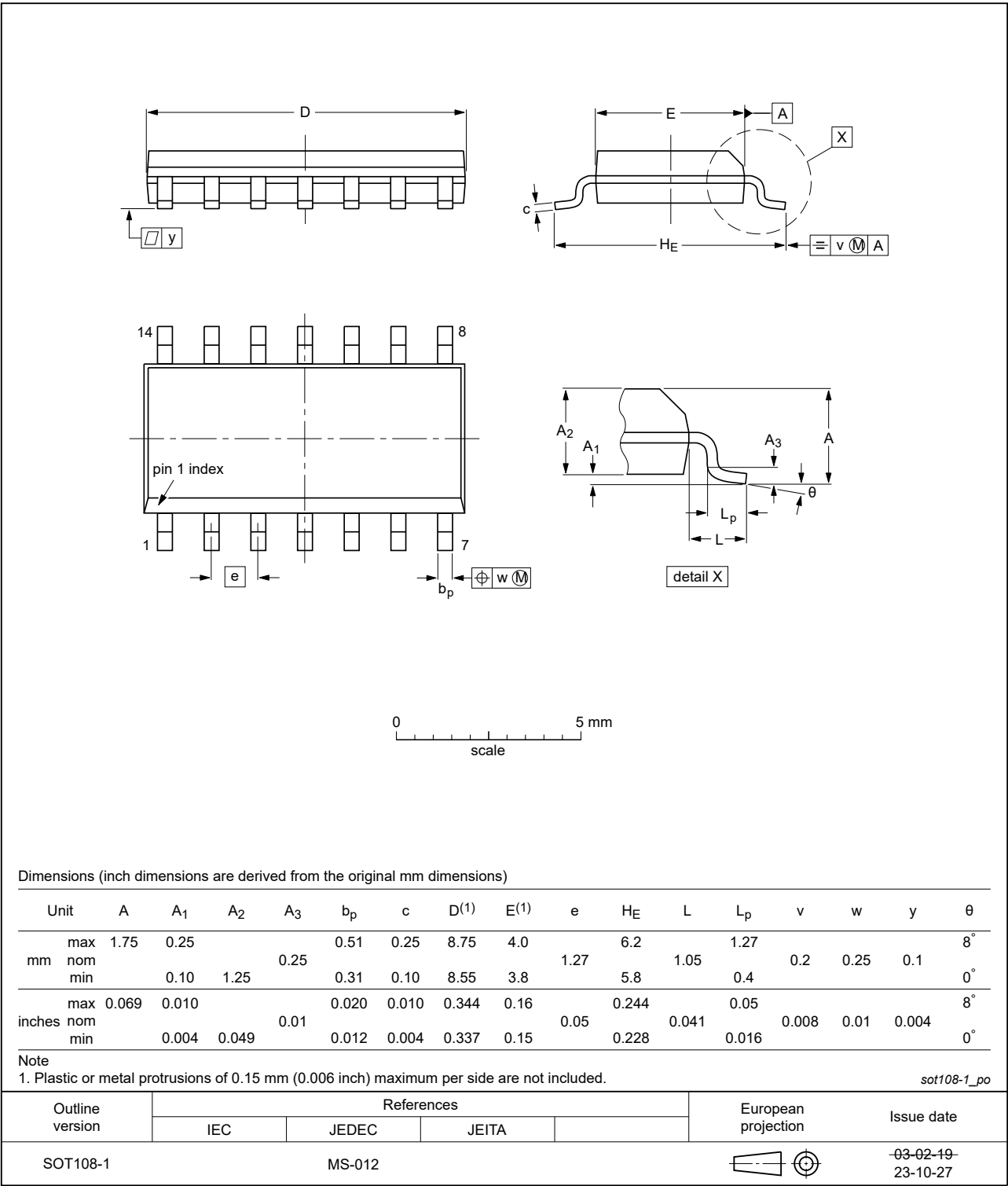


Fig. 15. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

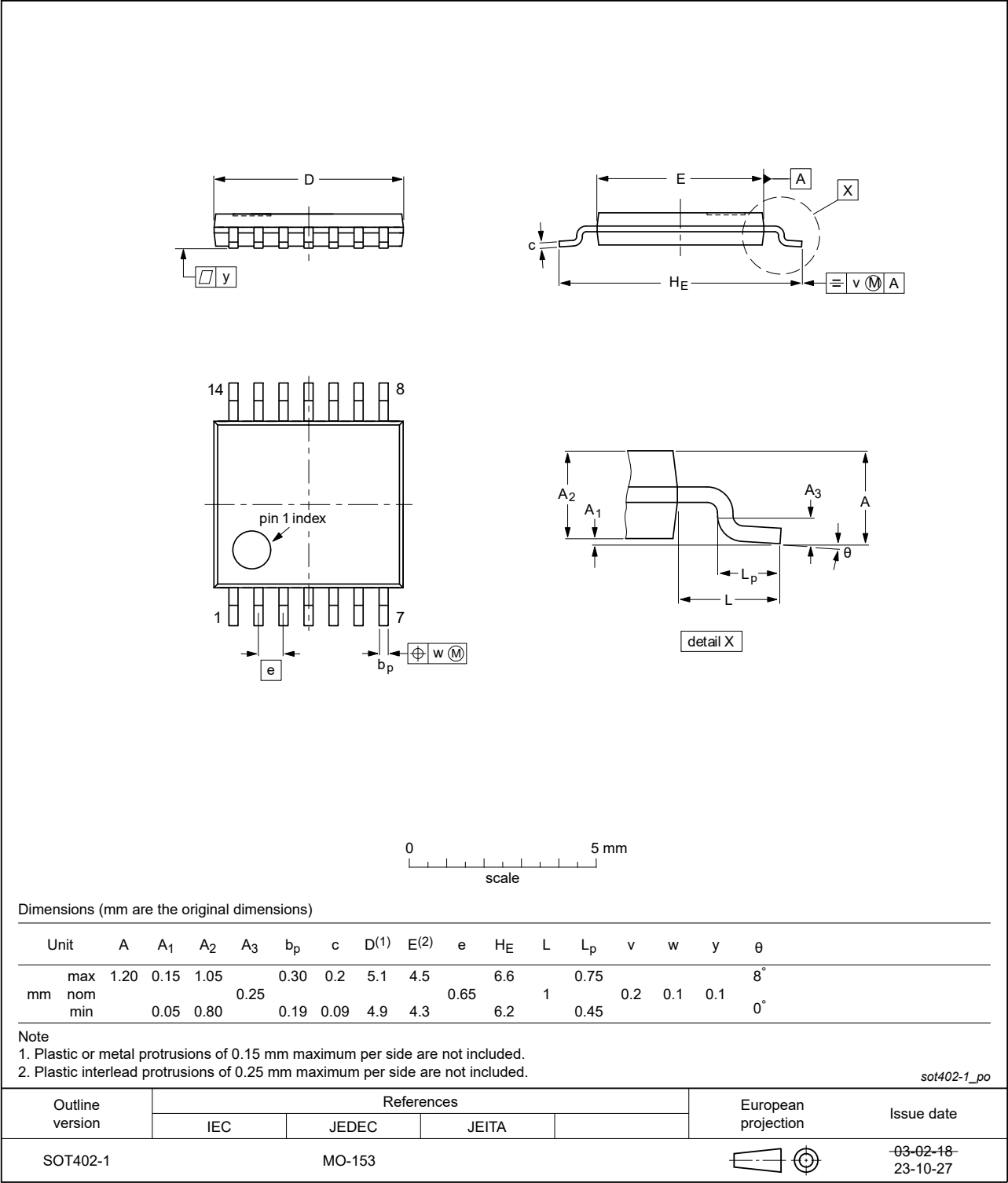


Fig. 16. Package outline SOT402-1 (TSSOP14)

8-bit serial-in, parallel-out shift register with Schmitt-trigger inputs and inverting outputs

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

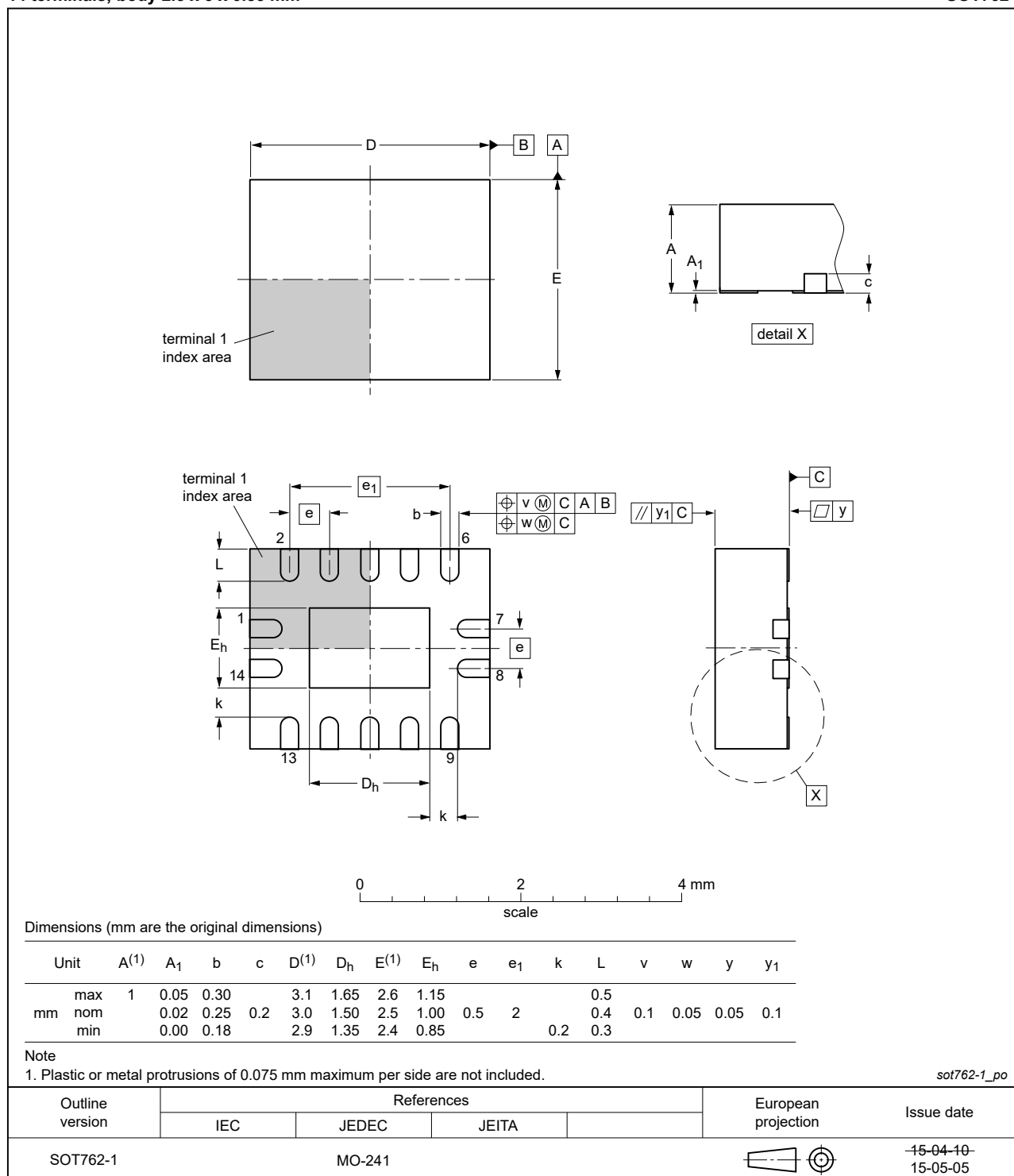


Fig. 17. Package outline SOT762-1 (DHVQFN14)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charge Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HCS264 v.1	20250605	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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