

74HCS03

Quad 2-input NAND gate with Schmitt-trigger inputs and open-drain output

Rev. 1 — 23 July 2025

Product data sheet

1. General description

The 74HCS03 is a quad 2-input NAND gate with open-drain outputs. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

All inputs are Schmitt-trigger inputs, capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

2. Features and benefits

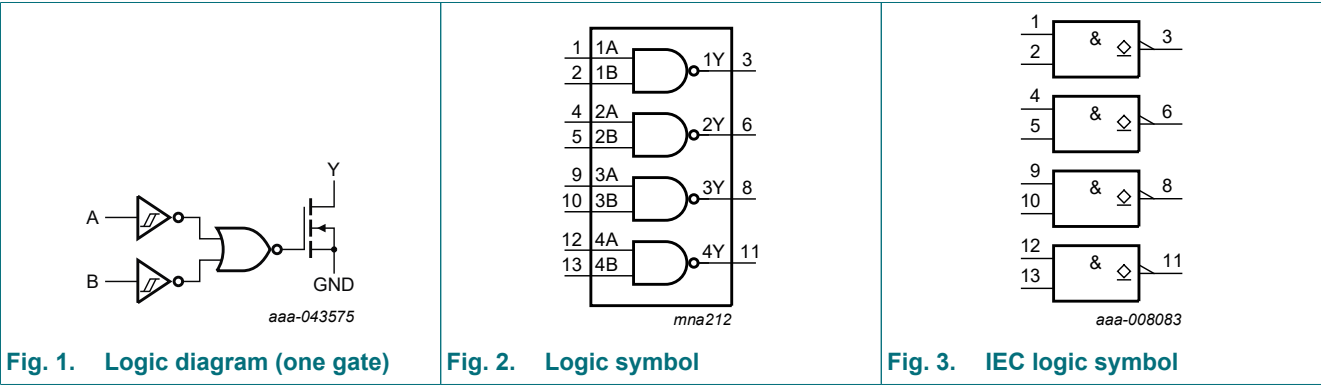
- Wide supply voltage range from 2.0 V to 6.0 V
- Schmitt-trigger inputs
- Low power consumption
 - Typical supply current (I_{CC}) of 100 nA
 - Typical input leakage current (I_I) of ± 10 nA
- ± 7.8 mA output drive at 6 V
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
 - JESD7A (2.0 V to 6.0 V)
- ESD protection:
 - HBM ANSI/ESDA/JEDEC JS-001 class 3A exceeds 4000 V
 - CDM ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1500 V
- Multiple package options
- Specified from -40 °C to $+85$ °C and from -40 °C to $+125$ °C

3. Ordering information

Table 1. Ordering information

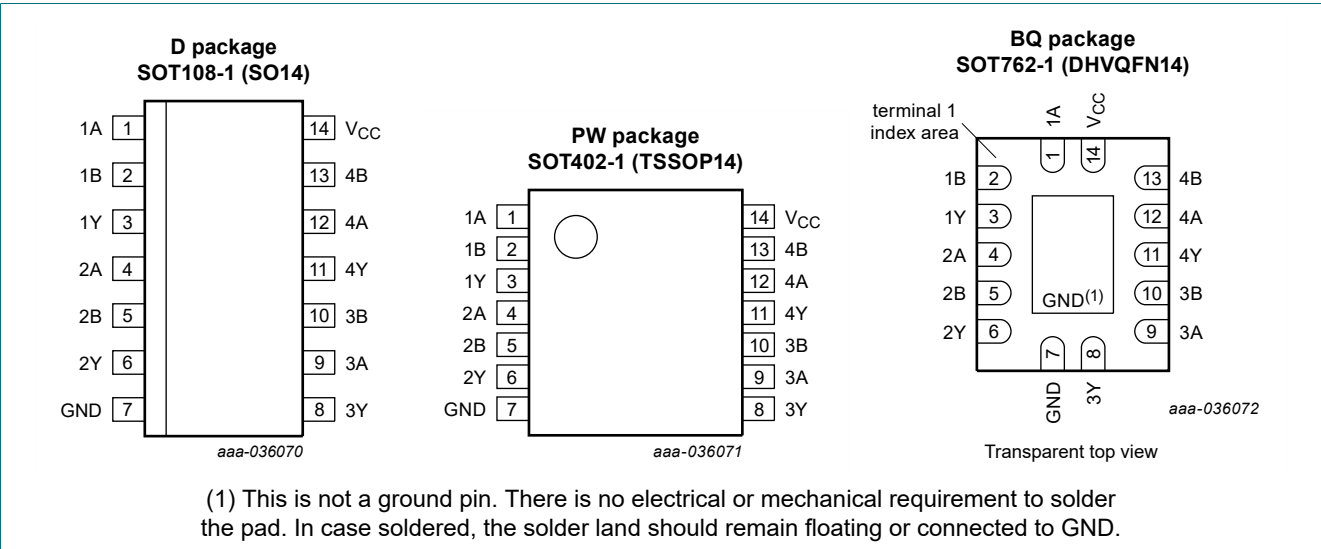
Type number	Package			
	Temperature range	Name	Description	Version
74HCS03D	-40 °C to $+125$ °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HCS03PW	-40 °C to $+125$ °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74HCS03BQ	-40 °C to $+125$ °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body $2.5 \times 3 \times 0.85$ mm	SOT762-1

4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A	1, 4, 9, 12	data input
1B, 2B, 3B, 4B	2, 5, 10, 13	data input
1Y, 2Y, 3Y, 4Y	3, 6, 8, 11	data output
GND	7	ground (0 V)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

Input		Output
nA	nB	nY
L	L	Z
L	H	Z
H	L	Z
H	H	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V [1]	-	±20	mA
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V [1]	-	±20	mA
I _O	output current	V _O = 0 V to V _{CC}	-	±35	mA
I _{CC}	supply current		-	70	mA
I _{GND}	ground current		-70	-	mA
T _j	junction temperature	[2]	-	+150	°C
T _{stg}	storage temperature		-65	+150	°C
V _{ESD}	electrostatic discharge	HBM ANSI/ESDA/JEDEC JS-001 class 3A exceeds 4000 V	-	±4000	V
		CDM ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1500 V	-	±1500	V
P _{tot}	total power dissipation	[3]	-	500	mW

- [1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] Guaranteed by design.
[3] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.
For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.
For SOT762-1 (DHVQFN14) package: P_{tot} derates linearly with 9.6 mW/K above 98 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		2.0	5.0	6.0	V
V _I	input voltage		0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	°C

9. Static characteristics

Table 6. Static characteristics

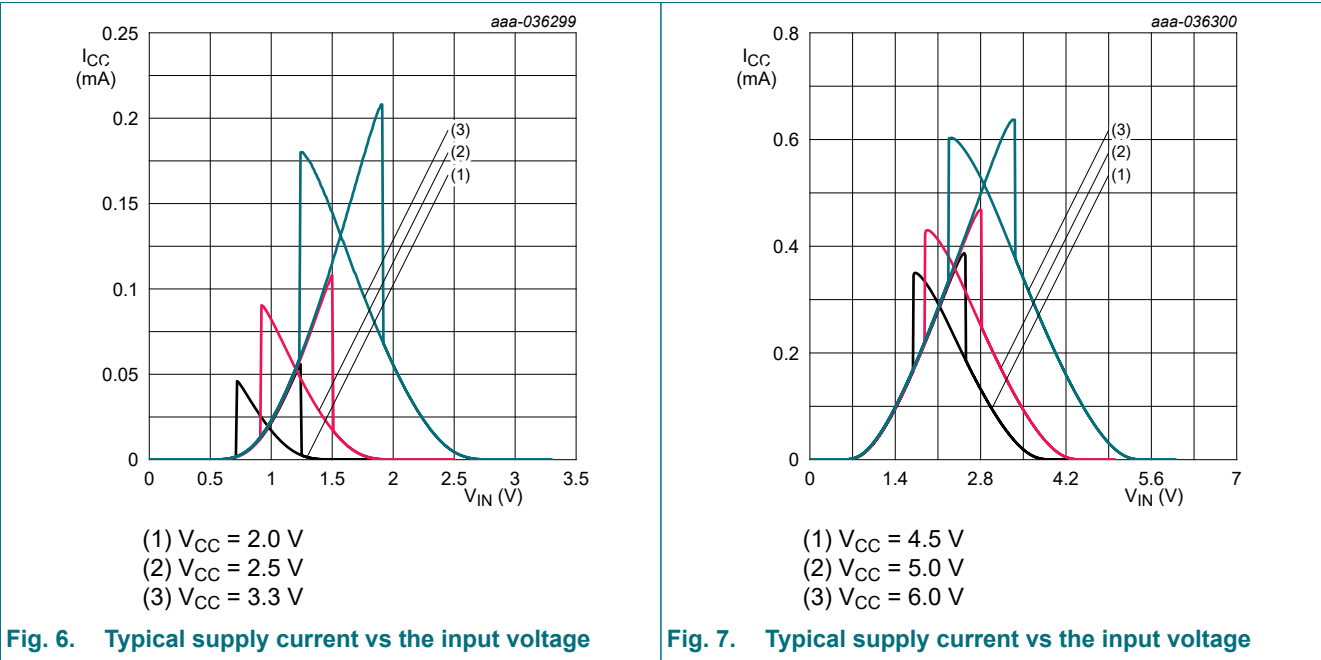
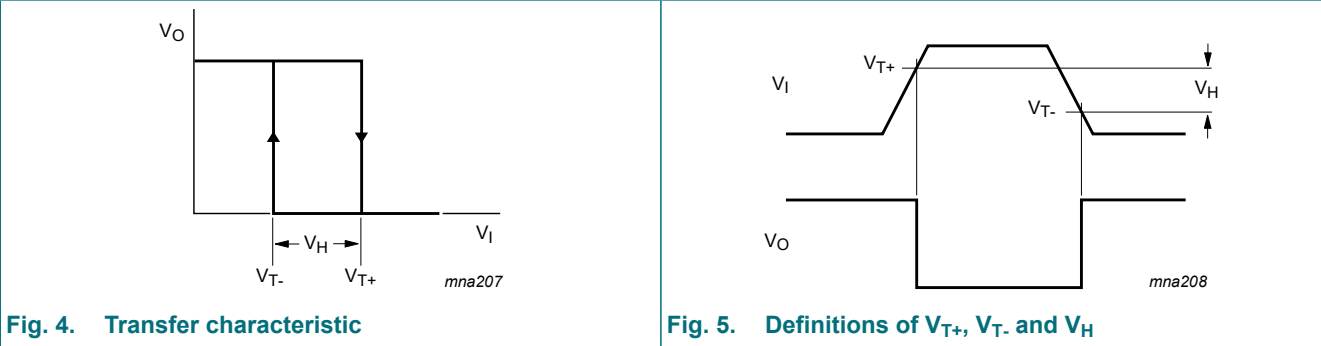
At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V _{T+}	positive-going threshold voltage	see Fig. 4 and Fig. 5								
		V _{CC} = 2.0 V	0.7	-	1.5	0.7	1.5	0.7	1.5	V
		V _{CC} = 4.5 V	1.7	-	3.15	1.7	3.15	1.7	3.15	V
		V _{CC} = 6 V	2.1	-	4.2	2.1	4.2	2.1	4.2	V
		V _{CC} = 3.0 V to 3.6 V	0.4V _{CC}	-	0.7V _{CC}	0.4V _{CC}	0.7V _{CC}	0.4V _{CC}	0.7V _{CC}	V
		V _{CC} = 4.5 V to 5.5 V	0.38V _{CC}	-	0.7V _{CC}	0.38V _{CC}	0.7V _{CC}	0.38V _{CC}	0.7V _{CC}	V
V _{T-}	negative-going threshold voltage	see Fig. 4 and Fig. 5								
		V _{CC} = 2.0 V	0.3	-	1.0	0.3	1.0	0.3	1.0	V
		V _{CC} = 4.5 V	0.9	-	2.2	0.9	2.2	0.9	2.2	V
		V _{CC} = 6 V	1.2	-	3.0	1.2	3.0	1.2	3.0	V
		V _{CC} = 3.0 V to 3.6 V	0.2V _{CC}	-	0.5V _{CC}	0.2V _{CC}	0.5V _{CC}	0.2V _{CC}	0.5V _{CC}	V
		V _{CC} = 4.5 V to 5.5 V	0.2V _{CC}	-	0.49V _{CC}	0.2V _{CC}	0.49V _{CC}	0.2V _{CC}	0.49V _{CC}	V
V _H	hysteresis voltage ^[1]	see Fig. 4 and Fig. 5								
		V _{CC} = 2.0 V	0.2	0.52	1.0	0.2	1.0	0.2	1.0	V
		V _{CC} = 4.5 V	0.4	0.85	1.4	0.4	1.4	0.4	1.4	V
		V _{CC} = 6 V	0.6	1.1	1.6	0.6	1.6	0.6	1.6	V
		V _{CC} = 3.0 V to 3.6 V	0.1V _{CC}	0.72	0.38V _{CC}	0.1V _{CC}	0.38V _{CC}	0.1V _{CC}	0.38V _{CC}	V
		V _{CC} = 4.5 V to 5.5 V	0.09V _{CC}	0.94	0.29V _{CC}	0.09V _{CC}	0.29V _{CC}	0.09V _{CC}	0.29V _{CC}	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _{OL} = 20 µA; V _{CC} = 2.0 V to 6 V	-	0.002	0.1	-	0.1	-	0.1	V
		I _{OL} = 4 mA; V _{CC} = 3.0 V	-	0.14	0.25	-	0.25	-	0.25	V
		I _{OL} = 6 mA; V _{CC} = 4.5 V	-	0.18	0.26	-	0.30	-	0.30	V
		I _{OL} = 7.8 mA; V _{CC} = 6.0 V	-	0.22	0.26	-	0.33	-	0.33	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	±0.01	±0.1	-	±0.25	-	±1.0	µA
I _{OZ}	OFF-state output current	V _{CC} = 6.0 V; V _O = V _{CC} or GND	-	±0.05	±0.25	-	±1.0	-	±2.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	0.1	-	-	0.5	-	2.0	µA

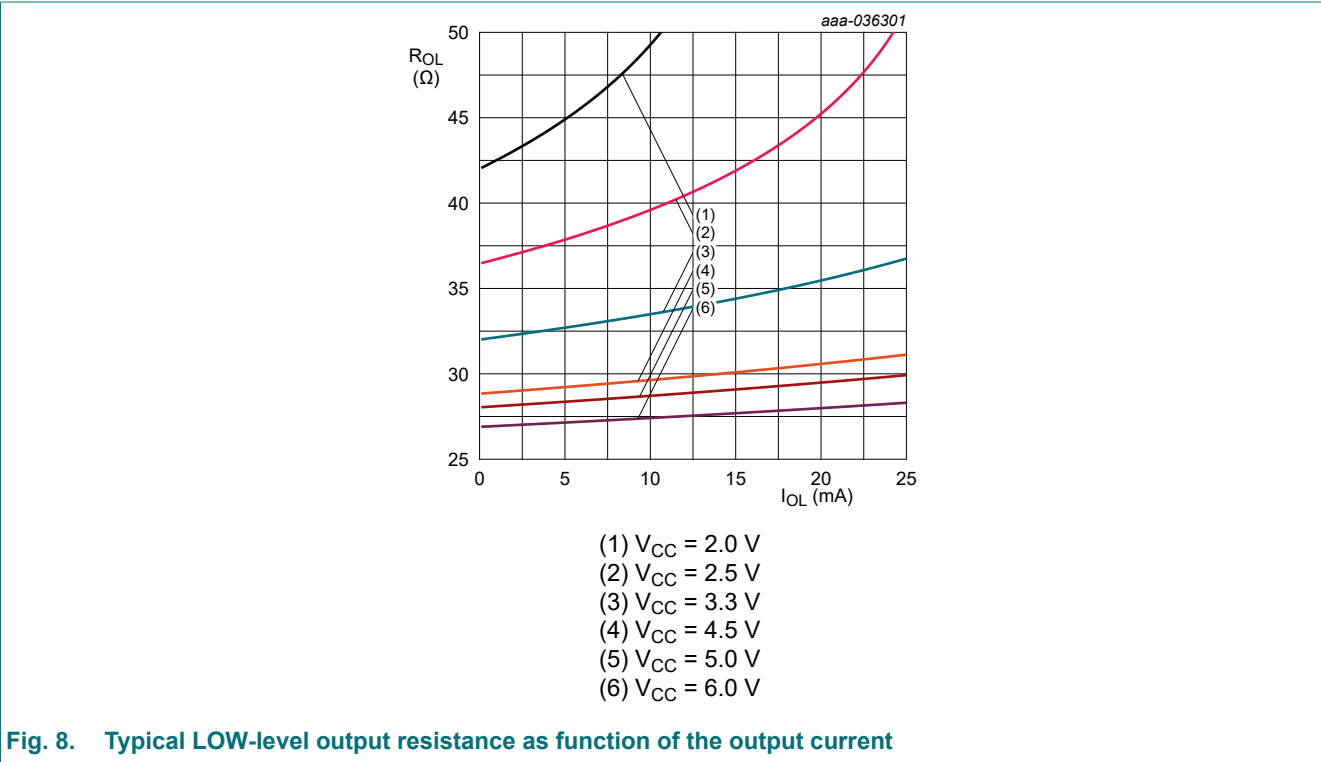
[1] Guaranteed by design.

9.1. Transfer characteristic waveforms and graphs

9.1.1. For inputs



9.1.2. For outputs



10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see [Section 10.1](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
t_{pd}	propagation delay	nA, nB to nY; see Fig. 9 [2]								
		$V_{CC} = 2\text{ V}$	-	15	21	-	24	-	25	ns
		$V_{CC} = 4.5\text{ V}$	-	9	12	-	13	-	13	ns
		$V_{CC} = 6\text{ V}$	-	9	11	-	12	-	12	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	-	10	17	-	18	-	19	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	9	12	-	13	-	13	ns
t_t	transition time	nY; see Fig. 9 [3]								
		$V_{CC} = 2\text{ V}$	-	9	13	-	15	-	16	ns
		$V_{CC} = 4.5\text{ V}$	-	5	7	-	8	-	8	ns
		$V_{CC} = 6\text{ V}$	-	4	6	-	7	-	7	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	-	5	8	-	9	-	10	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	4	7	-	8	-	8	ns
C_i	input capacitance		-	1.5	-	-	5	-	5	pF

Quad 2-input NAND gate with Schmitt-trigger inputs and open-drain output

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
C _{PD}	power dissipation capacitance	f _i = 1 MHz; C _L = 0 pF; V _I = GND to V _{CC} ; V _{CC} = 2.0 V to 6.0 V	-	3	-	-	-	-	-	pF

- [1] Typical values are measured at nominal supply voltage.
- [2] t_{pd} is the same as t_{PZL} and t_{PLZ}.
- [3] t_i is the same as t_{TZL}.
- [4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
Σ(C_L × V_{CC}² × f_o) = sum of outputs;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V.

10.1. Waveforms and test circuit

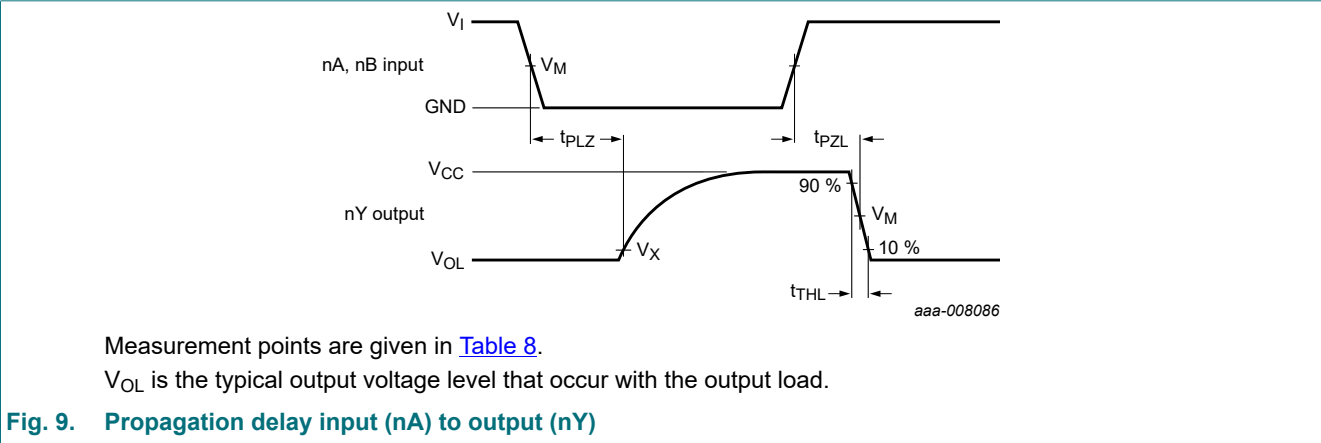


Table 8. Measurement points

Input	Output		
V _M	V _M	V _X	V _Y
0.5V _{CC}	0.5V _{CC}	10 %	90 %

Quad 2-input NAND gate with Schmitt-trigger inputs and open-drain output

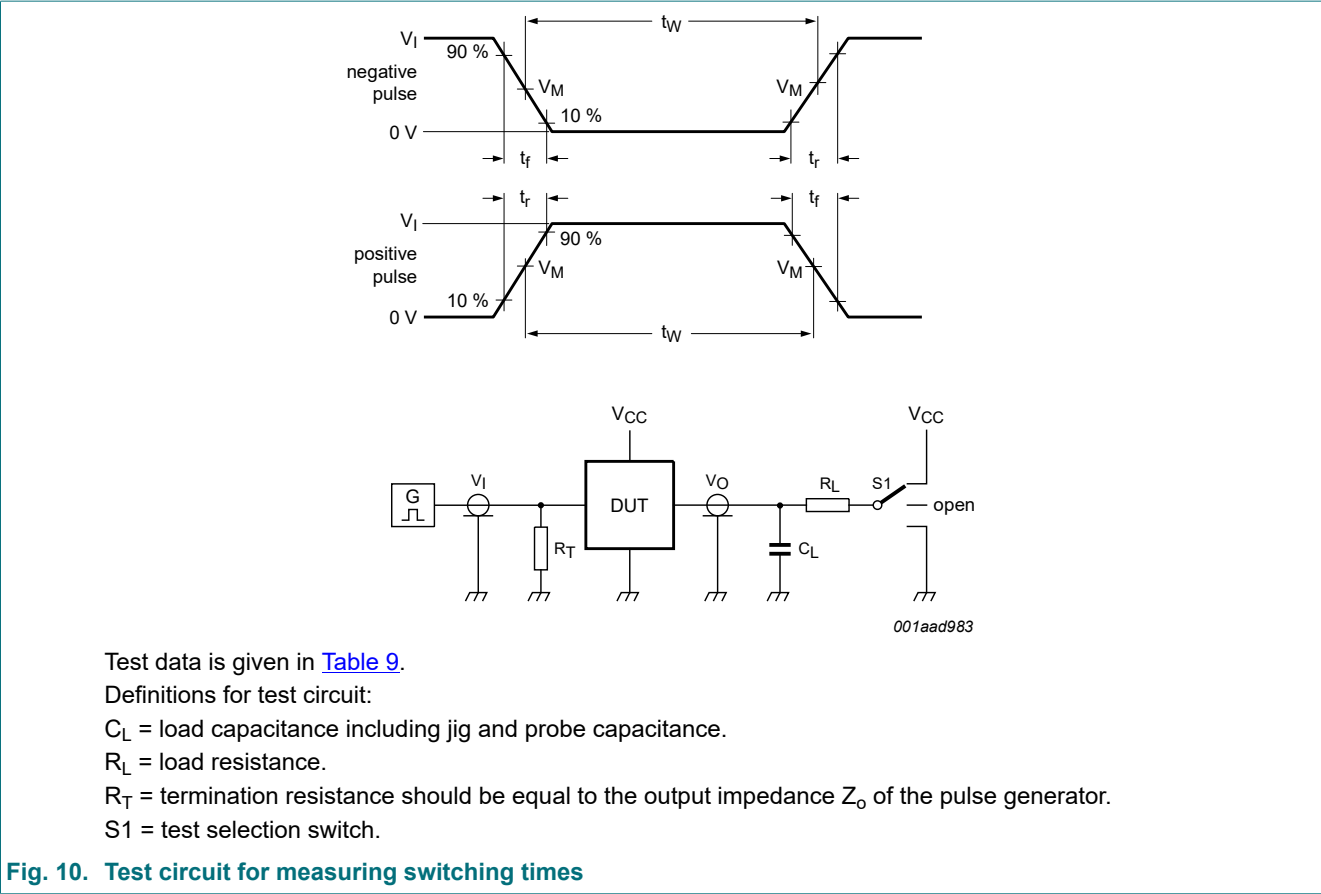


Fig. 10. Test circuit for measuring switching times

Table 9. Test data

Input		Load		S1 position		
V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
V_{CC}	2.5 ns	50 pF	1 kΩ	open	GND	V_{CC}

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm SOT108-1

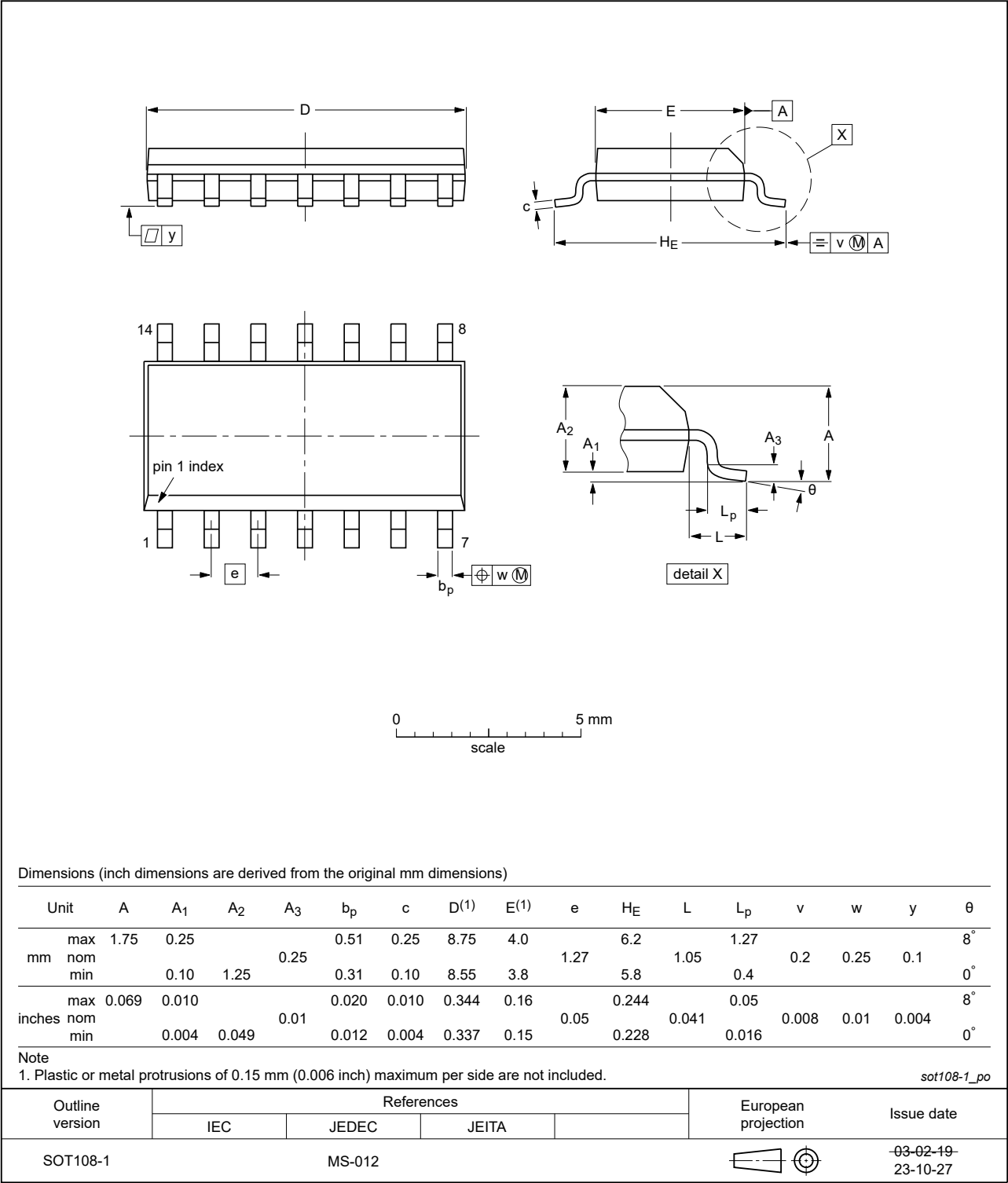


Fig. 11. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

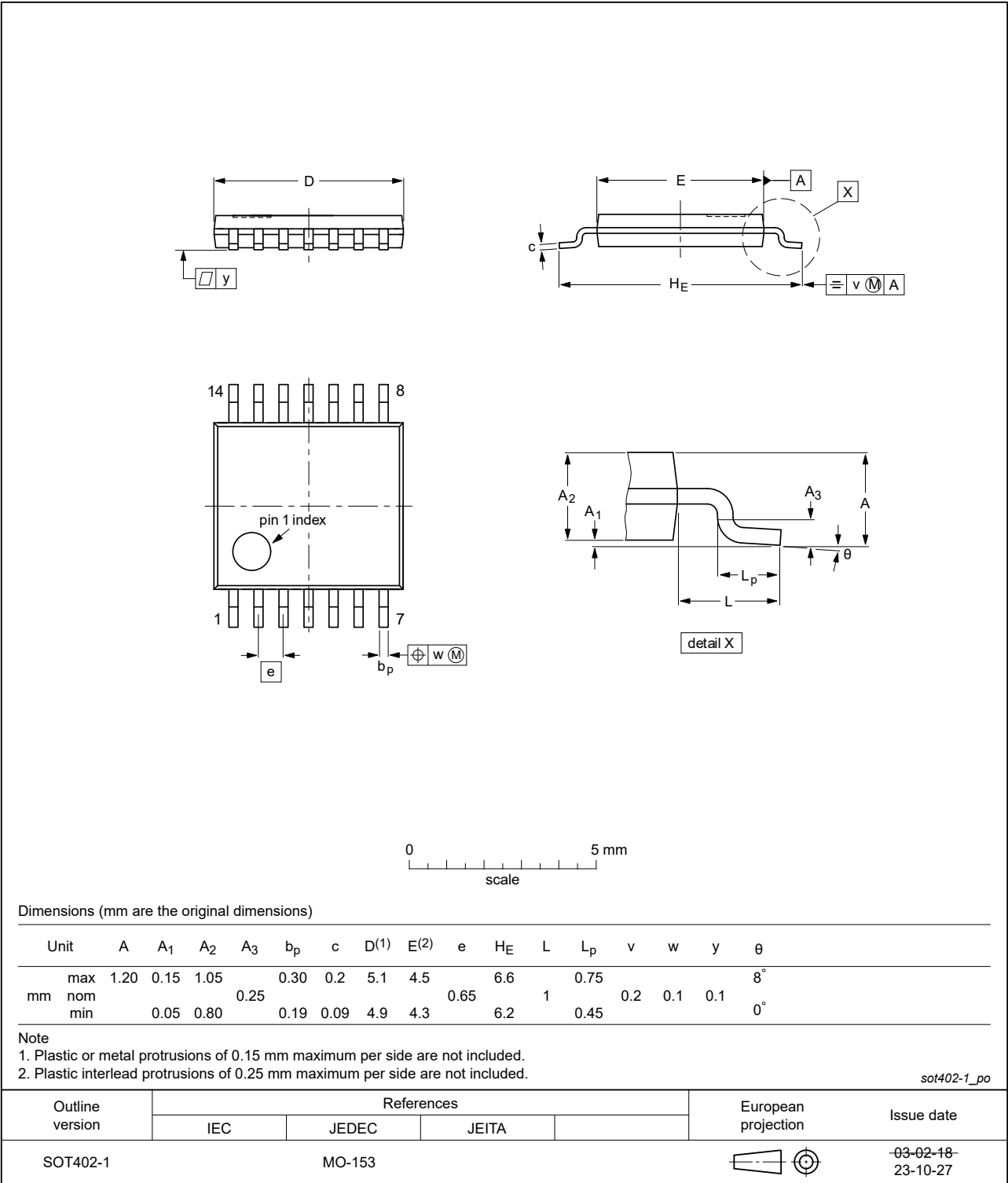


Fig. 12. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1



Fig. 13. Package outline SOT762-1 (DHVQFN14)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charge Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HCS03 v.1	20250723	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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Contents

1. General description..... 1

2. Features and benefits..... 1

3. Ordering information..... 1

4. Functional diagram..... 2

5. Pinning information..... 2

5.1. Pinning..... 2

5.2. Pin description..... 2

6. Functional description..... 3

7. Limiting values..... 3

8. Recommended operating conditions..... 3

9. Static characteristics..... 4

9.1. Transfer characteristic waveforms and graphs..... 5

9.1.1. For inputs..... 5

9.1.2. For outputs..... 6

10. Dynamic characteristics..... 6

10.1. Waveforms and test circuit..... 7

11. Package outline..... 9

12. Abbreviations..... 12

13. Revision history..... 12

14. Legal information..... 13

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