

74HC73-Q100

Dual JK flip-flop with reset; negative-edge trigger

Rev. 2 — 26 March 2024

Product data sheet

1. General description

The 74HC73-Q100 is a dual negative edge triggered JK flip-flop with individual J, K, clock ($n\overline{CP}$) and reset ($n\overline{R}$) inputs and complementary nQ and $n\overline{Q}$ outputs. The J and K inputs must be stable one set-up time prior to the HIGH-to-LOW clock transition for predictable operation. ($n\overline{R}$) is asynchronous, when LOW it overrides the clock and data inputs, forcing the nQ output LOW and the $n\overline{Q}$ output HIGH. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

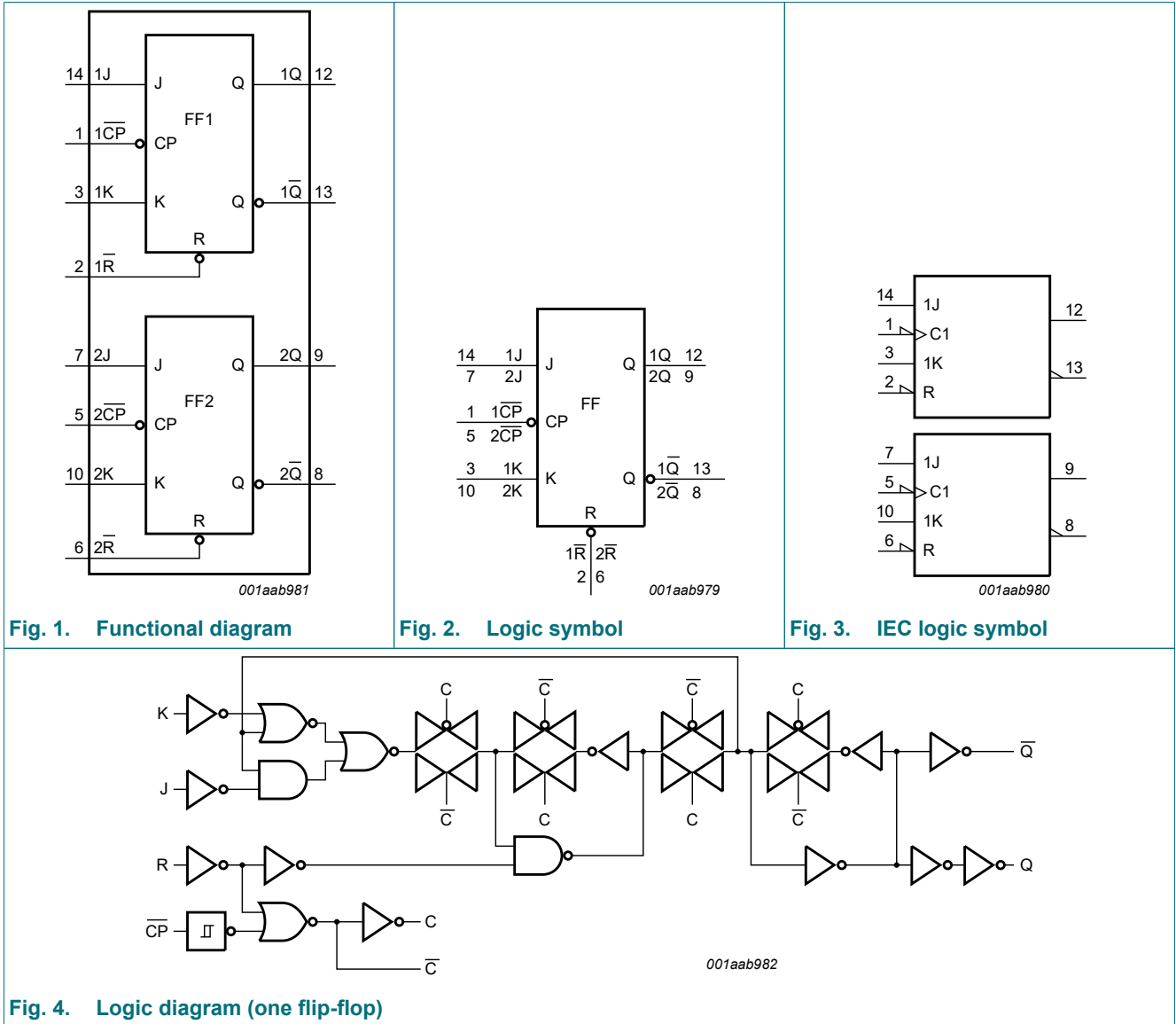
- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- CMOS low-power dissipation
- Wide supply voltage range from 2.0 to 6.0 V
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards
 - JESD8C (2.7 V to 3.6 V)
 - JESD7A (2.0 V to 6.0 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74HC73D-Q100	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1

4. Functional diagram



5. Pinning information

5.1. Pinning

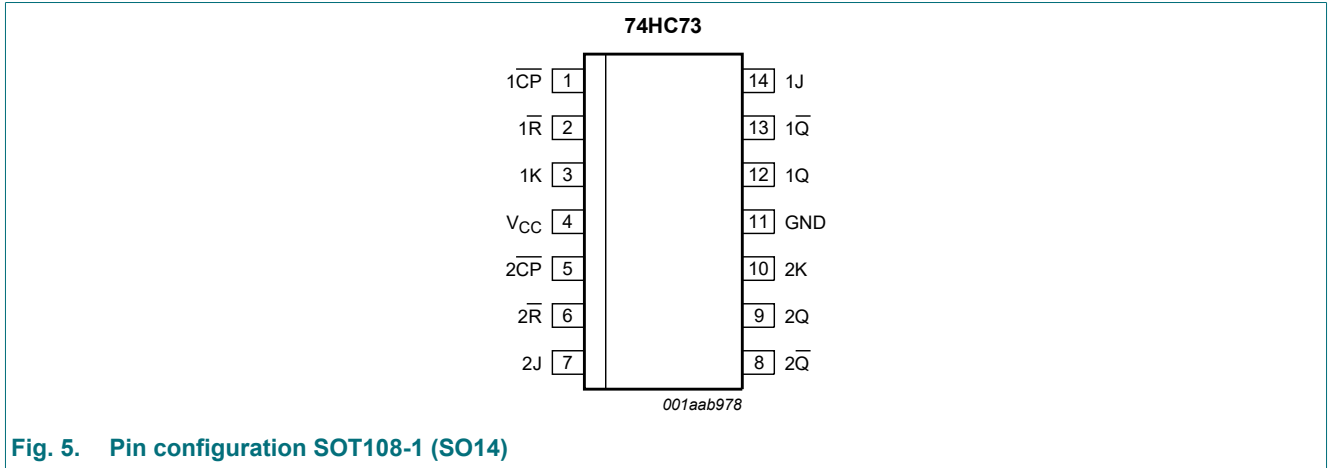


Fig. 5. Pin configuration SOT108-1 (SO14)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1CP, 2CP	1, 5	clock input (HIGH-to-LOW edge-triggered); also referred to as nCP
1R, 2R	2, 6	asynchronous reset input (active LOW); also referred to as nR
1K, 2K	3, 10	synchronous K input; also referred to as nK
VCC	4	positive supply voltage
GND	11	ground (0 V)
1Q, 2Q	12, 9	true output; also referred to as nQ
1Q, 2Q	13, 8	complement output; also referred to as nQ
1J, 2J	14, 7	synchronous J input; also referred to as nJ

6. Functional description

Table 3. Function table

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the HIGH-to-LOW clock transition;

L = LOW voltage level; l = LOW voltage level one set-up time prior to the HIGH-to-LOW clock transition;

q = state of referenced output one set-up time prior to the HIGH-to-LOW clock transition;

X = don't care; ↓ = HIGH-to-LOW clock transition.

Input				Output		Operating mode
nR	nCP	nJ	nK	nQ	nQ	
L	X	X	X	L	H	asynchronous reset
H	↓	h	h	q	q	toggle
H	↓	l	h	L	H	load 0 (reset)
H	↓	h	l	H	L	load 1 (set)
H	↓	l	l	q	q	hold (no change)

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ [1]	-	± 20	mA
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ [1]	-	± 20	mA
I_O	output current	$V_O = -0.5\text{ V}$ to $V_{CC} + 0.5\text{ V}$	-	± 25	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$ [2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$V_{CC} = 2.0\text{ V}$	1.5	1.2	-	1.5	-	1.5	-	V
		$V_{CC} = 4.5\text{ V}$	3.15	2.4	-	3.15	-	3.15	-	V
		$V_{CC} = 6.0\text{ V}$	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 2.0\text{ V}$	-	0.8	0.5	-	0.5	-	0.5	V
		$V_{CC} = 4.5\text{ V}$	-	2.1	1.35	-	1.35	-	1.35	V
		$V_{CC} = 6.0\text{ V}$	-	2.8	1.8	-	1.8	-	1.8	V

Dual JK flip-flop with reset; negative-edge trigger

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = -20 µA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -20 µA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -20 µA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = -4 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I _O = -5.2 mA; V _{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 20 µA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 µA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 µA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	4.0	-	40.0	-	80.0	µA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see Fig. 8

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t _{pd}	propagation delay	n $\overline{C}P$ to nQ; see Fig. 6 [1]								
		V _{CC} = 2.0 V	-	52	160	-	200	-	240	ns
		V _{CC} = 4.5 V	-	19	32	-	40	-	48	ns
		V _{CC} = 6.0 V	-	15	27	-	34	-	41	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	16	-	-	-	-	-	ns
		n $\overline{C}P$ to n \overline{Q} ; see Fig. 6								
		V _{CC} = 2.0 V	-	52	160	-	200	-	240	ns
		V _{CC} = 4.5 V	-	19	32	-	40	-	48	ns
		V _{CC} = 6.0 V	-	15	27	-	34	-	41	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	16	-	-	-	-	-	ns
		n \overline{R} to nQ, n \overline{Q} ; see Fig. 7								
		V _{CC} = 2.0 V	-	50	145	-	180	-	220	ns
		V _{CC} = 4.5 V	-	18	29	-	36	-	44	ns
		V _{CC} = 6.0 V	-	14	25	-	31	-	38	ns
V _{CC} = 5.0 V; C _L = 15 pF	-	15	-	-	-	-	-	ns		

Dual JK flip-flop with reset; negative-edge trigger

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t _t	transition time	nQ, n \bar{Q} ; see Fig. 6 [2]								
		V _{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V _{CC} = 6.0 V	-	6	13	-	16	-	19	ns
t _w	pulse width	n \overline{CP} input, HIGH or LOW; see Fig. 6								
		V _{CC} = 2.0 V	80	22	-	100	-	120	-	ns
		V _{CC} = 4.5 V	16	8	-	20	-	24	-	ns
		V _{CC} = 6.0 V	14	6	-	17	-	20	-	ns
		n \overline{R} input, HIGH or LOW; see Fig. 7								
		V _{CC} = 2.0 V	80	22	-	100	-	120	-	ns
		V _{CC} = 4.5 V	16	8	-	20	-	24	-	ns
		V _{CC} = 6.0 V	14	6	-	17	-	20	-	ns
t _{rec}	recovery time	n \overline{R} to n \overline{CP} ; see Fig. 7								
		V _{CC} = 2.0 V	80	22	-	100	-	120	-	ns
		V _{CC} = 4.5 V	16	8	-	20	-	24	-	ns
		V _{CC} = 6.0 V	14	6	-	17	-	20	-	ns
t _{su}	set-up time	nJ, nK to n \overline{CP} ; see Fig. 6								
		V _{CC} = 2.0 V	80	22	-	100	-	120	-	ns
		V _{CC} = 4.5 V	16	8	-	20	-	24	-	ns
		V _{CC} = 6.0 V	14	6	-	17	-	20	-	ns
t _h	hold time	nJ, nK to n \overline{CP} ; see Fig. 6								
		V _{CC} = 2.0 V	3	-8	-	3	-	3	-	ns
		V _{CC} = 4.5 V	3	-3	-	3	-	3	-	ns
		V _{CC} = 6.0 V	3	-2	-	3	-	3	-	ns
f _{max}	maximum frequency	n \overline{CP} input; see Fig. 6								
		V _{CC} = 2.0 V	6.0	23	-	4.8	-	4.0	-	MHz
		V _{CC} = 4.5 V	30	70	-	24	-	20	-	MHz
		V _{CC} = 6.0 V	35	83	-	28	-	24	-	MHz
		V _{CC} = 5.0 V; C _L = 15 pF	-	77	-	-	-	-	-	MHz
C _{PD}	power dissipation capacitance	per flip-flop; V _I = GND to V _{CC} [3]	-	30	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL}, t_{PLH}.

[2] t_t is the same as t_{THL}, t_{TLH}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μ W).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

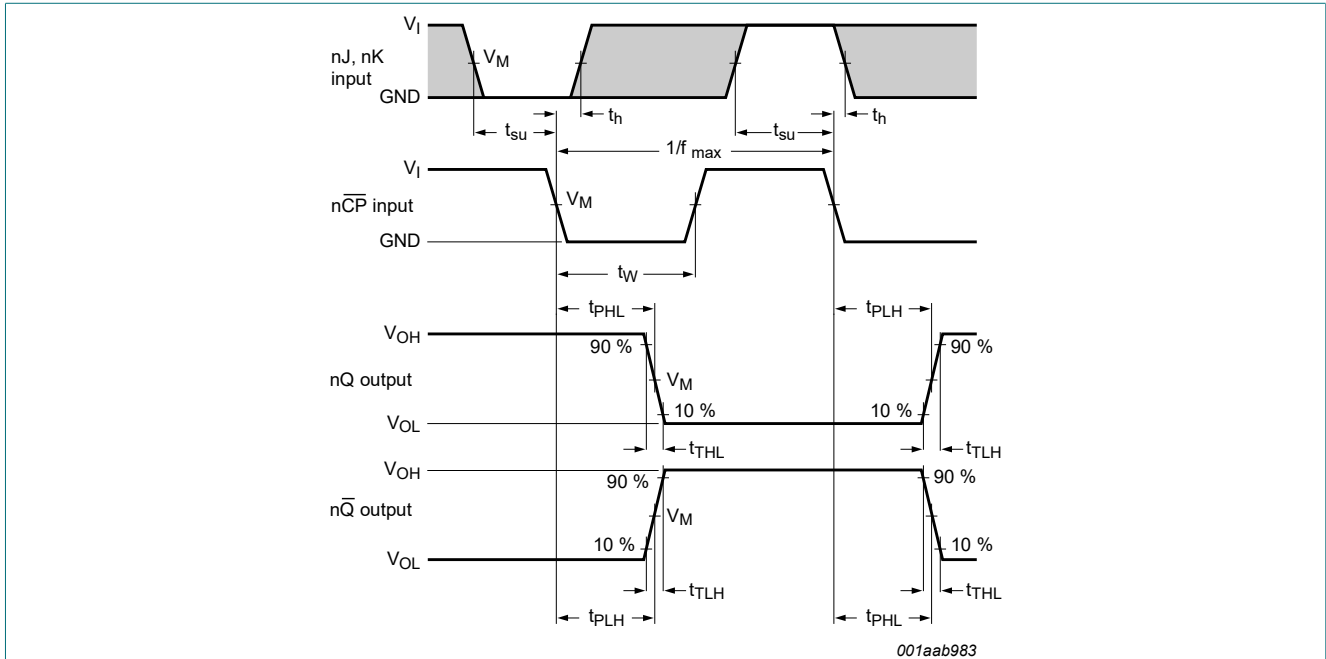
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

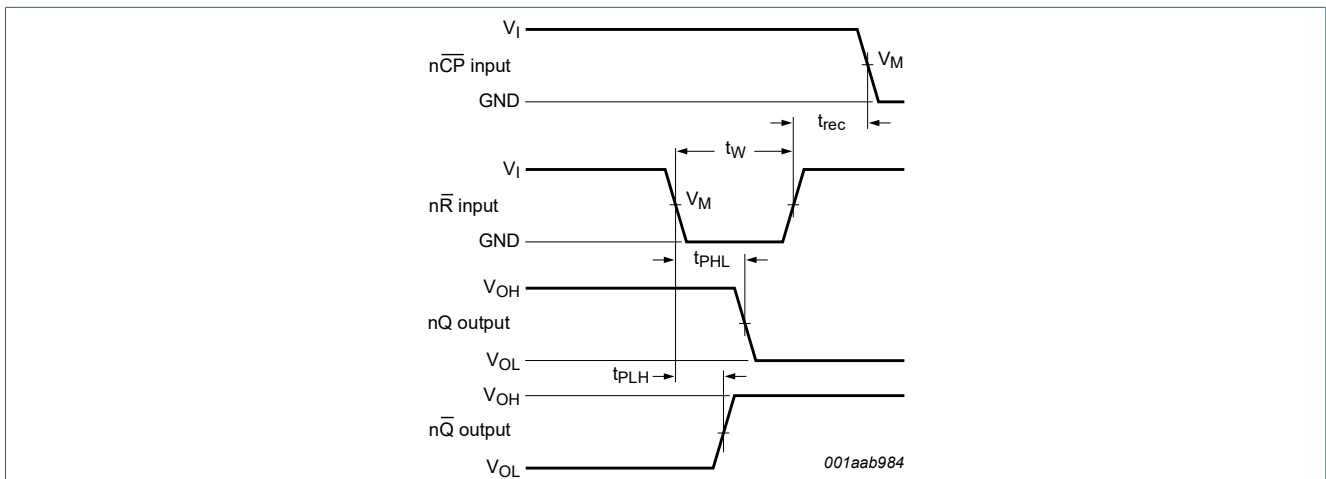
$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

10.1. Waveforms and test circuit



Measurement points are given in [Table 8](#).
 The shaded areas indicate when the input is permitted to change for predictable output performance.
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 6. Waveforms showing the clock (nCP) to output (nQ, nQ-bar) propagation delays, the clock pulse width, the J and K to nCP set-up and hold times, the output transition times and the maximum clock frequency



Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 7. Waveforms showing the reset (nR) input to output (nQ, nQ-bar) propagation delays and the reset pulse width and the nR to nCP removal time

Table 8. Measurement points

Input		Output
V_I	V_M	V_M
V_{CC}	$0.5V_{CC}$	$0.5V_{CC}$

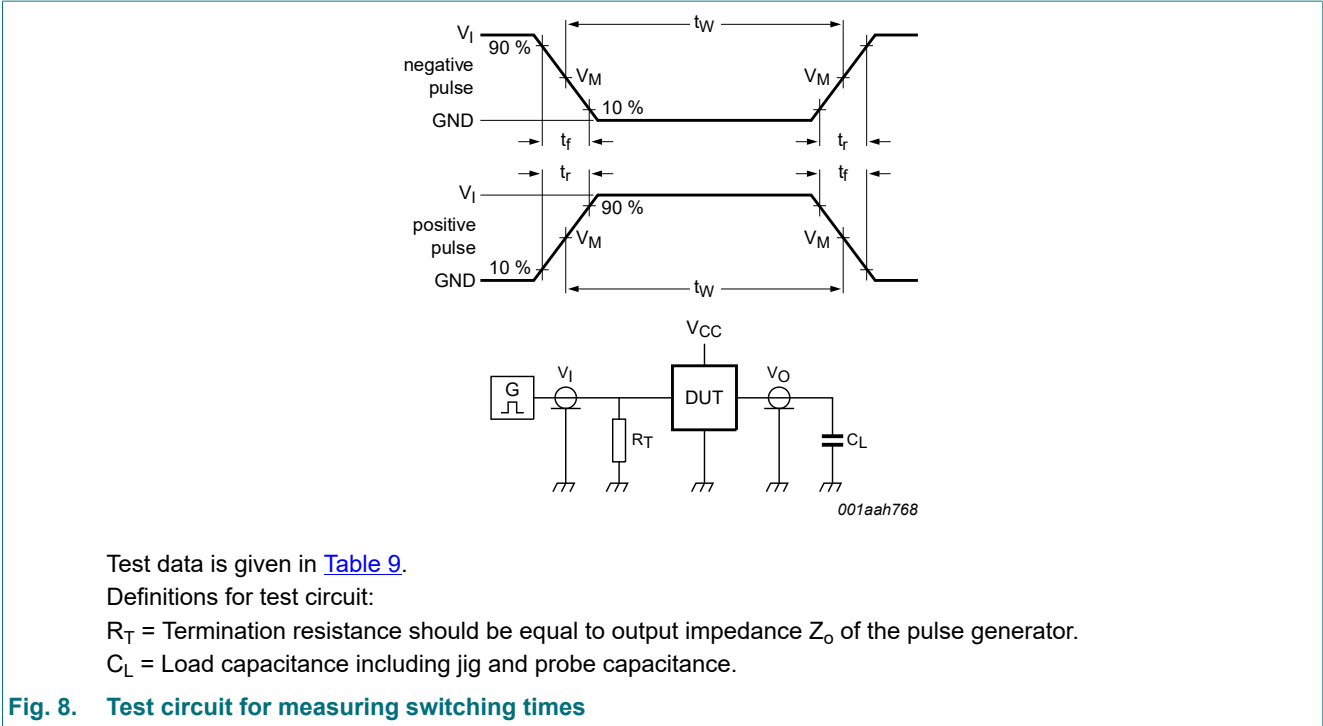


Fig. 8. Test circuit for measuring switching times

Table 9. Test data

Input		Load
V_I	t_r, t_f	C_L
V_{CC}	6 ns	15 pF, 50 pF

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

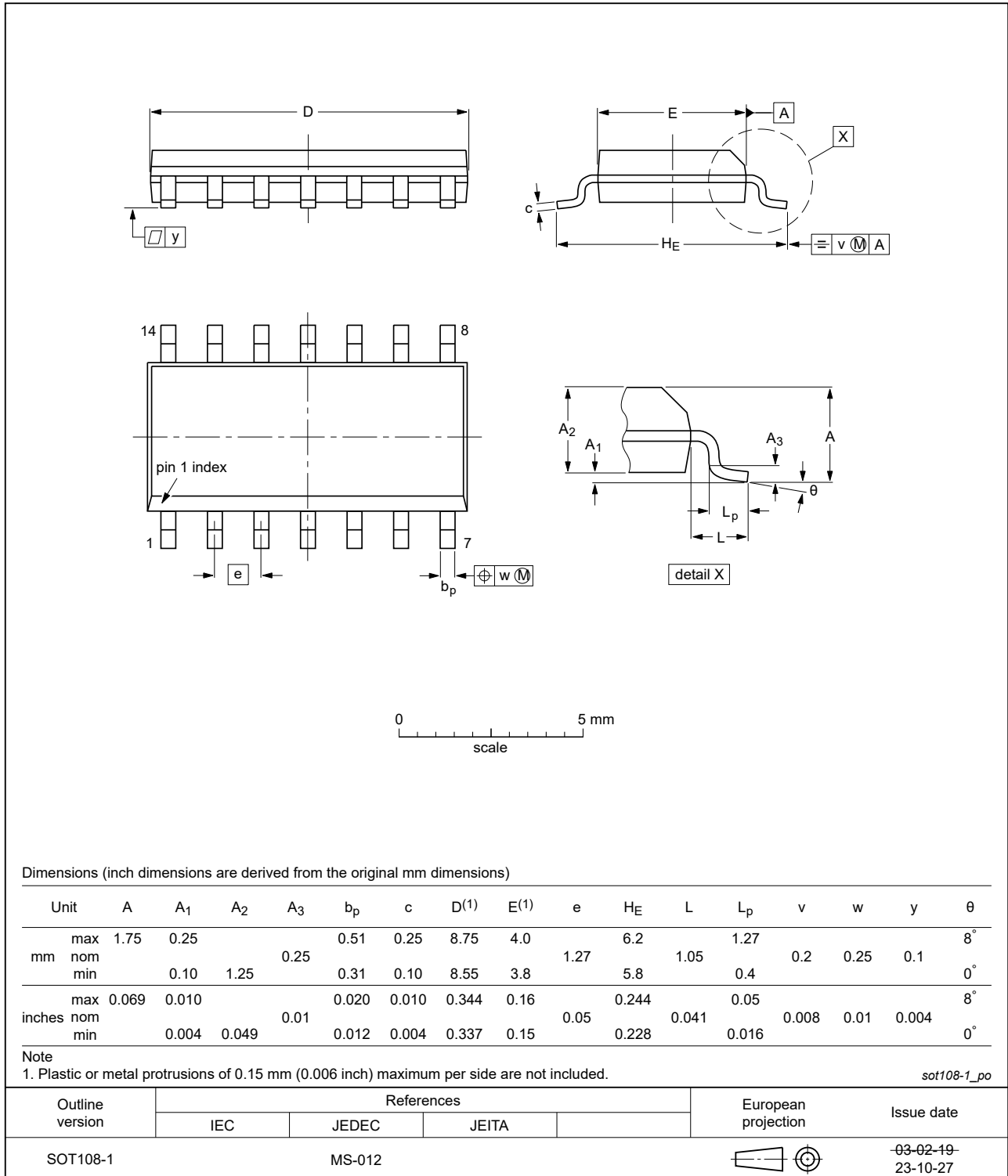


Fig. 9. Package outline SOT108-1 (SO14)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC73_Q100 v.2	20240326	Product data sheet	-	74HC73_Q100 v.1
Modifications:	<ul style="list-style-type: none"> • Fig. 9: Aligned SO package outline drawing to JEDEC MS-012. • Section 2: ESD specification updated according to the latest JEDEC standard. 			
74HC73_Q100 v.1	20201204	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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Contents

1. General description	1
2. Features and benefits	1
3. Ordering information	1
4. Functional diagram	2
5. Pinning information	3
5.1. Pinning.....	3
5.2. Pin description.....	3
6. Functional description	3
7. Limiting values	4
8. Recommended operating conditions	4
9. Static characteristics	4
10. Dynamic characteristics	5
10.1. Waveforms and test circuit.....	7
11. Package outline	9
12. Abbreviations	10
13. Revision history	10
14. Legal information	11

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