

Product data sheet

1. General description

The 74HC4049 is a hex inverter with over-voltage tolerant inputs. Inputs are overvoltage tolerant to 15 V. This enables the device to be used in HIGH-to-LOW level shifting applications.

2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- Overvoltage tolerant inputs to 15 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
 - Complies with JEDEC standards:
 - JESD8C (2.7 V to 3.6 V)
 - JESD7A (2.0 V to 6.0 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

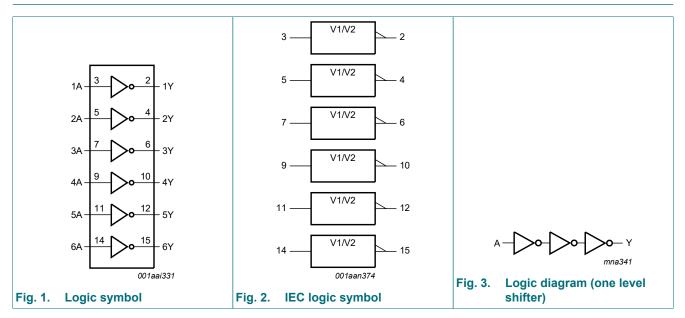
3. Ordering information

Table 1. Ordering information

Type number	Package								
	Temperature range	Name	Description	Version					
74HC4049D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	<u>SOT109-1</u>					
74HC4049PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	<u>SOT403-1</u>					

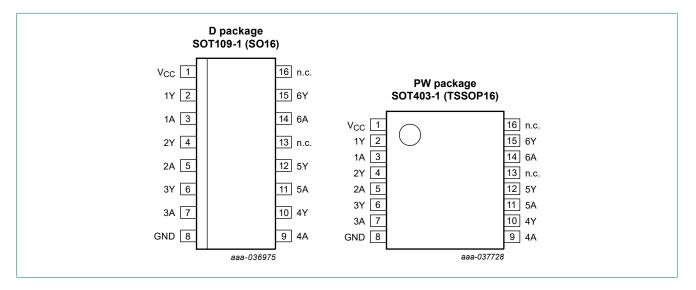


4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description						
Symbol	Pin	Description				
V _{CC}	1	supply voltage				
1Y, 2Y, 3Y, 4Y, 5Y, 6Y	2, 4, 6, 10, 12, 15	output				
1A, 2A, 3A, 4A, 5A, 6A	3, 5, 7, 9, 11, 14	input				
GND	8	ground (0 V)				
n.c.	13, 16	not connected				

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6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level.

Input	Output
nA	nY
L	Н
Н	L

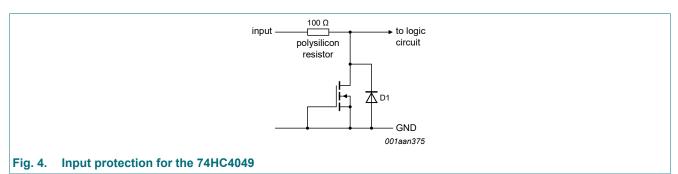
7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Мах	Unit
V _{CC}	supply voltage		-0.5	+7	V
V _{IK}	input clamping voltage		-0.5	+16	V
I _{IK}	input clamping current	V _I < -0.5 V	-20	-	mA
I _{OK}	output clamping current	$V_{\rm O}$ < -0.5 V or $V_{\rm O}$ > $V_{\rm CC}$ + 0.5 V	-	±20	mA
I _O	output current	V_{O} = -0.5 V to (V _{CC} + 0.5 V)	-	±25	mA
I _{CC}	supply current		-	+50	mA
I _{GND}	ground current		-	-50	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	[1]	-	500	mW

For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
 For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.



8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{CC}	supply voltage		2.0	5.0	6.0	V
VI	input voltage		0	-	15	V
Vo	output voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	°C

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Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V; V _I = 2.0 V	-	-	625	ns/V
		V_{CC} = 4.5 V; V _I = 4.5 V	-	1.67	139	ns/V
		V _{CC} = 6.0 V; V _I = 6.0 V	-	-	83	ns/V
		V _{CC} = 6.0 V; V _I = 10.0 V	-	-	81	ns/V
		V _{CC} = 6.0 V; V _I = 15.0 V	-	-	83	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C t	o +85 °C	-40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Max	1
VIH	HIGH-level	V _{CC} = 2.0 V	1.5	1.3	-	1.5	-	1.5	-	V
	input voltage	V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.1	-	4.2	-	4.2	-	V
V _{IL}	LOW-level	V _{CC} = 2.0 V	-	0.7	0.5	-	0.5	-	0.5	V
	input voltage	V _{CC} = 4.5 V	-	1.8	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.3	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level	V _I = V _{IH} or V _{IL}								
	output voltage	I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = -4.0 mA; V _{CC} = 4.5 V	3.98	-	-	3.84	-	3.7	-	V
		I _O = -5.2 mA; V _{CC} = 6.0 V	5.48	-	-	5.34	-	5.2	-	V
V _{OL}	LOW-level	V _I = V _{IH} or V _{IL}								
	output voltage	I _O = 20 μA; V _{CC} = 2.0 V	-	-	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	-	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	-	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	-	0.26	-	0.33	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	-	0.26	-	0.33	-	0.4	V
l _l	input leakage	$V_{I} = V_{CC}$ or GND; $V_{CC} = 6.0$ V	-	-	±0.1	-	±1.0	-	±1.0	μA
	current	V _I = 15 V; V _{CC} = 2.0 V to 6.0 V	-	-	±0.5	-	±5.0	-	±5.0	μA
I _{CC}	supply current	V _I = 15 V or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	2.0	-	20	-	40	μA
CI	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); $C_L = 50 \text{ pF}$ unless otherwise specified; for test circuit see Fig. 6.

Symbol	Parameter	Conditions		25 °C		-40 °C to +85 °C		-40 °C to +125 °C		Unit	
				Min	Тур	Max	Min	Max	Min	Max	1
t _{pd}	propagation	nA to nY; see <u>Fig. 5</u>	[1]								
	delay	V _{CC} = 2.0 V		-	28	85	-	105	-	130	ns
		V _{CC} = 4.5 V		-	10	17	-	21	-	26	ns
		V _{CC} = 5 V; C _L = 15 pF		-	8	-	-	-	-	-	ns
		V _{CC} = 6.0 V		-	8	14	-	18	-	22	ns
t _t	transition	nY; see <u>Fig. 5</u>	[2]								
	time	V _{CC} = 2.0 V		-	19	75	-	95	-	110	ns
		V _{CC} = 4.5 V		-	7	15	-	19	-	22	ns
		V _{CC} = 6.0 V		-	6	13	-	16	-	19	ns
C _{PD}	power dissipation capacitance	C_L = 50 pF; f = 1 MHz; V _I = GND to V _{CC}	[3]	-	14	-	-	-	-	-	pF

t_{pd} is the same as t_{PLH} and t_{PHL}. [1]

[2]

 t_t is the same as t_{THL} and t_{TLH} . C_{PD} is used to determine the dynamic power dissipation (P_D in μ W). $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where: [3]

f_i = input frequency in MHz;

 $f_o = output$ frequency in MHz;

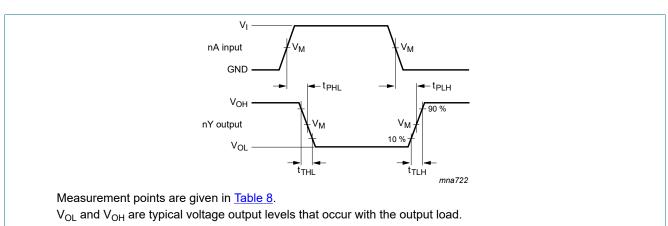
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

 $\Sigma(C_L \times V_{CC}^2 \times f_0)$ = sum of outputs.

10.1. Waveforms and test circuit



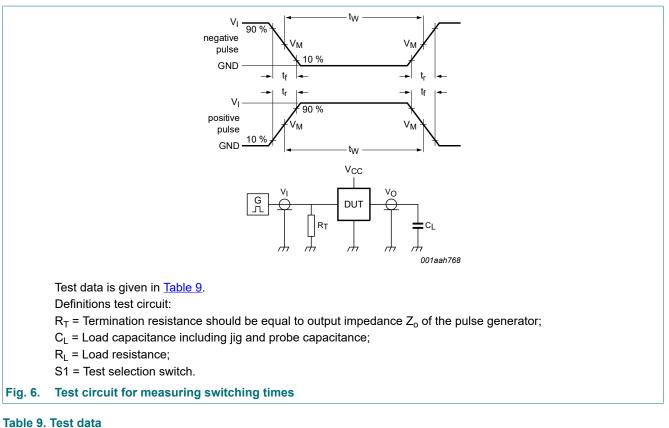
The input (nA) to output (nY) propagation delays Fig. 5.

Table 8. Measurement points

Input	Output
V _M	V _M
0.5V _{CC}	0.5V _{CC}

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Input		Load	Test	
V _I t _r , t _f		CL	-	
V _{CC}	6.0 ns	15 pF, 50 pF	t _{PLH} , t _{PHL}	

11. Package outline

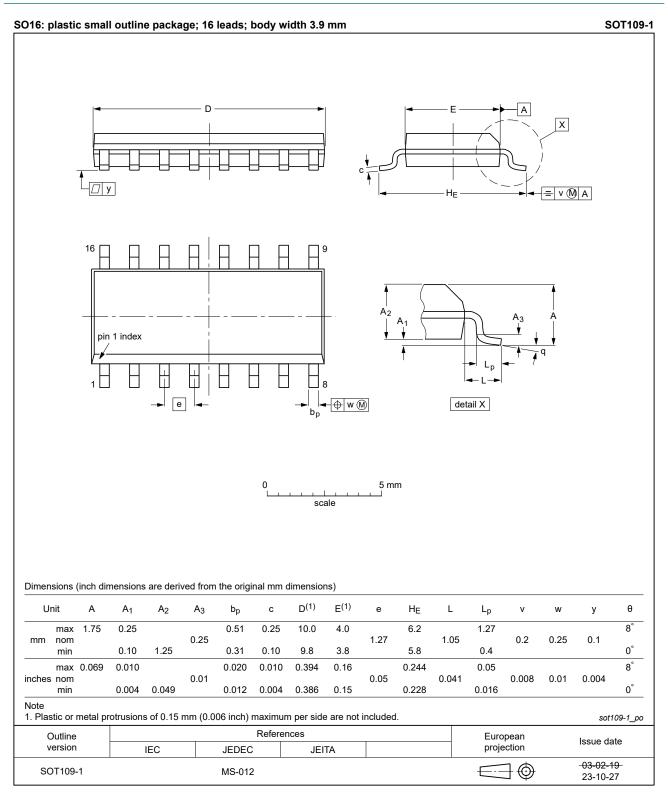


Fig. 7. Package outline SOT109-1 (SO16)

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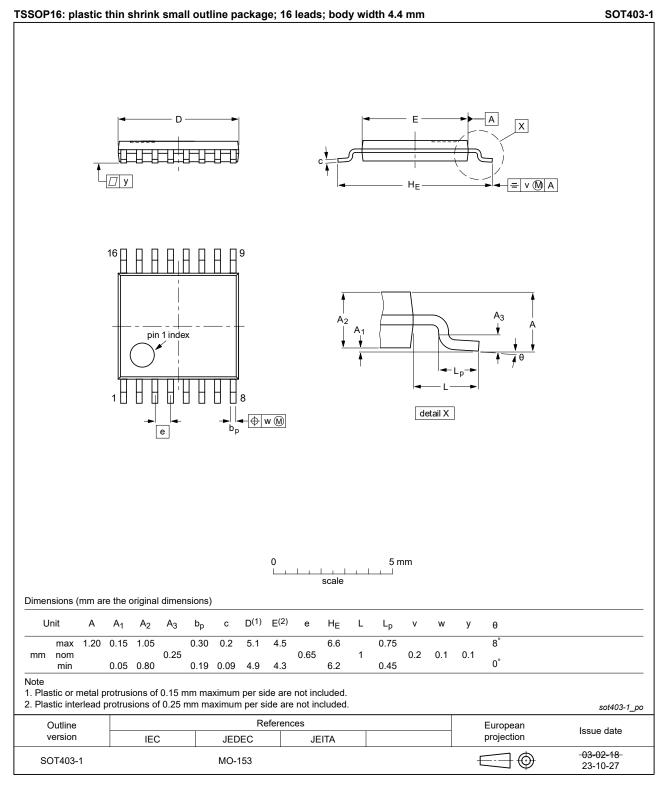


Fig. 8. Package outline SOT403-1 (TSSOP16)

12. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes				
74HC4049 v.9	20240312	Product data sheet	-	74HC4049 v.8.1				
Modifications: • Section 2: ESD specification updated according to the latest JEDEC standard. • Fig. 7 and Fig. 8: Aligned SO and TSSOP package outline drawings to JEDEC MS-0 and MO-153								
74HC4049 v.8.1	20231018	Product data sheet	-	74HC4049 v.7				
Modifications:	• <u>Section 7</u> : I	 <u>Section 2</u> updated. <u>Section 7</u>: Derating values for P_{tot} total power dissipation updated. Type number 74HC4049DB (SOT338-1 / SSOP16) removed. 						
74HC4049 v.7	20160205	Product data sheet	-	74HC4049 v.6				
Modifications:	Type numb	er 74HC4049N (SOT38-4)	removed.	1				
74HC4049 v.6	20130108	Product data sheet	-	74HC4049 v.5				
Modifications:	New gener	al description.	1	1				
74HC4049 v.5	20120803	Product data sheet	-	74HC4049 v.4				
Modifications:	Measureme	ent points added to <u>Fig. 5</u> (e	errata).	1				
74HC4049 v.4	20111212	Product data sheet	-	74HC4049 v.3				
74HC4049 v.3	20101230	Product data sheet	-	74HC4049_CNV v.2				
74HC4049_CNV v.2	19970827	Product specification	-	-				

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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