1. General description

The 74HC191 is an asynchronously presettable 4-bit binary up/down counter. It contains four master/slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous count-up and count-down operation. Asynchronous parallel load capability permits the counter to be preset to any desired value. Information present on the parallel data inputs (D0 to D3) is loaded into the counter and appears on the outputs when the parallel load (PL) input is LOW. This operation overrides the counting function. Counting is inhibited by a HIGH level on the count enable (CE) input. When CE is LOW internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The up/down (U/D) input signal determines the direction of counting as indicated in the function table. The CE input may go LOW when the clock is in either state, however, the LOW-to-HIGH CE transition must occur only when the clock is HIGH. Also, the U/D input should be changed only when either CE or CP is HIGH. Overflow/underflow indications are provided by two types of outputs, the terminal count (TC) and ripple clock (RC). The TC output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches ‘15’ in the count-up-mode. The TC output will remain HIGH until a state change occurs, either by counting or presetting, or until U/D is changed. Do not use the TC output as a clock signal because it is subject to decoding spikes. The TC signal is used internally to enable the RC output. When TC is HIGH and CE is LOW, the RC output follows the clock pulse (CP). This feature simplifies the design of multistage counters as shown in Fig. 5 and Fig. 6. In Fig. 5, each RC output is used as the clock input to the next higher stage. It is only necessary to inhibit the first stage to prevent counting in all stages, since a HIGH on CE inhibits the RC output pulse. The timing skew between state changes in the first and last stages is represented by the cumulative delay of the clock as it ripples through the preceding stages. This can be a disadvantage of this configuration in some applications. Fig. 6 shows a method of causing state changes to occur simultaneously in all stages. The RC outputs propagate the carry/borrow signals in ripple fashion and all clock inputs are driven in parallel. In this configuration the duration of the clock LOW state must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. Since the RC output of any package goes HIGH shortly after its CP input goes HIGH there is no such restriction on the HIGH-state duration of the clock. In Fig. 7, the configuration shown avoids ripple delays and their associated restrictions. Combining the TC signals from all the preceding stages forms the CE input for a given stage. An enable must be included in each carry gate in order to inhibit counting. The TC output of a given stage is not affected by its own CE signal therefore the simple inhibit scheme of Fig. 5 and Fig. 6 does not apply. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of VCC.

2. Features and benefits

- Wide supply voltage range from 2.0 to 6.0 V
- CMOS low power dissipation
- High noise immunity
-Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- CMOS input levels
- Synchronous reversible counting
- Asynchronous parallel load
- Count enable control for synchronous expansion
- Single up/down control input
Nexperia

74HC191

Presettable synchronous 4-bit binary up/down counter

- Complies with JEDEC standards:
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

<table>
<thead>
<tr>
<th>Type number</th>
<th>Package</th>
<th>Temperature range</th>
<th>Name</th>
<th>Description</th>
<th>Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>74HC191D</td>
<td>SO16</td>
<td>-40 °C to +125 °C</td>
<td>plastic small outline package; 16 leads; body width 3.9 mm</td>
<td>SOT109-1</td>
<td></td>
</tr>
<tr>
<td>74HC191PW</td>
<td>TSSOP16</td>
<td>-40 °C to +125 °C</td>
<td>plastic thin shrink small outline package; 16 leads; body width 4.4 mm</td>
<td>SOT403-1</td>
<td></td>
</tr>
</tbody>
</table>

4. Functional diagram

Fig. 1. Logic symbol

Fig. 2. Functional diagram
5. Pinning information

5.1. Pinning

![Pin configuration SOT109-1 (SO16)](aaa-024377)

![Pin configuration SOT403-1 (TSSOP16)](aaa-024378)

Table 2. Pin description

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D0, D1, D2, D3</td>
<td>15, 1, 10, 9</td>
<td>data input</td>
</tr>
<tr>
<td>Q0, Q1, Q2, Q3</td>
<td>3, 2, 6, 7</td>
<td>flip-flop output</td>
</tr>
<tr>
<td>CE</td>
<td>4</td>
<td>count enable input (active LOW)</td>
</tr>
<tr>
<td>U/D</td>
<td>5</td>
<td>up/down input</td>
</tr>
<tr>
<td>GND</td>
<td>8</td>
<td>ground (0 V)</td>
</tr>
<tr>
<td>PL</td>
<td>11</td>
<td>parallel load input (active LOW)</td>
</tr>
<tr>
<td>TC</td>
<td>12</td>
<td>terminal count output</td>
</tr>
<tr>
<td>RC</td>
<td>13</td>
<td>ripple clock output (active LOW)</td>
</tr>
<tr>
<td>CP</td>
<td>14</td>
<td>clock input (LOW-to-HIGH, edge-triggered)</td>
</tr>
<tr>
<td>VCC</td>
<td>16</td>
<td>supply voltage</td>
</tr>
</tbody>
</table>

5.2. Pin description

6. Functional description

Table 3. Function table

<table>
<thead>
<tr>
<th>Operating mode</th>
<th>Input</th>
<th>U/D</th>
<th>CE</th>
<th>CP</th>
<th>Dn</th>
<th>Qn</th>
</tr>
</thead>
<tbody>
<tr>
<td>parallel load</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td></td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>count up</td>
<td>H</td>
<td>L</td>
<td>I</td>
<td>↑</td>
<td>X</td>
<td>count up</td>
</tr>
<tr>
<td>count down</td>
<td>H</td>
<td>H</td>
<td>I</td>
<td>↑</td>
<td>X</td>
<td>count down</td>
</tr>
<tr>
<td>Hold (do nothing)</td>
<td>H</td>
<td>X</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>no change</td>
</tr>
</tbody>
</table>
Table 4. TC and RC Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; \(\text{\(\uparrow\)}\) = one LOW level pulse;
\(\text{\(\downarrow\)}\) = TC goes LOW on a LOW-to-HIGH clock transition.

<table>
<thead>
<tr>
<th>Input</th>
<th>Terminal count state</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>U/D</td>
<td>CE</td>
<td>CP</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>X</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>X</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>(\text{(\uparrow)})</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>X</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>X</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>(\text{(\uparrow)})</td>
</tr>
</tbody>
</table>

Fig. 5. N-stage ripple counter using ripple clock

Fig. 6. Synchronous n-stage counter using ripple carry/borrow

Fig. 7. Synchronous n-stage counter with parallel gated carry/borrow
Fig. 8. Logic diagram
Typical timing sequence:
- Reset outputs to zero
- Preset to binary twelve
- Count to thirteen, fourteen, fifteen, zero, one and two
- Inhibit

Fig. 9. Typical timing sequence

7. Limiting values

Table 5. Limiting values

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{CC}</td>
<td>supply voltage</td>
<td></td>
<td>-0.5</td>
<td>+7.0</td>
<td>V</td>
</tr>
<tr>
<td>I_{IK}</td>
<td>input clamping current</td>
<td>(V_I &lt; -0.5) V or (V_I &gt; V_{CC} + 0.5) V</td>
<td>-</td>
<td>±20</td>
<td>mA</td>
</tr>
<tr>
<td>I_{OK}</td>
<td>output clamping current</td>
<td>(V_O &lt; -0.5) V or (V_O &gt; V_{CC} + 0.5) V</td>
<td>-</td>
<td>±20</td>
<td>mA</td>
</tr>
<tr>
<td>I_O</td>
<td>output current</td>
<td>(V_O = -0.5) V to (V_{CC} + 0.5) V</td>
<td>-</td>
<td>±25</td>
<td>mA</td>
</tr>
<tr>
<td>I_{CC}</td>
<td>supply current</td>
<td></td>
<td>-</td>
<td>50</td>
<td>mA</td>
</tr>
<tr>
<td>I_{GND}</td>
<td>ground current</td>
<td></td>
<td>-50</td>
<td>-</td>
<td>mA</td>
</tr>
<tr>
<td>T_{stg}</td>
<td>storage temperature</td>
<td></td>
<td>-65</td>
<td>+150</td>
<td>°C</td>
</tr>
<tr>
<td>P_{tot}</td>
<td>total power dissipation</td>
<td></td>
<td>[1]</td>
<td>500</td>
<td>mW</td>
</tr>
</tbody>
</table>

[1] For SOT109-1 (SO16) package: \(P_{tot}\) derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: \(P_{tot}\) derates linearly with 8.5 mW/K above 91 °C.
8. Recommended operating conditions

Table 6. Recommended operating conditions
Voltages are referenced to GND (ground = 0 V)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{CC}</td>
<td>supply voltage</td>
<td></td>
<td>2.0</td>
<td>5.0</td>
<td>6.0</td>
<td>V</td>
</tr>
<tr>
<td>V_{I}</td>
<td>input voltage</td>
<td></td>
<td>0</td>
<td>-</td>
<td>V_{CC}</td>
<td>V</td>
</tr>
<tr>
<td>V_{O}</td>
<td>output voltage</td>
<td></td>
<td>0</td>
<td>-</td>
<td>V_{CC}</td>
<td>V</td>
</tr>
<tr>
<td>T_{amb}</td>
<td>ambient temperature</td>
<td></td>
<td>-40</td>
<td>+25</td>
<td>+125</td>
<td>°C</td>
</tr>
<tr>
<td>Δt/ΔV</td>
<td>input transition rise and fall rate</td>
<td>V_{CC} = 2.0 V</td>
<td>-</td>
<td>-</td>
<td>625</td>
<td>ns/V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_{CC} = 4.5 V</td>
<td>-</td>
<td>1.67</td>
<td>139</td>
<td>ns/V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_{CC} = 6.0 V</td>
<td>-</td>
<td>-</td>
<td>83</td>
<td>ns/V</td>
</tr>
</tbody>
</table>

9. Static characteristics

Table 7. Static characteristics
At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>25 °C</th>
<th>-40 °C to +85 °C</th>
<th>-40 °C to +125 °C</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Min</td>
<td>Max</td>
</tr>
<tr>
<td>V_{IH}</td>
<td>HIGH-level input voltage</td>
<td>V_{CC} = 2.0 V</td>
<td>1.5</td>
<td>2.0</td>
<td>-</td>
<td>1.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_{CC} = 4.5 V</td>
<td>3.15</td>
<td>2.4</td>
<td>-</td>
<td>3.15</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_{CC} = 6.0 V</td>
<td>4.2</td>
<td>3.2</td>
<td>-</td>
<td>4.2</td>
</tr>
<tr>
<td>V_{IL}</td>
<td>LOW-level input voltage</td>
<td>V_{CC} = 2.0 V</td>
<td>-</td>
<td>0.8</td>
<td>0.5</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_{CC} = 4.5 V</td>
<td>-</td>
<td>2.1</td>
<td>1.35</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_{CC} = 6.0 V</td>
<td>-</td>
<td>2.8</td>
<td>1.8</td>
<td>-</td>
</tr>
<tr>
<td>V_{OH}</td>
<td>HIGH-level output voltage</td>
<td>V_{I} = V_{IH} or V_{IL}</td>
<td>1.9</td>
<td>2.0</td>
<td>-</td>
<td>1.9</td>
</tr>
<tr>
<td></td>
<td></td>
<td>I_{O} = -20 μA; V_{CC} = 2.0 V</td>
<td>4.4</td>
<td>4.5</td>
<td>-</td>
<td>4.4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>I_{O} = -20 μA; V_{CC} = 4.5 V</td>
<td>5.9</td>
<td>6.0</td>
<td>-</td>
<td>5.9</td>
</tr>
<tr>
<td></td>
<td></td>
<td>I_{O} = -4.0; V_{CC} = 4.5 V</td>
<td>3.98</td>
<td>4.32</td>
<td>-</td>
<td>3.84</td>
</tr>
<tr>
<td></td>
<td></td>
<td>I_{O} = -5.2; V_{CC} = 6.0 V</td>
<td>5.48</td>
<td>5.81</td>
<td>-</td>
<td>5.34</td>
</tr>
<tr>
<td>V_{OL}</td>
<td>LOW-level output voltage</td>
<td>V_{I} = V_{IH} or V_{IL}</td>
<td>I_{O} = 20 μA; V_{CC} = 2.0 V</td>
<td>-</td>
<td>0</td>
<td>0.1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>I_{O} = 20 μA; V_{CC} = 4.5 V</td>
<td>-</td>
<td>0</td>
<td>0.1</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td>I_{O} = 20 μA; V_{CC} = 6.0 V</td>
<td>-</td>
<td>0</td>
<td>0.1</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td>I_{O} = 4.0 mA; V_{CC} = 4.5 V</td>
<td>-</td>
<td>0.15</td>
<td>0.26</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td>I_{O} = 5.2 mA; V_{CC} = 6.0 V</td>
<td>-</td>
<td>0.16</td>
<td>0.26</td>
<td>-</td>
</tr>
<tr>
<td>I_{I}</td>
<td>input leakage current</td>
<td>V_{I} = V_{CC} or GND; V_{CC} = 6.0 V</td>
<td>-</td>
<td>-</td>
<td>±0.1</td>
<td>-</td>
</tr>
<tr>
<td>I_{CC}</td>
<td>supply current</td>
<td>V_{I} = V_{CC} or GND; I_{O} = 0 A; V_{CC} = 6.0 V</td>
<td>-</td>
<td>-</td>
<td>8.0</td>
<td>-</td>
</tr>
<tr>
<td>C_{I}</td>
<td>input capacitance</td>
<td>-</td>
<td>3.5</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>
### 10. Dynamic characteristics

**Table 8. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V); \( C_L = 50 \, \text{pF} \) unless otherwise specified; for test circuit see Fig. 18.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>(25 , ^\circ\text{C} )</th>
<th>(-40 , ^\circ\text{C} \text{ to } +85 , ^\circ\text{C} )</th>
<th>(-40 , ^\circ\text{C} \text{ to } +125 , ^\circ\text{C} )</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{pd} )</td>
<td>propagation delay</td>
<td>CP to Qn; see Fig. 10</td>
<td>( V_{CC} = 2.0 , \text{V} )</td>
<td>-</td>
<td>72</td>
<td>220</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( V_{CC} = 4.5 , \text{V} )</td>
<td>-</td>
<td>26</td>
<td>44</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( V_{CC} = 6.0 , \text{V} )</td>
<td>-</td>
<td>22</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CP to TC; see Fig. 10</td>
<td>( V_{CC} = 2.0 , \text{V} )</td>
<td>-</td>
<td>83</td>
<td>255</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( V_{CC} = 4.5 , \text{V} )</td>
<td>-</td>
<td>30</td>
<td>51</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( V_{CC} = 6.0 , \text{V} )</td>
<td>-</td>
<td>24</td>
<td>43</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CP to RC; see Fig. 11</td>
<td>( V_{CC} = 2.0 , \text{V} )</td>
<td>47</td>
<td>150</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( V_{CC} = 4.5 , \text{V} )</td>
<td>17</td>
<td>30</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( V_{CC} = 6.0 , \text{V} )</td>
<td>14</td>
<td>26</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CE to RC; see Fig. 11</td>
<td>( V_{CC} = 2.0 , \text{V} )</td>
<td>33</td>
<td>130</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( V_{CC} = 4.5 , \text{V} )</td>
<td>12</td>
<td>26</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( V_{CC} = 6.0 , \text{V} )</td>
<td>10</td>
<td>22</td>
<td>-</td>
</tr>
<tr>
<td>( t_{tr} )</td>
<td>transition time</td>
<td>Dn to Qn; see Fig. 12</td>
<td>( V_{CC} = 2.0 , \text{V} )</td>
<td>61</td>
<td>220</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( V_{CC} = 4.5 , \text{V} )</td>
<td>22</td>
<td>44</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( V_{CC} = 6.0 , \text{V} )</td>
<td>18</td>
<td>37</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PE to Qn; see Fig. 13</td>
<td>( V_{CC} = 2.0 , \text{V} )</td>
<td>61</td>
<td>220</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( V_{CC} = 4.5 , \text{V} )</td>
<td>22</td>
<td>44</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( V_{CC} = 6.0 , \text{V} )</td>
<td>18</td>
<td>37</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( \bar{U}/D ) to TC; see Fig. 14</td>
<td>( V_{CC} = 2.0 , \text{V} )</td>
<td>44</td>
<td>190</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
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## Presetable synchronous 4-bit binary up/down counter

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<tr>
<td>t(_{\text{rec}})</td>
<td>recovery time</td>
<td>PL to CP; see Fig. 15</td>
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<td>set-up time</td>
<td>(\overline{U}/D) to CP; see Fig. 16</td>
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<td>t(_{\text{h}})</td>
<td>hold time</td>
<td>(\overline{U}/D) to CP; see Fig. 16</td>
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<td>f(_{\text{max}})</td>
<td>maximum frequency</td>
<td>CP; see Fig. 10</td>
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Nexperia

74HC191

Presetable synchronous 4-bit binary up/down counter

<table>
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<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>25 °C</th>
<th>-40 °C to +85 °C</th>
<th>-40 °C to +125 °C</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>V_I = GND to V_CC; V_CC = 5 V; f_i = 1 MHz</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td></td>
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<tr>
<td>C_PD</td>
<td>power dissipation capacitance</td>
<td>[3]</td>
<td>0</td>
<td>31</td>
<td>-</td>
<td>pF</td>
</tr>
</tbody>
</table>

[1] $t_{pd}$ is the same as $t_{PHL}$ and $t_{PLH}$.
[2] $t_{t}$ is the same as $t_{THL}$ and $t_{TLH}$.
[3] $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in $\mu$W):

$$P_D = C_{PD} \times V_CC^2 \times f_i \times N + \sum(C_L \times V_CC^2 \times f_o)$$

where:

- $f_i$ is input frequency in MHz;
- $f_o$ is output frequency in MHz;
- $C_L$ is output load capacitance in pF;
- $V_CC$ is supply voltage in V;
- $N$ is number of inputs switching;
- $\sum(C_L \times V_CC^2 \times f_o)$ is sum of outputs.

10.1. Waveforms and test circuit

![Waveform Diagram]

Measurement points are given in Table 9.
Logic levels $V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

Fig. 10. The clock input (CP) to outputs (Qn, TC) propagation delays, clock pulse width and maximum clock frequency

![Waveform Diagram]

Measurement points are given in Table 9.
Logic levels $V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

Fig. 11. The clock and count enable inputs (CP, CE) to ripple clock output (RC) propagation delays
Measurement points are given in Table 9.
Logic levels $V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

Fig. 12. The input (Dn) to output (Qn) propagation delays

Measurement points are given in Table 9.
Logic levels $V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

Fig. 13. The parallel load input (PL) to output (Qn) propagation delays

Measurement points are given in Table 9.
Logic levels $V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

Fig. 14. The up/down count input (U/D) to terminal count and ripple clock output (TC, RC) propagation delays
Presettable synchronous 4-bit binary up/down counter

Measurement points are given in Table 9.
Logic levels $V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

Fig. 15. The parallel load input (PL) to clock (CP) recovery times, parallel load pulse width and output (Qn) transition times

Measurement points are given in Table 9.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 16. The count enable and up/down count inputs (CE, U/D) to clock input (CP) set-up and hold times
Measurement points are given in Table 9.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 17. The parallel load input (PL) to data input (Dn) set-up and hold times

Table 9. Measurement points

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<thead>
<tr>
<th>Input</th>
<th>Output</th>
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<tr>
<td>VM</td>
<td>Vl</td>
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<tr>
<td>0.5 x VCC</td>
<td>GND to VCC</td>
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<tr>
<td>0.5 x VCC</td>
<td>0.5 x VCC</td>
</tr>
</tbody>
</table>

Test data is given in Table 10.
Test circuit definitions:
- RT = Termination resistance should be equal to output impedance Zo of the pulse generator
- CL = Load capacitance including jig and probe capacitance
- RL = Load resistance.
- S1 = Test selection switch

Fig. 18. Test circuit for measuring switching times

Table 10. Test data

<table>
<thead>
<tr>
<th>Input</th>
<th>Load</th>
<th>S1 position</th>
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<td>Vl</td>
<td>tᵣ, tᵣ</td>
<td>tᵩH, tᵩL</td>
</tr>
<tr>
<td>VCC</td>
<td>6 ns, 15 pF, 50 pF</td>
<td>1 kΩ, open</td>
</tr>
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11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

**Fig. 19. Package outline SOT109-1 (SO16)**

### Dimensions (inch dimensions are derived from the original mm dimensions)

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<th>A1</th>
<th>A2</th>
<th>A3</th>
<th>bP</th>
<th>c</th>
<th>D(1)</th>
<th>E(1)</th>
<th>e</th>
<th>H_E</th>
<th>L</th>
<th>L_p</th>
<th>Q</th>
<th>v</th>
<th>w</th>
<th>y</th>
<th>Z(1)</th>
<th>θ</th>
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<tbody>
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<td>1.45</td>
<td>1.25</td>
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<td>0.25</td>
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<td>4.0</td>
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**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

### Outline Version

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<th>REFERENCES</th>
<th>EUROPEAN PROJECTION</th>
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<td>JEDEC MS-012</td>
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</table>

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Presettable synchronous 4-bit binary up/down counter

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

**DIMENSIONS (mm are the original dimensions)**

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<tr>
<th>UNIT</th>
<th>A_{max}</th>
<th>A_1</th>
<th>A_2</th>
<th>A_3</th>
<th>b_p</th>
<th>c</th>
<th>D^{(1)}</th>
<th>E^{(2)}</th>
<th>e</th>
<th>H_E</th>
<th>L</th>
<th>L_p</th>
<th>Q</th>
<th>v</th>
<th>w</th>
<th>y</th>
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**Notes**
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

**OUTLINE VERSION**
- SOT403-1

**REFERENCES**
- IEC
- JEDEC
- JEITA

**EUROPEAN PROJECTION**

**ISSUE DATE**
- 06-12-27
- 03-02-18

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Fig. 20. Package outline SOT403-1 (TSSOP16)
12. Abbreviations

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<td>CMOS</td>
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<td>DUT</td>
<td>Device Under Test</td>
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<td>ESD</td>
<td>ElectroStatic Discharge</td>
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<td>HBM</td>
<td>Human Body Model</td>
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<td>MM</td>
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13. Revision history

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<td>19901201</td>
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