



74AXP1T45

1-bit dual supply translating transceiver; 3-state

Rev. 2.1 — 25 July 2024

Product data sheet

1. General description

The 74AXP1T45 is a single bit, dual supply transceiver with 3-state output that enables bidirectional level translation. It features two 1-bit input-output ports (A and B), a direction control input (DIR) and dual supply pins ($V_{CC(A)}$ and $V_{CC(B)}$). Both $V_{CC(A)}$ and $V_{CC(B)}$ can be supplied at any voltage between 0.9 V and 5.5 V making the device suitable for translating between any of the low voltage nodes (0.9 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V and 5.0 V). No power supply sequencing is required and output glitches during power supply transitions are prevented using patented circuitry. As a result glitches will not appear on the outputs for supply transitions during power-up/down between 20 mV/ μ s and 5.5 V/s. Pins A and DIR are referenced to $V_{CC(A)}$ and pin B is referenced to $V_{CC(B)}$. A HIGH on DIR allows transmission from A to B and a LOW on DIR allows transmission from B to A.

The device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing any damaging backflow current through the device when it is powered down. In suspend mode when either $V_{CC(A)}$ or $V_{CC(B)}$ are at GND level, both A and B are in the high-impedance OFF-state.

2. Features and benefits

- Wide supply voltage range:
 - $V_{CC(A)}$: 0.9 V to 5.5 V
 - $V_{CC(B)}$: 0.9 V to 5.5 V
- Low input capacitance; $C_I = 1.5$ pF (typical)
- Low output capacitance; $C_O = 3.8$ pF (typical)
- Low dynamic power consumption; $C_{PD} = 11$ pF (typical)
- Low static power consumption; $I_{CC} = 2$ μ A (25 °C maximum)
- High noise immunity
- Complies with JEDEC standard:
 - JESD8-12 (1.1 V to 1.3 V; inputs)
 - JESD8-11 (1.4 V to 1.6 V)
 - JESD8-7 (1.65 V to 1.95 V)
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8C (2.7 V to 3.6 V)
 - JESD12-6 (4.5 V to 5.5 V)
- Latch-up performance exceeds 100 mA per JESD78D Class II
- Inputs accept voltages up to 5.5 V
- Low noise overshoot and undershoot < 10% of V_{CCO}
- I_{OFF} circuitry provides partial power-down mode operation
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AXP1T45GW	-40 °C to +125 °C	TSSOP6	plastic thin shrink small outline package; 6 leads; body width 1.25 mm	SOT363-2
74AXP1T45GX	-40 °C to +125 °C	X2SON6	plastic thermal enhanced extremely thin small outline package; no leads; 6 terminals; body 1.0 × 0.8 × 0.32 mm	SOT1255-2

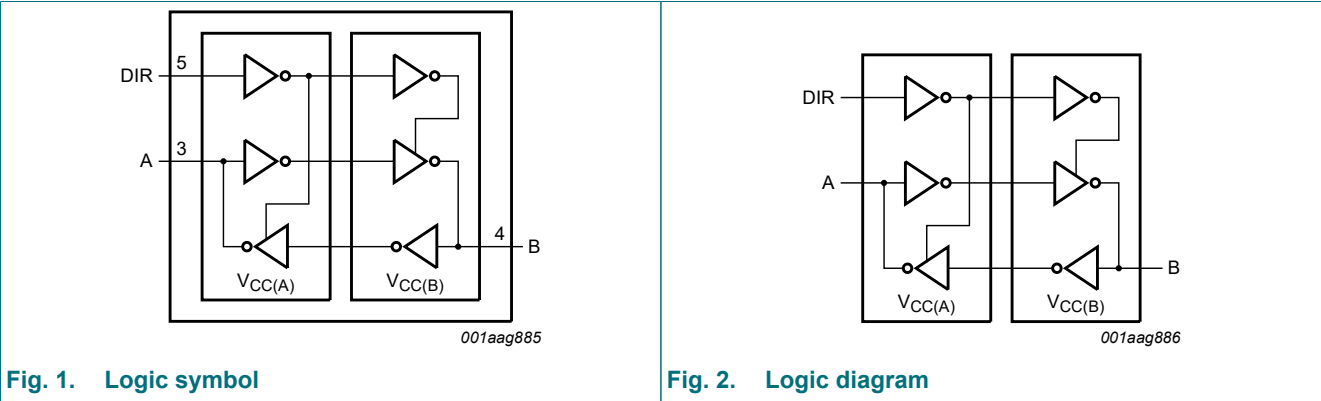
4. Marking

Table 2. Marking

Type number	Marking code [1]
74AXP1T45GW	R5
74AXP1T45GX	R5

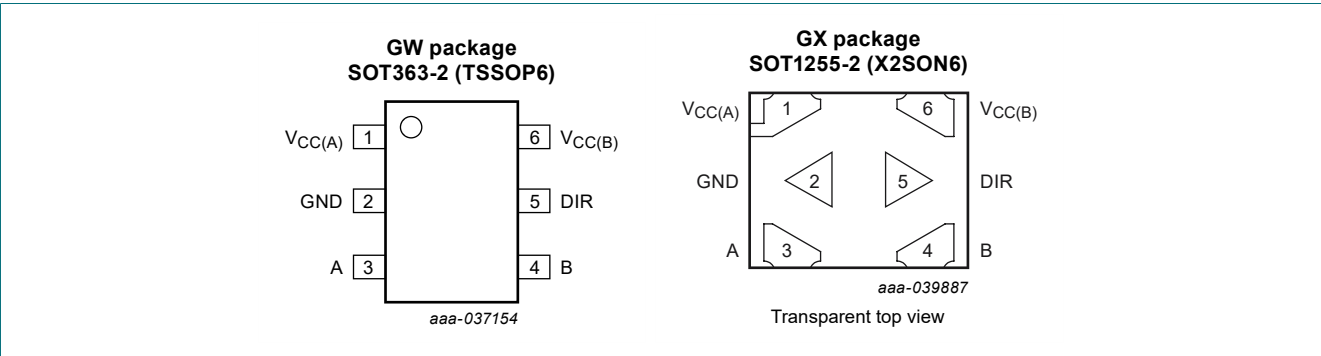
[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram



6. Pinning information

6.1. Pinning



6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
V _{CC(A)}	1	supply voltage A (A and DIR are referenced to V _{CC(A)})
GND	2	ground (0 V)
A	3	data input or output
B	4	data input or output
DIR	5	direction control
V _{CC(B)}	6	supply voltage B (B is referenced to V _{CC(B)})

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Supply voltage	Input	Input/output [1]	
V _{CC(A)} , V _{CC(B)}	DIR [2]	A [2]	B [2]
0.9 V to 5.5 V	L	A = B	input
0.9 V to 5.5 V	H	input	B = A
GND [1]	X	Z	Z

- [1] If at least one of V_{CC(A)} or V_{CC(B)} is at GND level, the device goes into suspend mode.
[2] A and DIR are referenced to V_{CC(A)}; B is referenced to V_{CC(B)}.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC(A)}	supply voltage A		-0.5	+6.5	V
V _{CC(B)}	supply voltage B		-0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0 V	-20	-	mA
V _I	input voltage	[1]	-0.5	+6.5	V
I _{OK}	output clamping current	V _O < 0 V	-20	-	mA
V _O	output voltage	Active mode [1][2][3]	-0.5	V _{CCO} + 0.5	V
		Suspend or 3-state mode [1]	-0.5	+6.5	V
I _O	output current	V _O = 0 V to V _{CCO} [2]	-	±25	mA
I _{CC}	supply current	I _{CC(A)} or I _{CC(B)} ; per V _{CC} pin	-	100	mA
I _{GND}	ground current	per GND pin	-100	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C [4]	-	250	mW

- [1] The minimum input voltage ratings and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] V_{CCO} is the supply voltage associated with the output port.
[3] V_{CCO} + 0.5 V should not exceed 6.5 V.
[4] For SOT363-2 (TSSOP6) package: P_{tot} derates linearly with 3.7 mW/K above 83 °C.
For SOT1255-2 (X2SON6) package: P_{tot} derates linearly with 3.3 mW/K above 75 °C.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC(A)}	supply voltage A		0.9	5.5	V
V _{CC(B)}	supply voltage B		0.9	5.5	V
V _I	input voltage		0	5.5	V
V _O	output voltage	Active mode [1]	0	V _{CCO}	V
		Suspend or 3-state mode	0	5.5	V
T _{amb}	ambient temperature		-40	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CCI} = 0.9 V [2]	-	20	ns/V
		V _{CCI} = 1.2 V	-	20	ns/V
		V _{CCI} = 1.4 V to 1.95 V	-	20	ns/V
		V _{CCI} = 2.3 V to 2.7 V	-	20	ns/V
		V _{CCI} = 3.0 V to 3.6 V	-	10	ns/V
		V _{CCI} = 4.5 V to 5.5 V	-	8	ns/V

[1] V_{CCO} is the supply voltage associated with the output port.
[2] V_{CCI} is the supply voltage associated with the input port.

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	+25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V _{IH}	HIGH-level input voltage	A, B and DIR input [1]								
		V _{CCI} = 0.9 V	0.7 × V _{CCI}	-	-	0.7 × V _{CCI}	-	0.7 × V _{CCI}	-	V
		V _{CCI} = 1.1 V to 1.95 V	0.65 × V _{CCI}	-	-	0.65 × V _{CCI}	-	0.65 × V _{CCI}	-	V
		V _{CCI} = 2.3 V to 2.7 V	1.6	-	-	1.6	-	1.6	-	V
		V _{CCI} = 3.0 V to 3.6 V	2.0	-	-	2.0	-	2.0	-	V
		V _{CCI} = 4.5 V to 5.5 V	0.7 × V _{CCI}	-	-	0.7 × V _{CCI}	-	0.7 × V _{CCI}	-	V
V _{IL}	LOW-level input voltage	A, B and DIR input [1]								
		V _{CCI} = 0.9 V	-	-	0.3 × V _{CCI}	-	0.3 × V _{CCI}	-	0.3 × V _{CCI}	V
		V _{CCI} = 1.1 V to 1.95 V	-	-	0.35 × V _{CCI}	-	0.35 × V _{CCI}	-	0.35 × V _{CCI}	V
		V _{CCI} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	-	0.7	V
		V _{CCI} = 3.0 V to 3.6 V	-	-	0.8	-	0.8	-	0.8	V
		V _{CCI} = 4.5 V to 5.5 V	-	-	0.3 × V _{CCI}	-	0.3 × V _{CCI}	-	0.3 × V _{CCI}	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} [2]								
		I _O = -0.1 mA; V _{CCO} = 0.9 V to 5.5 V [3]	V _{CCO} - 0.1	0.9	-	V _{CCO} - 0.1	-	V _{CCO} - 0.1	-	V
		I _O = -1.5 mA; V _{CCO} = 1.1 V	0.825	-	-	0.825	-	0.825	-	V
		I _O = -3 mA; V _{CCO} = 1.4 V	1.05	-	-	1.05	-	1.05	-	V
		I _O = -4.5 mA; V _{CCO} = 1.65 V	1.2	-	-	1.2	-	1.2	-	V
		I _O = -8 mA; V _{CCO} = 2.3 V	1.7	-	-	1.7	-	1.7	-	V
		I _O = -10 mA; V _{CCO} = 3.0 V	2.2	-	-	2.2	-	2.2	-	V
		I _O = -12 mA; V _{CCO} = 4.5 V	3.7	-	-	3.7	-	3.7	-	V

1-bit dual supply translating transceiver; 3-state

Symbol	Parameter	Conditions	+25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V _{OL}	LOW-level output voltage	V _I = V _{IL} [2]								
		I _O = 0.1 mA; V _{CCO} = 0.9 V to 5.5 V [3]	-	0	0.1	-	0.1	-	0.1	V
		I _O = 1.5 mA; V _{CCO} = 1.1 V	-	-	0.275	-	0.275	-	0.275	V
		I _O = 3 mA; V _{CCO} = 1.4 V	-	-	0.35	-	0.35	-	0.35	V
		I _O = 4.5 mA; V _{CCO} = 1.65 V	-	-	0.45	-	0.45	-	0.45	V
		I _O = 8 mA; V _{CCO} = 2.3 V	-	-	0.7	-	0.7	-	0.7	V
		I _O = 10 mA; V _{CCO} = 3.0 V	-	-	0.8	-	0.8	-	0.8	V
		I _O = 8 mA; V _{CCO} = 4.5 V	-	-	0.5	-	0.5	-	0.5	V
		I _O = 12 mA; V _{CCO} = 4.5 V	-	-	0.8	-	0.8	-	0.8	V
I _I	input leakage current	DIR input; V _I = 0 V to 5.5 V; V _{CCI} = 0.9 V to 5.5 V	-	-	±0.1	-	±0.5	-	±1	µA
I _{OZ}	OFF-state output current	A or B port; V _O = 0 V or V _{CCO} ; V _{CCO} = 0.9 V to 5.5 V [2]	-	-	±0.1	-	±0.5	-	±2	µA
		suspend mode A port; V _O = 0 V or V _{CCO} ; V _{CC(A)} = 5.5 V; V _{CC(B)} = 0 V [2]	-	-	±0.1	-	±0.5	-	±2	µA
		suspend mode B port; V _O = 0 V or V _{CCO} ; V _{CC(A)} = 0 V; V _{CC(B)} = 5.5 V [2]	-	-	±0.1	-	±0.5	-	±2	µA
I _{OFF}	power-off leakage current	DIR input; V _I = 0 V to 5.5 V; V _{CC(A)} = 0 V; V _{CC(B)} = 0.9 V to 5.5 V	-	-	0.1	-	0.5	-	2	µA
		A port; V _I or V _O = 0 V to 5.5 V; V _{CC(A)} = 0 V; V _{CC(B)} = 0.9 V to 5.5 V	-	-	0.1	-	0.5	-	2	µA
		B port; V _I or V _O = 0 V to 5.5 V; V _{CC(B)} = 0 V; V _{CC(A)} = 0.9 V to 5.5 V	-	-	0.1	-	0.5	-	2	µA
ΔI _{OFF}	additional power-off leakage current	DIR input; V _I = 0 V or 5.5 V; V _{CC(A)} = 0 V to 0.1 V; V _{CC(B)} = 0.9 V to 5.5 V	-	-	±0.1	-	±0.5	-	±2	µA
		A port; V _O = 0 V or 5.5 V; V _{CC(A)} = 0 V to 0.1 V; V _{CC(B)} = 0.9 V to 5.5 V; V _I = 0 V or 5.5 V	-	-	±0.1	-	±0.5	-	±2	µA
		B port; V _O = 0 V or 5.5 V; V _{CC(B)} = 0 V to 0.1 V; V _{CC(A)} = 0.9 V to 5.5 V; V _I = 0 V or 5.5 V	-	-	±0.1	-	±0.5	-	±2	µA

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Symbol	Parameter	Conditions	+25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I _{CC}	supply current	A port; V _I = 0 V or V _{CCI} ; I _O = 0 A [1]								
		V _{CC(A)} , V _{CC(B)} = 0.9 V to 5.5 V	-	-	2	-	4	-	9	µA
		V _{CC(A)} = 5.5 V; V _{CC(B)} = 0 V	-	-	2	-	4	-	9	µA
		V _{CC(A)} = 0 V; V _{CC(B)} = 5.5 V	-	-	±0.1	-	±0.4	-	±1	µA
		B port; V _I = 0 V or V _{CCI} ; I _O = 0 A								
		V _{CC(A)} , V _{CC(B)} = 0.9 V to 5.5 V	-	-	2	-	4	-	9	µA
		V _{CC(B)} = 5.5 V; V _{CC(A)} = 0 V	-	-	2	-	4	-	9	µA
		V _{CC(B)} = 0 V; V _{CC(A)} = 5.5 V	-	-	±0.1		±0.4		±1	µA
ΔI _{CC}	additional supply current	per input; other pins at V _{CCI} or ground (0 V); I _O = 0 A; V _{CC(A)} , V _{CC(B)} = 4.5 V to 5.5 V; V _I = V _{CCI} - 0.6 V [4]	-	2	100	-	150	-	200	µA

[1] V_{CCI} is the supply voltage associated with the control input or input port.

[2] V_{CCO} is the supply voltage associated with the output port.

[3] Typical values for V_{OL} and V_{OH} are measured at V_{CCO} is 0.9 V.

[4] Typical values for ΔI_{CC} are measured at V_{CC(A)}, V_{CC(B)} = 5 V.

Table 8. Typical total supply current I_{CC(A)} at T_{amb} = 25 °C

Voltages are referenced to GND (ground = 0 V).

V _{CC(A)}	V _{CC(B)}								Unit
	0 V	0.9 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V	
0 V	0.00	0.01	0.01	0.01	0.01	0.01	0.01	0.01	µA
0.9 V	0.01	0.08	0.08	0.08	0.08	0.08	0.08	0.08	µA
1.2 V	0.01	0.10	0.10	0.10	0.10	0.10	0.10	0.10	µA
1.5 V	0.01	0.13	0.13	0.13	0.13	0.13	0.13	0.13	µA
1.8 V	0.01	0.16	0.16	0.16	0.16	0.16	0.16	0.16	µA
2.5 V	0.01	0.22	0.22	0.22	0.22	0.22	0.22	0.22	µA
3.3 V	0.01	0.29	0.29	0.29	0.29	0.29	0.29	0.29	µA
5.0 V	0.01	0.44	0.44	0.44	0.44	0.44	0.44	0.44	µA

Table 9. Typical total supply current $I_{CC(B)}$ at $T_{amb} = 25\text{ °C}$
Voltages are referenced to GND (ground = 0 V).

V _{CC(A)}	V _{CC(B)}								Unit
	0 V	0.9 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V	
0 V	0.00	0.01	0.01	0.01	0.01	0.01	0.01	0.01	μA
0.9 V	0.01	0.08	0.10	0.13	0.16	0.22	0.29	0.44	μA
1.2 V	0.01	0.08	0.10	0.13	0.16	0.22	0.29	0.44	μA
1.5 V	0.01	0.08	0.10	0.13	0.16	0.22	0.29	0.44	μA
1.8 V	0.01	0.08	0.10	0.13	0.16	0.22	0.29	0.44	μA
2.5 V	0.01	0.08	0.10	0.13	0.16	0.22	0.29	0.44	μA
3.3 V	0.01	0.08	0.10	0.13	0.16	0.22	0.29	0.44	μA
5.0 V	0.01	0.08	0.10	0.13	0.16	0.22	0.29	0.44	μA

11. Dynamic characteristics

Table 10. Typical dynamic characteristics at $V_{CC(A)} = 0.9\text{ V}$ and $T_{amb} = 25\text{ }^{\circ}\text{C}$

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5; for waveforms see Fig. 3 and Fig. 4.

Symbol	Parameter	Conditions	$V_{CC(B)}$							Unit
			0.9 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V	
t_{pd}	propagation delay	A to B [1]	40	22	18.5	16.5	15	15	15	ns
		B to A [1]	40	33	32	31	31	31	32	ns
t_{dis}	disable time	DIR to A [1]	34	34	34	34	34	34	34	ns
		DIR to B [1]	42	30	26	26	24	25	23	ns
t_{en}	enable time	DIR to A [1]	82	63	58	57	55	56	55	ns
		DIR to B [1]	74	56	53	51	49	49	49	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL} ; t_{dis} is the same as t_{PLZ} and t_{PHZ} ; t_{en} is the same as t_{PZL} and t_{PZH} .

Table 11. Typical dynamic characteristics at $V_{CC(B)} = 0.9\text{ V}$ and $T_{amb} = 25\text{ }^{\circ}\text{C}$

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5; for waveforms see Fig. 3 and Fig. 4.

Symbol	Parameter	Conditions	$V_{CC(A)}$							Unit
			0.9 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V	
t_{pd}	propagation delay	A to B [1]	40	33	32	31	31	31	32	ns
		B to A [1]	40	22	18.5	16.5	15	15	15	ns
t_{dis}	disable time	DIR to A [1]	34	16	11	10	7.0	7.7	5.3	ns
		DIR to B [1]	42	31	28	28	27	27	27	ns
t_{en}	enable time	DIR to A [1]	82	53	47	45	42	42	42	ns
		DIR to B [1]	74	49	43	41	38	39	37	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL} ; t_{dis} is the same as t_{PLZ} and t_{PHZ} ; t_{en} is the same as t_{PZL} and t_{PZH} .

Table 12. Typical dynamic characteristics at $T_{amb} = 25\text{ }^{\circ}\text{C}$

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5.

Symbol	Parameter	Conditions	$V_{CC(A)}$ and $V_{CC(B)}$							Unit
			0.9 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V	
C_{PD}	power dissipation capacitance	A port: (direction A to B); [1]	1.5	1.6	1.7	1.7	1.9	2.1	2.7	pF
		B port: (direction B to A) [2]								
		A port: (direction B to A); [1] B port: (direction A to B) [2]	10	10.4	10.6	10.7	10.9	11.3	12.1	pF
C_I	input capacitance	$V_I = 0\text{ V}$ or V_{CCI} ; $V_{CCI} = 0\text{ V}$ to 5.5 V	1.9	1.9	1.9	1.9	1.9	1.9	1.9	pF
$C_{I/O}$	input/output capacitance	$V_O = 0\text{ V}$; $V_{CCO} = 0\text{ V}$	4.5	4.5	4.5	4.5	4.5	4.5	4.5	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[2] $f_i = 1\text{ MHz}$; $V_I = \text{GND to } V_{CC}$; $t_r = t_f = 1\text{ ns}$; $C_L = 0\text{ pF}$; $R_L = \infty\text{ }\Omega$.

Table 13. Dynamic characteristics for temperature range -40 °C to +85 °C

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5; for waveforms see Fig. 3 and Fig. 4.

Symbol	Parameter	Conditions	V _{CC(B)}												Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t _{pd}	propagation delay	A to B [1]													
		V _{CC(A)} = 1.2 V ± 0.1 V	4.0	38	3.6	25	3.4	21	3.1	16	2.9	14.5	2.7	14.5	ns
		V _{CC(A)} = 1.5 V ± 0.1 V	3.5	33	3.0	21	2.8	16.5	2.6	12.5	2.4	10.5	2.2	9.8	ns
		V _{CC(A)} = 1.8 V ± 0.15 V	3.1	32	2.7	19	2.4	15	2.2	11	2.1	9.0	1.9	8.2	ns
		V _{CC(A)} = 2.5 V ± 0.2 V	2.8	31	2.4	17.5	2.1	13.5	1.9	9.1	1.7	7.5	1.6	6.6	ns
		V _{CC(A)} = 3.3 V ± 0.3 V	2.7	31	2.3	17	2.0	13	1.8	8.5	1.6	6.9	1.4	5.8	ns
		V _{CC(A)} = 5.0 V ± 0.5 V	2.7	31	2.2	16.5	1.9	12.5	1.6	8.1	1.4	6.4	1.2	5.0	ns
		B to A													
		V _{CC(A)} = 1.2 V ± 0.1 V	4.0	38	3.5	33	3.1	32	2.8	31	2.7	31	2.7	31	ns
		V _{CC(A)} = 1.5 V ± 0.1 V	3.6	25	3.0	21	2.7	19	2.4	17.5	2.3	17	2.2	16.5	ns
		V _{CC(A)} = 1.8 V ± 0.15 V	3.4	21	2.8	16.5	2.4	15	2.1	13.5	2.0	13	1.9	12.5	ns
		V _{CC(A)} = 2.5 V ± 0.2 V	3.1	16	2.6	12.5	2.2	11	1.9	9.1	1.8	8.5	1.6	8.1	ns
		V _{CC(A)} = 3.3 V ± 0.3 V	2.9	14.5	2.4	10.5	2.1	9.0	1.7	7.5	1.6	6.9	1.4	6.4	ns
		V _{CC(A)} = 5.0 V ± 0.5 V	2.7	14.5	2.2	9.8	1.9	8.2	1.6	6.6	1.4	5.8	1.2	5.0	ns

Symbol	Parameter	Conditions	V _{CC(B)}												Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t _{en}	enable time	DIR to A [1]													
		V _{CC(A)} = 1.2 V ± 0.1 V	9.6	67.3	9.6	67.3	9.6	67.3	9.6	67.3	9.6	67.3	9.6	67.3	ns
		V _{CC(A)} = 1.5 V ± 0.1 V	7.4	37.5	7.4	37.5	7.4	37.5	7.4	37.5	7.4	37.5	7.4	37.5	ns
		V _{CC(A)} = 1.8 V ± 0.15 V	6.7	29	6.7	29	6.7	29	6.7	29	6.7	29	6.7	29	ns
		V _{CC(A)} = 2.5 V ± 0.2 V	4.9	19	4.9	19	4.9	19	4.9	19	4.9	19	4.9	19	ns
		V _{CC(A)} = 3.3 V ± 0.3 V	5.3	17.3	5.3	17.3	5.3	17.3	5.3	17.3	5.3	17.3	5.3	17.3	ns
		V _{CC(A)} = 5.0 V ± 0.5 V	3.7	12	3.7	12	3.7	12	3.7	12	3.7	12	3.7	12	ns
		DIR to B													
		V _{CC(A)} = 1.2 V ± 0.1 V	8.9	58.3	8.5	49.3	8.3	47	8.0	45.8	7.8	45	7.6	44.7	ns
		V _{CC(A)} = 1.5 V ± 0.1 V	7.4	45.2	6.9	32.5	6.7	29.8	6.5	27.2	6.3	26.6	6.1	26	ns
		V _{CC(A)} = 1.8 V ± 0.15 V	7.1	42	6.7	28.9	6.4	26.2	6.2	23.9	6.1	23	5.9	22.5	ns
		V _{CC(A)} = 2.5 V ± 0.2 V	5.7	37	5.3	25	5.0	22.5	4.8	20.1	4.6	19	4.5	18.4	ns
		V _{CC(A)} = 3.3 V ± 0.3 V	6.2	37.2	5.8	23.8	5.5	21.2	5.3	18.6	5.1	17.7	4.9	17.1	ns
		V _{CC(A)} = 5.0 V ± 0.5 V	5.1	33.7	4.6	21	4.3	18.2	4.0	15.7	3.8	14.6	3.6	13.9	ns

Symbol	Parameter	Conditions	V _{CC(B)}												Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t _{dis}	disable time	DIR to A [1]													
		V _{CC(A)} = 1.2 V ± 0.1 V	4.9	31	4.9	31	4.9	31	4.9	31	4.9	31	4.9	31	ns
		V _{CC(A)} = 1.5 V ± 0.1 V	3.9	17.8	3.9	17.8	3.9	17.8	3.9	17.8	3.9	17.8	3.9	17.8	ns
		V _{CC(A)} = 1.8 V ± 0.15 V	4.0	15.9	4.0	15.9	4.0	15.9	4.0	15.9	4.0	15.9	4.0	15.9	ns
		V _{CC(A)} = 2.5 V ± 0.2 V	2.9	12.9	2.9	12.9	2.9	12.9	2.9	12.9	2.9	12.9	2.9	12.9	ns
		V _{CC(A)} = 3.3 V ± 0.3 V	3.5	12.3	3.5	12.3	3.5	12.3	3.5	12.3	3.5	12.3	3.5	12.3	ns
		V _{CC(A)} = 5.0 V ± 0.5 V	2.4	9.6	2.4	9.6	2.4	9.6	2.4	9.6	2.4	9.6	2.4	9.6	ns
		DIR to B													
		V _{CC(A)} = 1.2 V ± 0.1 V	5.6	36.8	4.8	27.9	5.1	26.7	4.4	22.8	5.1	23.5	4.1	20.7	ns
		V _{CC(A)} = 1.5 V ± 0.1 V	5.1	32.3	4.4	23.1	4.6	21.8	3.8	17.6	4.6	18.5	3.6	15.8	ns
		V _{CC(A)} = 1.8 V ± 0.15 V	4.7	30.9	4.0	21.5	4.3	20	3.4	16	4.2	15.5	3.3	13.2	ns
		V _{CC(A)} = 2.5 V ± 0.2 V	4.3	29	3.6	20	3.9	17.7	3.0	14	3.9	14.3	2.9	10.7	ns
		V _{CC(A)} = 3.3 V ± 0.3 V	4.2	28.9	3.5	19	3.7	16.7	2.9	12.6	3.7	13	2.7	10.3	ns
		V _{CC(A)} = 5.0 V ± 0.5 V	4.1	27.8	3.3	18.9	3.6	16.5	2.7	12.4	3.5	12.4	2.5	9.4	ns
t _t	transition time	A, B output													
		V _{CC(A)} = 1.1 V to 5.5 V	1.0	-	1.0	-	1.0	-	1.0	-	1.0	-	1.0	-	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.

Table 14. Dynamic characteristics for temperature range -40 °C to +125 °C
Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5; for waveforms see Fig. 3 and Fig. 4.

Symbol	Parameter	Conditions	V _{CC(B)}												Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t _{pd}	propagation delay	A to B [1]													
		V _{CC(A)} = 1.2 V ± 0.1 V	4.0	38	3.6	26	3.4	22	3.1	17	2.9	15	2.7	15	ns
		V _{CC(A)} = 1.5 V ± 0.1 V	3.5	33	3.0	22	2.8	17.5	2.6	13.5	2.4	11.5	2.2	10.5	ns
		V _{CC(A)} = 1.8 V ± 0.15 V	3.1	32	2.7	20	2.4	16	2.2	12	2.1	9.7	1.9	9.4	ns
		V _{CC(A)} = 2.5 V ± 0.2 V	2.8	31	2.4	18.5	2.1	14.5	1.9	9.8	1.7	8.1	1.6	7.1	ns
		V _{CC(A)} = 3.3 V ± 0.3 V	2.7	31	2.3	18	2.0	14	1.8	9.2	1.6	7.5	1.4	6.3	ns
		V _{CC(A)} = 5.0 V ± 0.5 V	2.7	31	2.2	17.5	1.9	13.5	1.6	8.8	1.4	6.9	1.2	5.5	ns
		B to A													
		V _{CC(A)} = 1.2 V ± 0.1 V	4.0	38	3.5	33	3.1	32	2.8	31	2.7	31	2.7	31	ns
		V _{CC(A)} = 1.5 V ± 0.1 V	3.6	26	3.0	22	2.7	20	2.4	18.5	2.3	18	2.2	17.5	ns
		V _{CC(A)} = 1.8 V ± 0.15 V	3.4	22	2.8	17.5	2.4	16	2.1	14.5	2.0	14	1.9	13.5	ns
		V _{CC(A)} = 2.5 V ± 0.2 V	3.1	17	2.6	13.5	2.2	12	1.9	9.8	1.8	9.2	1.6	8.8	ns
		V _{CC(A)} = 3.3 V ± 0.3 V	2.9	15	2.4	11.5	2.1	9.7	1.7	8.1	1.6	7.5	1.4	6.9	ns
		V _{CC(A)} = 5.0 V ± 0.5 V	2.7	15	2.2	10.5	1.9	9.4	1.6	7.1	1.4	6.3	1.2	5.5	ns

Symbol	Parameter	Conditions	V _{CC(B)}												Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t _{en}	enable time	DIR to A [1]													
		V _{CC(A)} = 1.2 V ± 0.1 V	9.6	67.6	9.6	67.6	9.6	67.6	9.6	67.6	9.6	67.6	9.6	67.6	ns
		V _{CC(A)} = 1.5 V ± 0.1 V	7.4	38	7.4	38	7.4	38	7.4	38	7.4	38	7.4	38	ns
		V _{CC(A)} = 1.8 V ± 0.15 V	6.7	30.2	6.7	30.2	6.7	30.2	6.7	30.2	6.7	30.2	6.7	30.2	ns
		V _{CC(A)} = 2.5 V ± 0.2 V	4.9	19.9	4.9	19.9	4.9	19.9	4.9	19.9	4.9	19.9	4.9	19.9	ns
		V _{CC(A)} = 3.3 V ± 0.3 V	5.3	17.9	5.3	17.9	5.3	17.9	5.3	17.9	5.3	17.9	5.3	17.9	ns
		V _{CC(A)} = 5.0 V ± 0.5 V	3.7	12.2	3.7	12.2	3.7	12.2	3.7	12.2	3.7	12.2	3.7	12.2	ns
		DIR to B													
		V _{CC(A)} = 1.2 V ± 0.1 V	8.9	58.6	8.5	49.8	8.3	47.3	8.0	46	7.8	45.5	7.6	44.9	ns
		V _{CC(A)} = 1.5 V ± 0.1 V	7.4	45.9	6.9	33.3	6.7	30	6.5	27.8	6.3	26.8	6.1	26.3	ns
		V _{CC(A)} = 1.8 V ± 0.15 V	7.1	42.5	6.7	30	6.4	27	6.2	24.5	6.1	24	5.9	23	ns
		V _{CC(A)} = 2.5 V ± 0.2 V	5.7	37.6	5.3	25.2	5.0	22.7	4.8	20.3	4.6	19.2	4.5	18.5	ns
		V _{CC(A)} = 3.3 V ± 0.3 V	6.2	37.5	5.8	24.8	5.5	21.5	5.3	18.9	5.1	18	4.9	17.3	ns
		V _{CC(A)} = 5.0 V ± 0.5 V	5.1	34.1	4.6	21.5	4.3	18.5	4.0	15.9	3.8	14.8	3.6	14	ns

Symbol	Parameter	Conditions	V _{CC(B)}												Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t _{dis}	disable time	DIR to A [1]													
		V _{CC(A)} = 1.2 V ± 0.1 V	4.9	31.2	4.9	31.2	4.9	31.2	4.9	31.2	4.9	31.2	4.9	31.2	ns
		V _{CC(A)} = 1.5 V ± 0.1 V	3.9	18	3.9	18	3.9	18	3.9	18	3.9	18	3.9	18	ns
		V _{CC(A)} = 1.8 V ± 0.15 V	4.0	16	4.0	16	4.0	16	4.0	16	4.0	16	4.0	16	ns
		V _{CC(A)} = 2.5 V ± 0.2 V	2.9	13	2.9	13	2.9	13	2.9	13	2.9	13	2.9	13	ns
		V _{CC(A)} = 3.3 V ± 0.3 V	3.5	12.4	3.5	12.4	3.5	12.4	3.5	12.4	3.5	12.4	3.5	12.4	ns
		V _{CC(A)} = 5.0 V ± 0.5 V	2.4	9.7	2.4	9.7	2.4	9.7	2.4	9.7	2.4	9.7	2.4	9.7	ns
		DIR to B													
		V _{CC(A)} = 1.2 V ± 0.1 V	5.6	37	4.8	28.3	5.1	27.1	4.4	23.2	5.1	23.8	4.1	21	ns
		V _{CC(A)} = 1.5 V ± 0.1 V	5.1	32.6	4.4	23.6	4.6	22	3.8	18	4.6	18.7	3.6	16	ns
		V _{CC(A)} = 1.8 V ± 0.15 V	4.7	31.1	4.0	22	4.3	20.1	3.4	16.1	4.2	15.6	3.3	13.4	ns
		V _{CC(A)} = 2.5 V ± 0.2 V	4.3	29.8	3.6	20.2	3.9	17.9	3.0	14.1	3.9	14.4	2.9	10.9	ns
		V _{CC(A)} = 3.3 V ± 0.3 V	4.2	29.1	3.5	19.1	3.7	16.9	2.9	12.9	3.7	13.1	2.7	10.4	ns
		V _{CC(A)} = 5.0 V ± 0.5 V	4.1	28	3.3	19	3.6	16.7	2.7	12.5	3.5	12.5	2.5	9.5	ns
t _t	transition time	A, B output													
		V _{CC(A)} = 1.1 V to 5.5 V	1.0	-	1.0	-	1.0	-	1.0	-	1.0	-	1.0	-	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.

11.1. Waveforms and test circuit

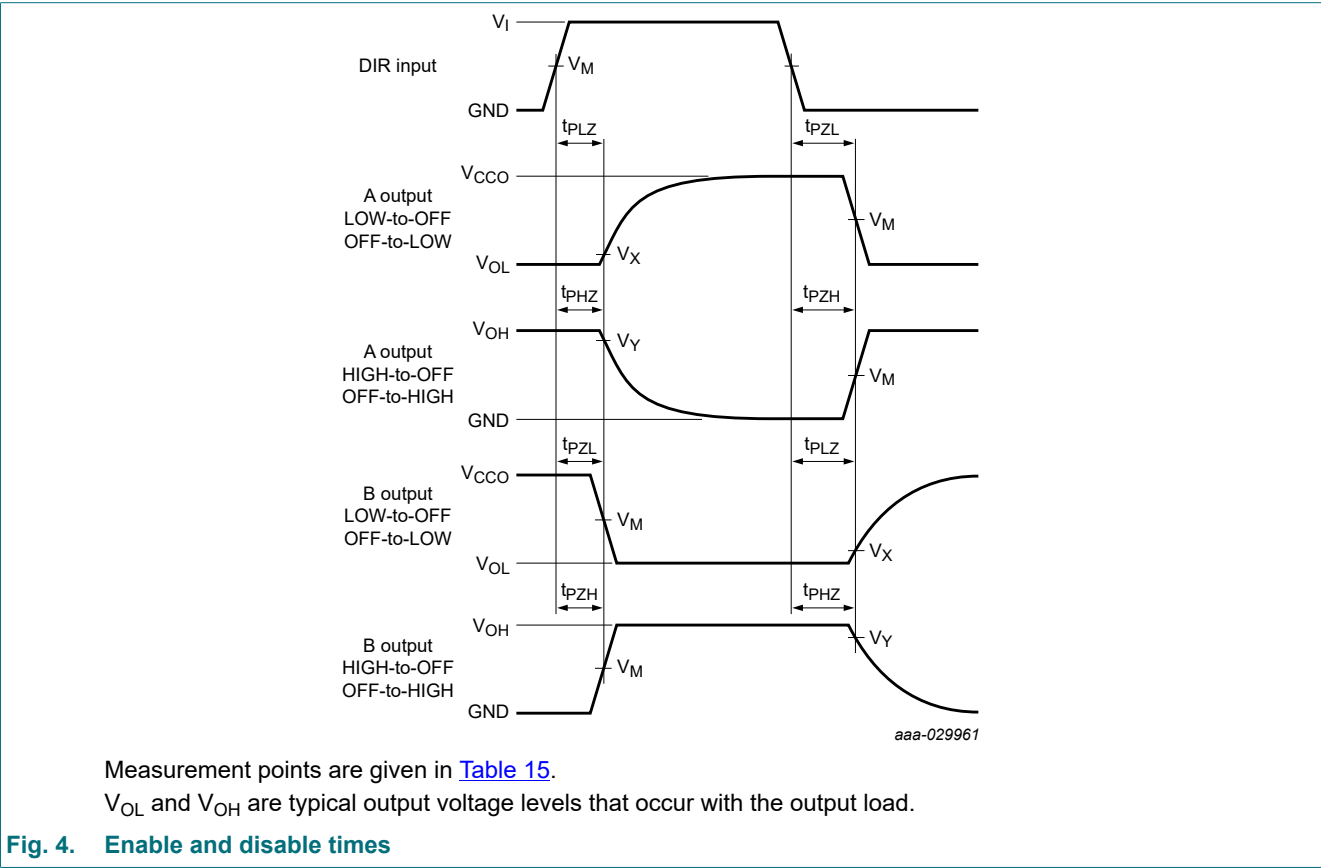
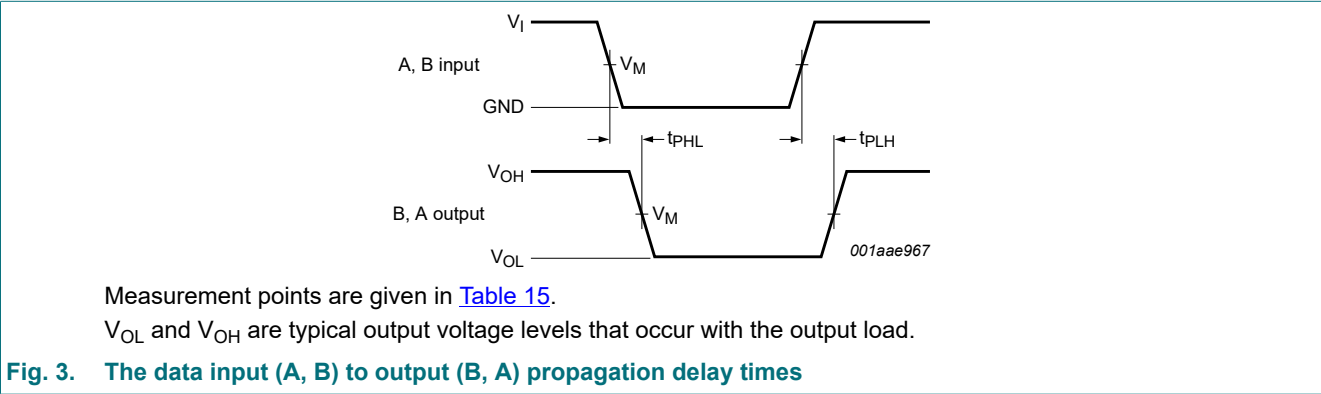
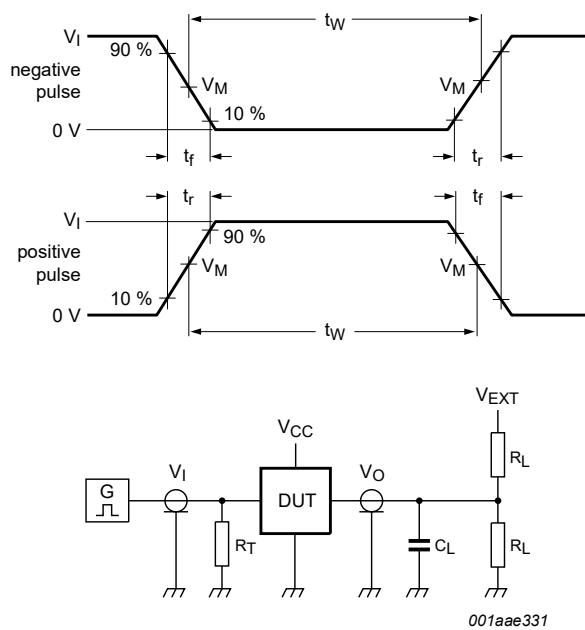


Table 15. Measurement points

Supply voltage	Input[1]	Output[2]		
$V_{CC(A)}, V_{CC(B)}$	V_M	V_M	V_X	V_Y
0.9 V to 1.6 V	$0.5 \times V_{CCI}$	$0.5 \times V_{CCO}$	$V_{OL} + 0.1\text{ V}$	$V_{OH} - 0.1\text{ V}$
1.65 V to 2.7 V	$0.5 \times V_{CCI}$	$0.5 \times V_{CCO}$	$V_{OL} + 0.15\text{ V}$	$V_{OH} - 0.15\text{ V}$
3.0 V to 5.5 V	$0.5 \times V_{CCI}$	$0.5 \times V_{CCO}$	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$

[1] V_{CCI} is the supply voltage associated with the control input or input port.
 [2] V_{CCO} is the supply voltage associated with the output port.



Test data is given in [Table 16](#).
Definitions test circuit:
 R_L = Load resistance;
 C_L = Load capacitance including jig and probe capacitance;
 R_T = Termination resistance;
 V_{EXT} = External voltage for measuring switching times.

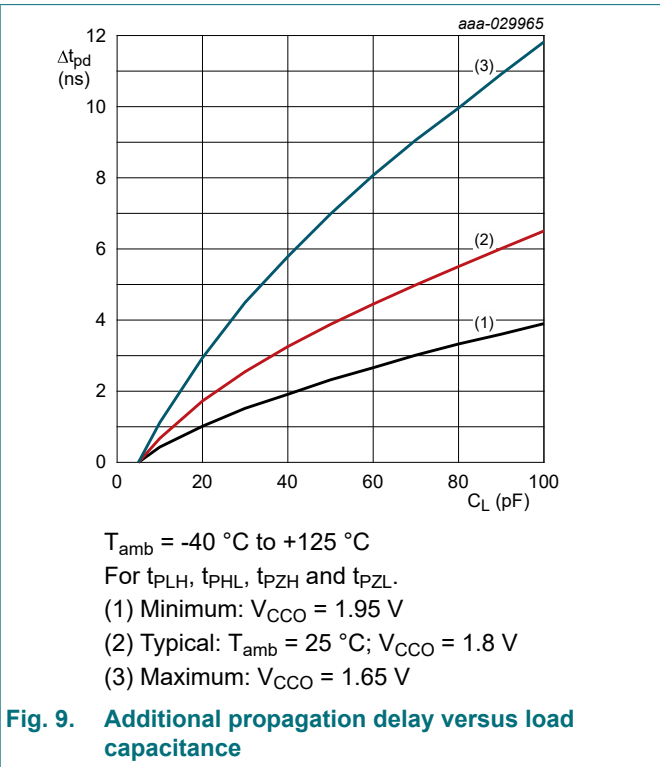
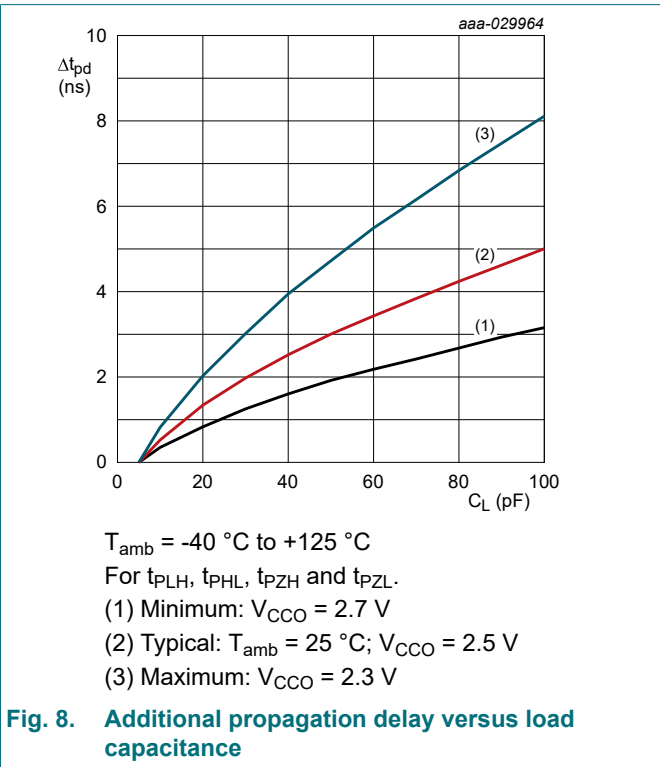
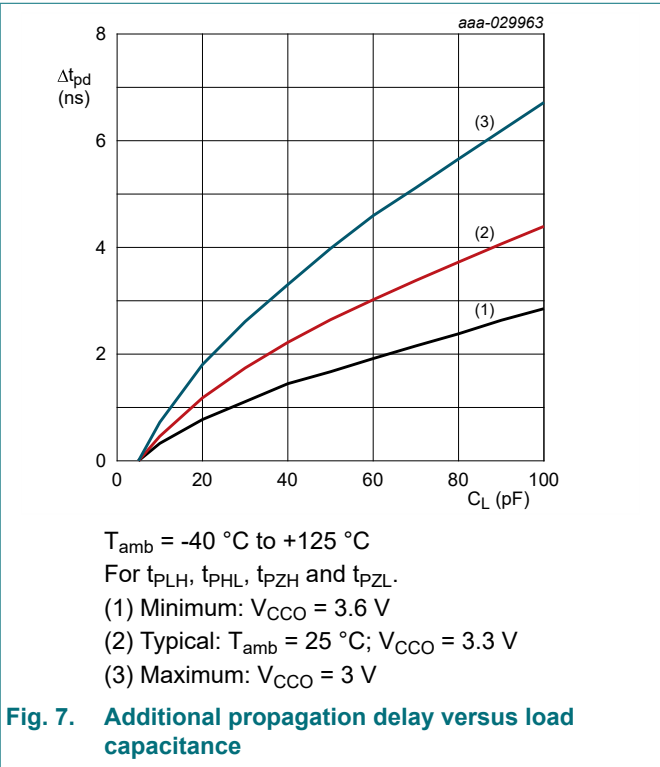
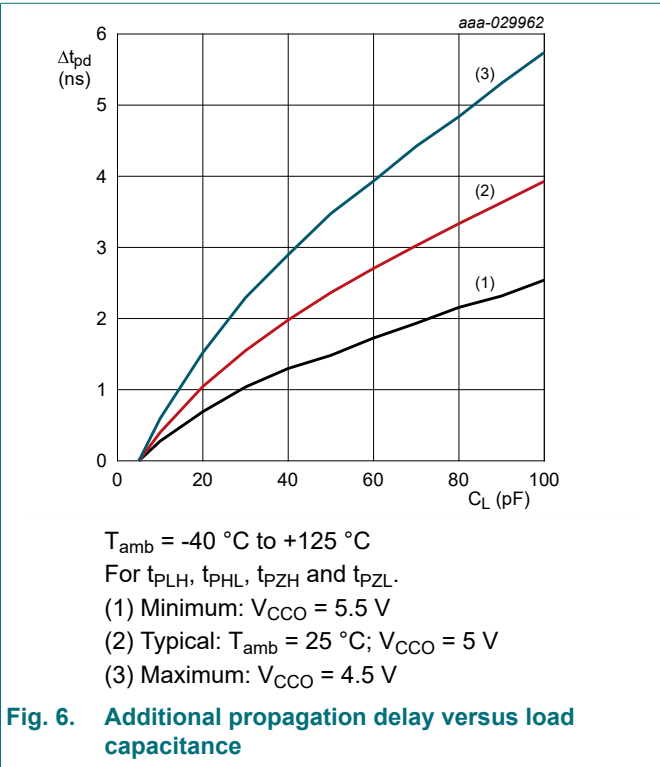
Fig. 5. Test circuit for measuring switching times

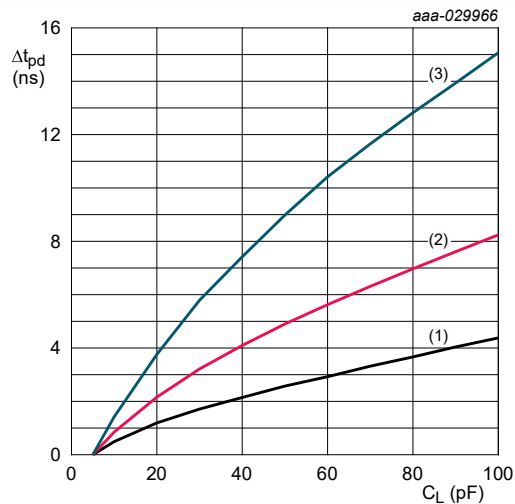
Table 16. Test data

Supply voltage	Load		Input		V_{EXT}		
$V_{CC(A)}, V_{CC(B)}$	C_L	R_L	t_r, t_f	V_I [1]	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ} [2]
0.9 V to 5.5 V	5 pF	10 k Ω	≤ 3.0 ns	V_{CCI}	GND	GND	$2 \times V_{CCO}$

[1] V_{CCI} is the supply voltage associated with the control input or input port.
[2] V_{CCO} is the supply voltage associated with the output port.

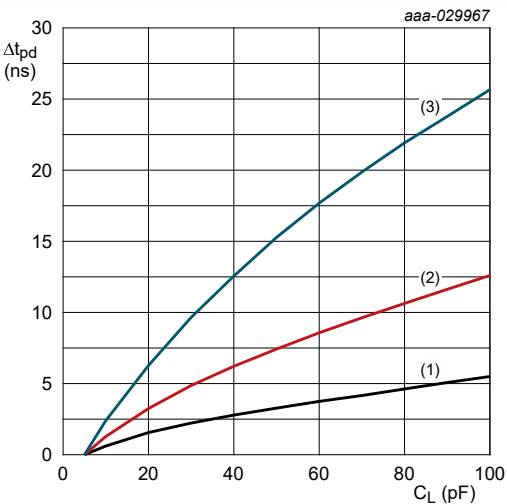
11.2. Additional propagation delay versus load capacitance graphs





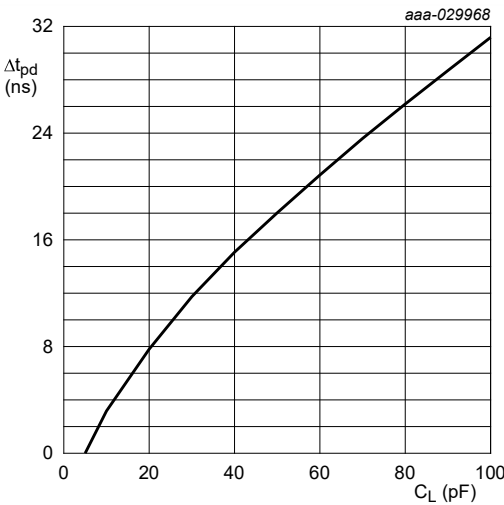
$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$
For t_{PLH} , t_{PHL} , t_{PZH} and t_{PZL} .
(1) Minimum: $V_{CCO} = 1.6\text{ V}$
(2) Typical: $T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{CCO} = 1.5\text{ V}$
(3) Maximum: $V_{CCO} = 1.4\text{ V}$

Fig. 10. Additional propagation delay versus load capacitance



$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$
For t_{PLH} , t_{PHL} , t_{PZH} and t_{PZL} .
(1) Minimum: $V_{CCO} = 1.3\text{ V}$
(2) Typical: $T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{CCO} = 1.2\text{ V}$
(3) Maximum: $V_{CCO} = 1.1\text{ V}$

Fig. 11. Additional propagation delay versus load capacitance



$T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{CCO} = 0.9\text{ V}$
For t_{PLH} , t_{PHL} , t_{PZH} and t_{PZL} .

Fig. 12. Additional propagation delay versus load capacitance

12. Application information

12.1. Unidirectional logic level-shifting application

The circuit given in Fig. 13 is an example of the 74AXP1T45 being used in an unidirectional logic level-shifting application.

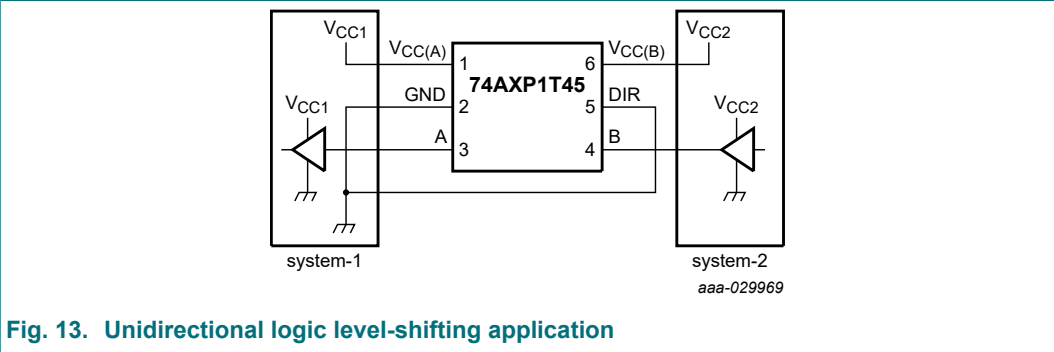


Table 17. Description unidirectional logic level-shifting application

Pin	Name	Function	Description
1	V _{CC(A)}	V _{CC1}	supply voltage of system-1 (0.9 V to 5.5 V)
2	GND	GND	device GND
3	A	OUT	output level depends on V _{CC1} voltage
4	B	IN	input threshold value depends on V _{CC2} voltage
5	DIR	DIR	the GND (LOW level) determines B port to A port direction
6	V _{CC(B)}	V _{CC2}	supply voltage of system-2 (0.9 V to 5.5 V)

12.2. Bidirectional logic level-shifting application

Fig. 14 shows the 74AXP1T45 being used in a bidirectional logic level-shifting application. Since the device does not have an output enable pin, the system designer should take precautions to avoid bus contention between system-1 and system-2 when changing directions.

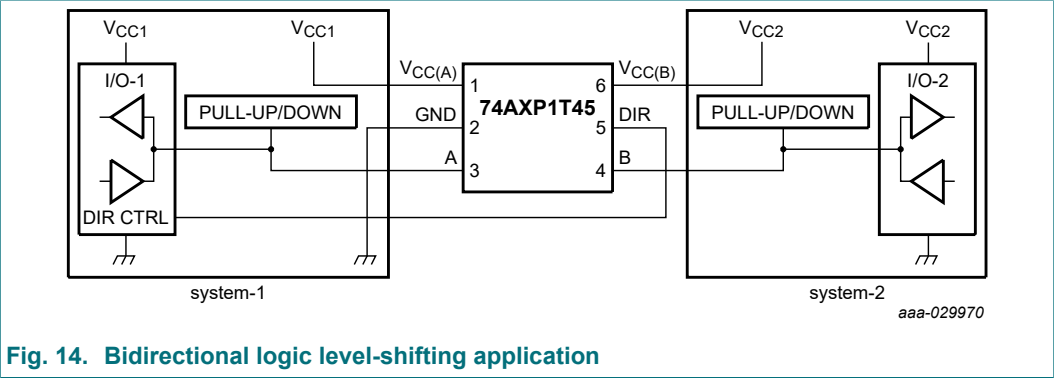


Fig. 14. Bidirectional logic level-shifting application

Table 18 gives a sequence that will illustrate data transmission from system-1 to system-2 and then from system-2 to system-1.

Table 18. Description bidirectional logic level-shifting application

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

State	DIR CTRL	I/O-1	I/O-2	Description
1	H	output	input	system-1 data to system-2
2	H	Z	Z	system-2 is getting ready to send data to system-1. I/O-1 and I/O-2 are disabled. The bus-line state depends on bus hold.
3	L	Z	Z	DIR bit is set LOW. I/O-1 and I/O-2 still are disabled. The bus-line state depends on bus hold.
4	L	input	output	system-2 data to system-1

12.3. Enable times

Calculate the enable times for the 74AXP1T45 using the following formulas:

- Direction A to B:
 - $t_{PZL} \text{ (DIR to B)} = t_{PHL} \text{ (A to B)} + t_{PHZ} \text{ (DIR to A)}$
 - $t_{PZH} \text{ (DIR to B)} = t_{PLH} \text{ (A to B)} + t_{PLZ} \text{ (DIR to A)}$
- Direction B to A:
 - $t_{PZL} \text{ (DIR to A)} = t_{PHL} \text{ (B to A)} + t_{PHZ} \text{ (DIR to B)}$
 - $t_{PZH} \text{ (DIR to A)} = t_{PLH} \text{ (B to A)} + t_{PLZ} \text{ (DIR to B)}$

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the 74AXP1T45 initially is transmitting from A to B, then the DIR bit is switched, the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

13. Package outline

TSSOP6: plastic thin shrink small outline package; 6 leads; body width 1.25 mm

SOT363-2

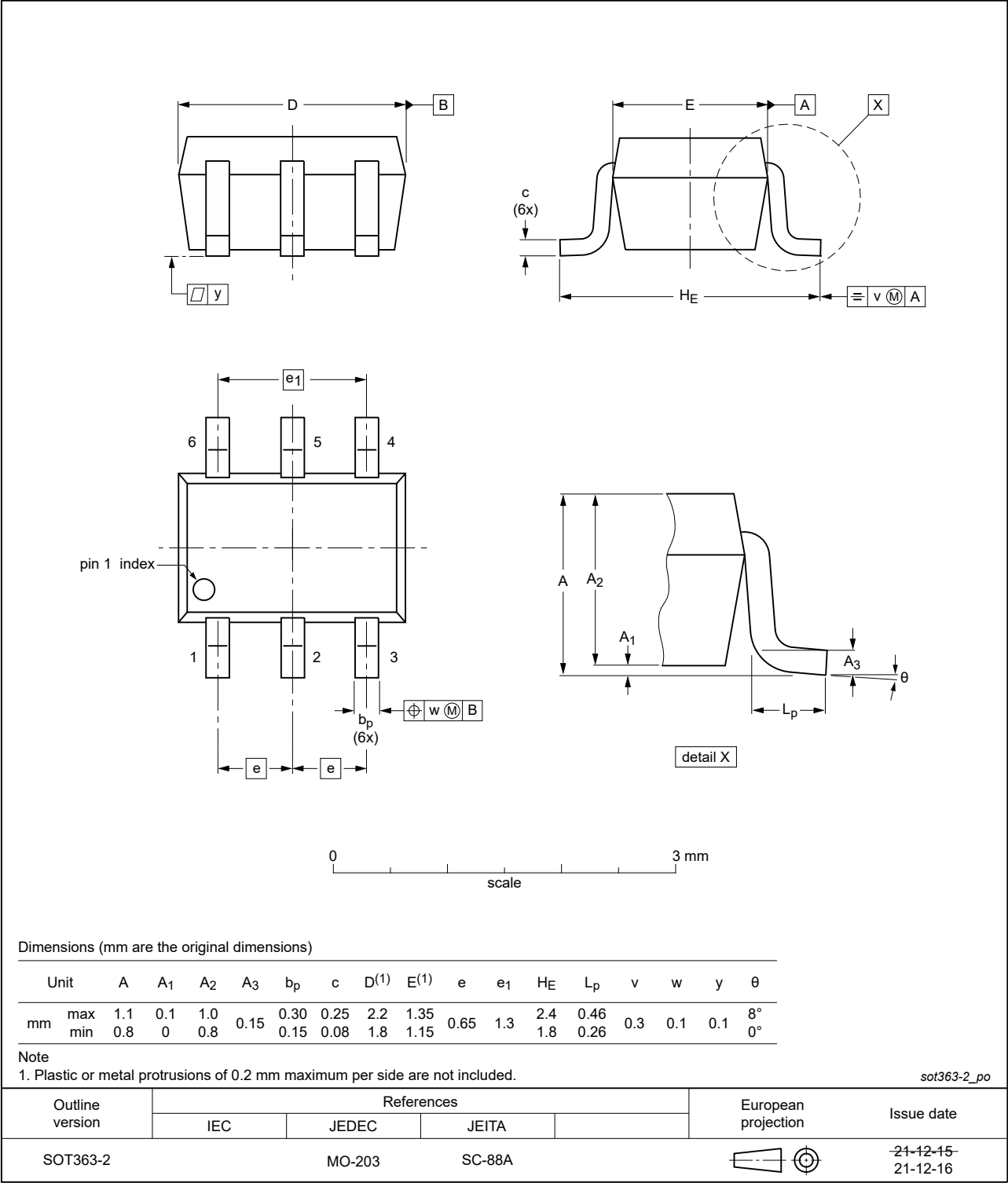


Fig. 15. Package outline SOT363-2 (TSSOP6)

X2SON6: plastic thermal enhanced extremely thin small outline package; no leads;
6 terminals; body 1.0 x 0.8 x 0.32 mm

SOT1255-2

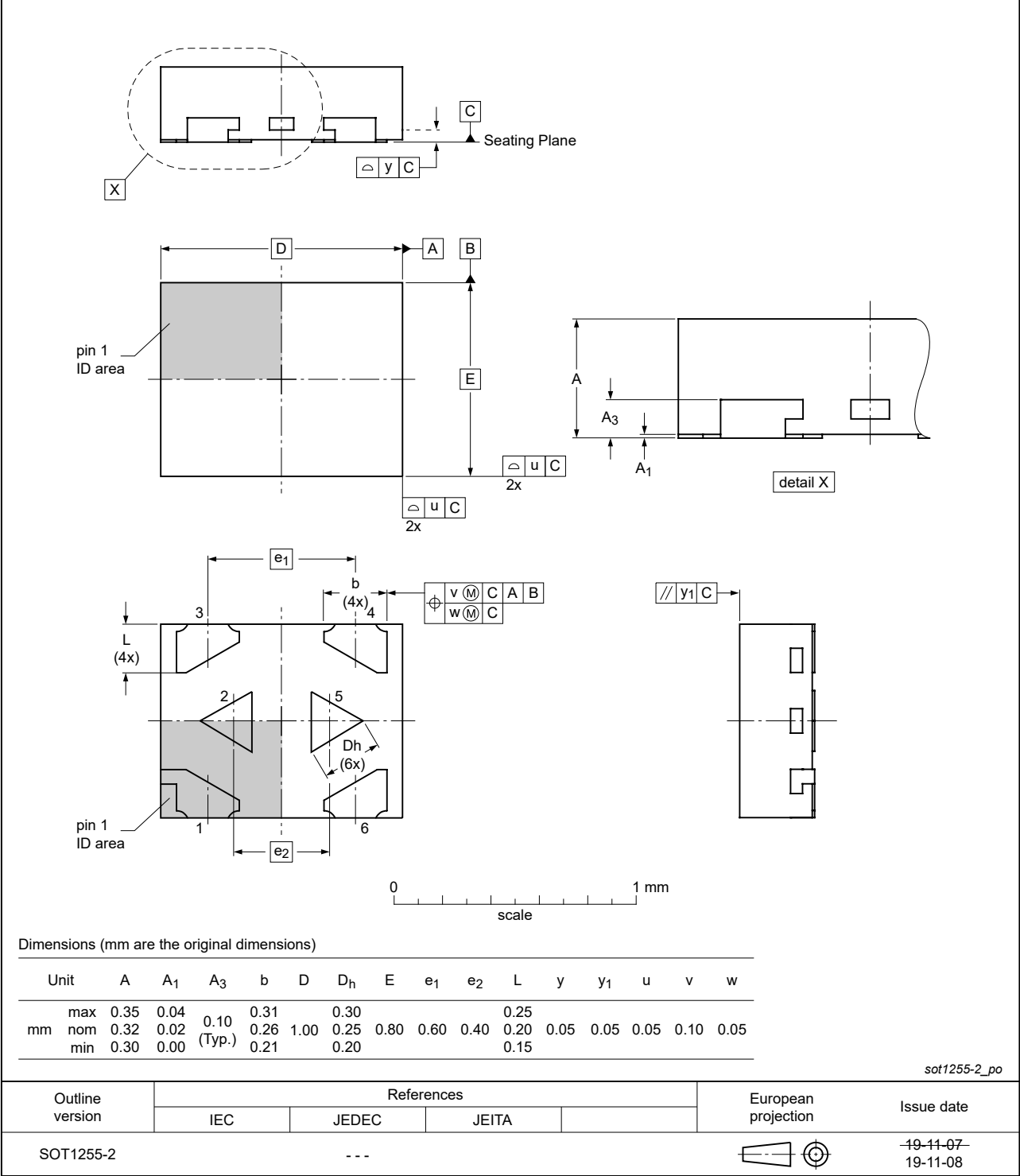


Fig. 16. Package outline SOT1255-2 (X2SON6)

14. Abbreviations

Table 19. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council

15. Revision history

Table 20. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AXP1T45 v.2.1	20240725	Product data sheet	-	74AXP1T45 v.2
74AXP1T45 v.2	20220203	Product data sheet	-	74AXP1T45 v.1
Modifications	• Package SOT363 (SC-88) changed to SOT363-2 (TSSOP6).			
74AXP1T45 v.1	20200625	Product data sheet	-	-

16. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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