74AVC1T1004

1-to-4 fan-out buffer

Rev. 3 — 25 June 2024

Product data sheet

1. General description

The 74AVC1T1004 is a translating 1-to-4 fan-out buffer suitable for use in clock distribution. It has dual supplies ($V_{CC(A)}$ and $V_{CC(B)}$) for voltage translation. It also has a data input (A), four data outputs (Yn) and an output enable input ($\overline{OE}$). $V_{CC(A)}$ and $V_{CC(B)}$ can be independently supplied at any voltage between 0.8 V and 3.6 V. It makes the device suitable for low voltage translation between any of the following voltages: 0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V. The levels of A and $\overline{OE}$ are referenced to $V_{CC(A)}$, outputs Yn are referenced to $V_{CC(B)}$. This supply configuration ensures that the fanned out signals can be used in level shifting. A HIGH on $\overline{OE}$ causes all outputs to be pulled LOW via pull-down resistors, a LOW on $\overline{OE}$ disconnects the pull-down resistors and enables all outputs.

Schmitt trigger action at all inputs makes the circuit tolerant for slower input rise and fall time.

The I_{OFF} circuitry disables the output, preventing any damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range:
  - $V_{CC(A)}$: 0.8 V to 3.6 V
  - $V_{CC(B)}$: 0.8 V to 3.6 V
- Complies with JEDEC standards:
  - JESD8-12 (0.8 V to 1.3 V)
  - JESD8-11 (0.9 V to 1.65 V)
  - JESD8-7 (1.2 V to 1.95 V)
  - JESD8-5 (1.8 V to 2.7 V)
  - JESD8-B (2.7 V to 3.6 V)
- Maximum data rates:
  - 380 Mbit/s (≥ 1.8 V to 3.3 V translation)
  - 200 Mbit/s (≥ 1.1 V to 3.3 V translation)
  - 200 Mbit/s (≥ 1.1 V to 2.5 V translation)
  - 200 Mbit/s (≥ 1.1 V to 1.8 V translation)
  - 150 Mbit/s (≥ 1.1 V to 1.5 V translation)
  - 100 Mbit/s (≥ 1.1 V to 1.2 V translation)
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Inputs accept voltages up to 3.6 V
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

nexperia

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AVC1T1004DP	-40 °C to +125 °C	TSSOP10	plastic thin shrink small outline package; 10 leads; body width 3 mm	SOT552-1

4. Marking

Table 2. Marking codes

Type number	Marking code
74AVC1T1004DP	Bc

5. Functional diagram

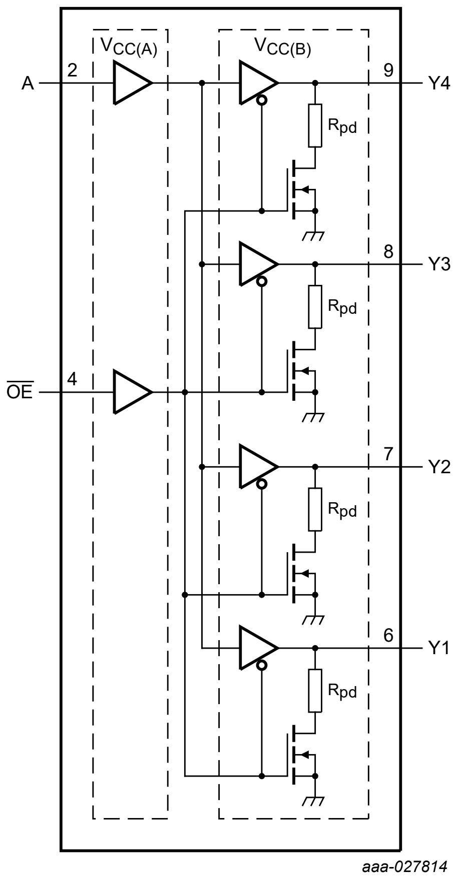


Fig. 1. Logic symbol

6. Pinning information

6.1. Pinning

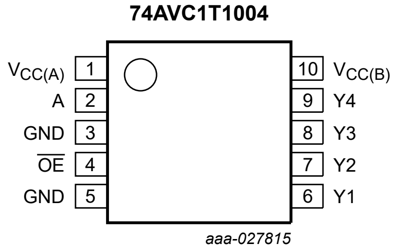


Fig. 2. Pin configuration SOT552-1 (TSSOP10)

6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
$V_{CC(A)}$	1	supply voltage A
A	2	data input (referenced to $V_{CC(A)}$)
GND[1]	3, 5	ground (0 V)
$\overline{OE}$	4	output enable input (active LOW) (referenced to $V_{CC(A)}$)
Y1, Y2, Y3, Y4	6, 7, 8, 9	data outputs (referenced to $V_{CC(B)}$)
$V_{CC(B)}$	10	supply voltage B

[1] All GND pins must be connected to ground (0 V).

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Inputs		Output
$\overline{OE}$	A	Yn
L	L	L
L	H	H
H	X	L

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{CC(A)}$	supply voltage A			-0.5	+4.6	V
$V_{CC(B)}$	supply voltage B			-0.5	+4.6	V
V_I	input voltage		[1]	-0.5	+4.6	V
V_O	output voltage	$\overline{OE}$ = LOW	[1] [2]	-0.5	$V_{CC(B)}$ + 0.5	V
		$\overline{OE}$ = HIGH	[1]	-0.5	+4.6	V
I_{IK}	input clamping current	V_I < 0 V		-50	-	mA
I_{OK}	output clamping current	V_O < 0 V		-50	-	mA
I_O	output current	V_O = 0 V to $V_{CC(B)}$		-	±50	mA
I_{CC}	supply current	$I_{CC(A)}$ or $I_{CC(B)}$		-	100	mA
I_{GND}	ground current			-100	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[3]	-	250	mW

[1] The minimum input voltage ratings and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] $V_{CC(B)}$ + 0.5 V should not exceed 4.6 V.
[3] For SOT552-1 (TSSOP10) packages: P_{tot} derates linearly with 8.3 mW/K above 120 °C.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		0.8	3.6	V
$V_{CC(B)}$	supply voltage B		0.8	3.6	V
V_I	input voltage		0	3.6	V
V_O	output voltage	$\overline{OE}$ = LOW	0	V_{CCB}	V
		$\overline{OE}$ = HIGH	0	3.6	V
T_{amb}	ambient temperature		-40	+125	°C
Δt/ΔV	input transition rise and fall rate	$V_{CC(A)}$ = 0.8 V to 3.6 V	0	200	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = 25 °C			Unit
			Min	Typ	Max	
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = -1.5 mA; $V_{CC(B)}$ = 0.8 V	-	0.69	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 1.5 mA; $V_{CC(B)}$ = 0.8 V	-	0.07	-	V
I_I	input leakage current	A, $\overline{OE}$ input; V_I = 0 V or 3.6 V; $V_{CC(A)} = V_{CC(B)}$ = 0.8 V to 3.6 V	-	±0.025	±0.25	μA
I_{OFF}	power-off leakage current	V_I or V_O = 0 V to 3.6 V; $V_{CC(A)}$ or $V_{CC(B)}$ = 0 V	-	±0.1	±1	μA
R_{pd}	pull-down resistance		-	50	-	kΩ
C_I	input capacitance	A, $\overline{OE}$ input; V_I = 0 V or 3.3 V; $V_{CC(A)}$ = 3.3 V	-	1.2	-	pF
C_O	output capacitance	Yn; V_O = 3.3 V or 0 V; $V_{CC(B)}$ = 3.3 V	-	4.7	-	pF

Table 8. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = -40 °C to +85 °C		T_{amb} = -40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	A, $\overline{OE}$ input					
		$V_{CC(A)}$ = 0.8 V	$0.70V_{CC(A)}$	-	$0.70V_{CC(A)}$	-	V
		$V_{CC(A)}$ = 1.1 V to 1.95 V	$0.65V_{CC(A)}$	-	$0.65V_{CC(A)}$	-	V
		$V_{CC(A)}$ = 2.3 V to 2.7 V	1.6	-	1.6	-	V
		$V_{CC(A)}$ = 3.0 V to 3.6 V	2	-	2	-	V
V_{IL}	LOW-level input voltage	A, $\overline{OE}$ input					
		$V_{CC(A)}$ = 0.8 V	-	$0.30V_{CC(A)}$	-	$0.30V_{CC(A)}$	V
		$V_{CC(A)}$ = 1.1 V to 1.95 V	-	$0.35V_{CC(A)}$	-	$0.35V_{CC(A)}$	V
		$V_{CC(A)}$ = 2.3 V to 2.7 V	-	0.7	-	0.7	V
		$V_{CC(A)}$ = 3.0 V to 3.6 V	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = -100 μA; $V_{CC(B)}$ = 0.8 V to 3.6 V	$V_{CC(B)}$ - 0.1	-	$V_{CC(B)}$ - 0.1	-	V
		I_O = -3 mA; $V_{CC(B)}$ = 1.1 V	0.85	-	0.85	-	V
		I_O = -6 mA; $V_{CC(B)}$ = 1.4 V	1.05	-	1.05	-	V
		I_O = -8 mA; $V_{CC(B)}$ = 1.65 V	1.2	-	1.2	-	V
		I_O = -9 mA; $V_{CC(B)}$ = 2.3 V	1.75	-	1.75	-	V
		I_O = -12 mA; $V_{CC(B)}$ = 3.0 V	2.3	-	2.3	-	V

Symbol	Parameter	Conditions	T_{amb} = -40 °C to +85 °C		T_{amb} = -40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = 100 μA; $V_{CC(B)}$ = 0.8 V to 3.6 V	-	0.1	-	0.1	V
		I_O = 3 mA; $V_{CC(B)}$ = 1.1 V	-	0.25	-	0.25	V
		I_O = 6 mA; $V_{CC(B)}$ = 1.4 V	-	0.35	-	0.35	V
		I_O = 8 mA; $V_{CC(B)}$ = 1.65 V	-	0.45	-	0.45	V
		I_O = 9 mA; $V_{CC(B)}$ = 2.3 V	-	0.55	-	0.55	V
		I_O = 12 mA; $V_{CC(B)}$ = 3.0 V	-	0.7	-	0.7	V
I_I	input leakage current	A, $\overline{OE}$ input; V_I = 0 V or 3.6 V; $V_{CC(A)} = V_{CC(B)}$ = 0.8 V to 3.6 V	-	±1	-	±5	μA
I_{OFF}	power-off leakage current	V_I or V_O = 0 V to 3.6 V; $V_{CC(B)}$ = 0 V; $V_{CC(A)}$ = 0.8 V to 3.6 V	-	±5	-	±30	μA
$I_{CC(A)}$	supply current A	V_I = 0 V or $V_{CC(A)}$; I_O = 0 A; $V_{CC(A)}$ = 0.8 V to 3.6 V; $V_{CC(B)}$ = 0.8 V to 3.6 V	-	8	-	50	μA
$I_{CC(B)}$	supply current B	V_I = 0 V or $V_{CC(A)}$; I_O = 0 A; $V_{CC(A)}$ = 0.8 V to 3.6 V; $V_{CC(B)}$ = 0.8 V to 3.6 V	-	8	-	50	μA

11. Dynamic characteristics

Table 9. Typical dynamic characteristics at $V_{CC(A)}$ = 0.8 V and T_{amb} = 25 °C

Voltages are referenced to GND (ground = 0 V); for test circuit, see Fig. 5; for waveforms, see Fig. 3 and Fig. 4.

Symbol [1]	Parameter	Conditions	$V_{CC(B)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
t_{pd}	propagation delay	A to Yn	29	16	15	15	14	14	ns
t_{dis}	disable time	$\overline{OE}$ to Yn	25	15	14	14	14	15	ns
t_{en}	enable time	$\overline{OE}$ to Yn	33	18	16	16	15	15	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL};
t_{dis} is the same as t_{PLZ} and t_{PHZ};
t_{en} is the same as t_{PZL} and t_{PZH}.

Table 10. Typical dynamic characteristics at $V_{CC(B)}$ = 0.8 V and T_{amb} = 25 °C

Voltages are referenced to GND (ground = 0 V); for test circuit, see Fig. 5; for waveforms, see Fig. 3 and Fig. 4.

Symbol [1]	Parameter	Conditions	$V_{CC(A)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
t_{pd}	propagation delay	A to Yn	29	20	20	19	19	18	ns
t_{dis}	disable time	$\overline{OE}$ to Yn	25	17	16	16	15	15	ns
t_{en}	enable time	$\overline{OE}$ to Yn	33	24	23	23	22	22	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL};
t_{dis} is the same as t_{PLZ} and t_{PHZ};
t_{en} is the same as t_{PZL} and t_{PZH}.

Table 11. Dynamic characteristics for temperature range -40 °C to +85 °C

Voltages are referenced to GND (ground = 0 V); for test circuit, see Fig. 5; for waveforms, see Fig. 3 and Fig. 4.

Symbol [1]	Parameter	Conditions	$V_{CC(B)}$										Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 1.1 V to 1.3 V													
t_{pd}	propagation delay	A to Yn	0.9	14.7	0.8	11.2	0.7	9.9	0.6	8.8	0.6	8.5	ns
t_{dis}	disable time	$\overline{OE}$ to Yn	1.0	14.7	0.9	12.2	0.9	12.1	0.8	10.8	1.0	11.7	ns
t_{en}	enable time	$\overline{OE}$ to Yn	1.0	15.8	0.8	11.8	0.8	10.3	0.7	8.9	0.7	8.5	ns
$V_{CC(A)}$ = 1.4 V to 1.6 V													
t_{pd}	propagation delay	A to Yn	0.8	13.2	0.7	9.5	0.6	8.2	0.5	6.7	0.5	6.2	ns
t_{dis}	disable time	$\overline{OE}$ to Yn	0.9	12.4	0.8	9.7	0.8	9.7	0.7	8.3	0.9	9.0	ns
t_{en}	enable time	$\overline{OE}$ to Yn	0.9	14.0	0.7	9.9	0.7	8.5	0.6	6.9	0.6	6.2	ns
$V_{CC(A)}$ = 1.65 V to 1.95 V													
t_{pd}	propagation delay	A to Yn	0.8	12.5	0.7	8.9	0.6	7.6	0.5	6.1	0.5	5.4	ns
t_{dis}	disable time	$\overline{OE}$ to Yn	0.9	11.7	0.8	9.0	0.8	8.8	0.7	7.4	0.8	8.2	ns
t_{en}	enable time	$\overline{OE}$ to Yn	0.9	13.5	0.7	9.3	0.6	7.9	0.6	6.3	0.5	5.6	ns
$V_{CC(A)}$ = 2.3 V to 2.7 V													
t_{pd}	propagation delay	A to Yn	0.8	12.0	0.6	8.3	0.6	6.9	0.5	5.4	0.4	4.7	ns
t_{dis}	disable time	$\overline{OE}$ to Yn	0.9	11.0	0.7	8.3	0.8	8.0	0.6	6.5	0.8	7.2	ns
t_{en}	enable time	$\overline{OE}$ to Yn	0.8	12.8	0.7	8.7	0.6	7.3	0.5	5.5	0.5	4.8	ns
$V_{CC(A)}$ = 3.0 V to 3.6 V													
t_{pd}	propagation delay	A to Yn	0.8	11.6	0.6	8.0	0.5	6.5	0.5	5.1	0.4	4.4	ns
t_{dis}	disable time	$\overline{OE}$ to Yn	0.9	10.8	0.7	8.0	0.7	7.7	0.6	6.2	0.7	6.9	ns
t_{en}	enable time	$\overline{OE}$ to Yn	0.8	12.5	0.6	8.4	0.6	6.9	0.5	5.2	0.5	4.5	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL};
t_{dis} is the same as t_{PLZ} and t_{PHZ};
t_{en} is the same as t_{PZL} and t_{PZH}.

Table 12. Dynamic characteristics for temperature range -40 °C to +125 °C

Voltages are referenced to GND (ground = 0 V); for test circuit, see Fig. 5; for waveforms, see Fig. 3 and Fig. 4.

Symbol [1]	Parameter	Conditions	$V_{CC(B)}$										Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 1.1 V to 1.3 V													
t_{pd}	propagation delay	A to Yn	0.9	15.7	0.8	12.1	0.7	10.8	0.6	9.7	0.6	9.3	ns
t_{dis}	disable time	$\overline{OE}$ to Yn	1.0	16.5	0.9	13.8	0.9	13.7	0.8	12.3	1.0	13.1	ns
t_{en}	enable time	$\overline{OE}$ to Yn	1.0	16.9	0.8	12.9	0.8	11.4	0.7	9.7	0.7	9.2	ns
$V_{CC(A)}$ = 1.4 V to 1.6 V													
t_{pd}	propagation delay	A to Yn	0.8	14.1	0.7	10.4	0.6	9.0	0.5	7.3	0.5	6.8	ns
t_{dis}	disable time	$\overline{OE}$ to Yn	0.9	14.0	0.8	11.0	0.8	11.0	0.7	9.5	0.9	10.2	ns
t_{en}	enable time	$\overline{OE}$ to Yn	0.9	15.1	0.7	10.9	0.7	9.3	0.6	7.6	0.6	6.8	ns
$V_{CC(A)}$ = 1.65 V to 1.95 V													
t_{pd}	propagation delay	A to Yn	0.8	13.6	0.7	9.7	0.6	8.3	0.5	6.7	0.5	6.0	ns
t_{dis}	disable time	$\overline{OE}$ to Yn	0.9	13.4	0.8	10.2	0.8	10.0	0.7	8.4	0.8	9.2	ns
t_{en}	enable time	$\overline{OE}$ to Yn	0.9	14.5	0.7	10.2	0.6	8.7	0.6	6.9	0.5	6.2	ns
$V_{CC(A)}$ = 2.3 V to 2.7 V													
t_{pd}	propagation delay	A to Yn	0.8	12.9	0.6	9.1	0.6	7.6	0.5	5.9	0.4	5.2	ns
t_{dis}	disable time	$\overline{OE}$ to Yn	0.9	12.5	0.7	9.4	0.8	9.1	0.6	7.5	0.8	8.2	ns
t_{en}	enable time	$\overline{OE}$ to Yn	0.8	13.7	0.7	9.5	0.6	8.0	0.5	6.1	0.5	5.3	ns
$V_{CC(A)}$ = 3.0 V to 3.6 V													
t_{pd}	propagation delay	A to Yn	0.8	12.5	0.6	8.7	0.5	7.2	0.5	5.6	0.4	4.9	ns
t_{dis}	disable time	$\overline{OE}$ to Yn	0.9	12.1	0.7	9.1	0.7	8.8	0.6	7.1	0.7	7.7	ns
t_{en}	enable time	$\overline{OE}$ to Yn	0.8	13.4	0.6	9.2	0.6	7.6	0.5	5.7	0.5	4.9	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL};
t_{dis} is the same as t_{PLZ} and t_{PHZ};
t_{en} is the same as t_{PZL} and t_{PZH}.

Table 13. Dynamic characteristics for temperature range -40 °C to +85 °C and -40 °C to +125 °C

Voltages are referenced to GND (ground = 0 V); for test circuit, see Fig. 5.

Symbol	Parameter	Conditions	$V_{CC(A)} = V_{CC(B)}$					Unit
			1.2 V ± 0.1 V	1.5 V ± 0.1 V	1.8 V ± 0.15 V	2.5 V ± 0.2 V	3.3 V ± 0.3 V	
			Max	Max	Max	Max	Max	
T_{amb} = -40 °C to +85 °C								
$t_{sk(o)}$	output skew time	between any output	0.7	0.4	0.3	0.2	0.2	ns
T_{amb} = -40 °C to +125 °C								
$t_{sk(o)}$	output skew time	between any output	0.9	0.5	0.4	0.3	0.2	ns

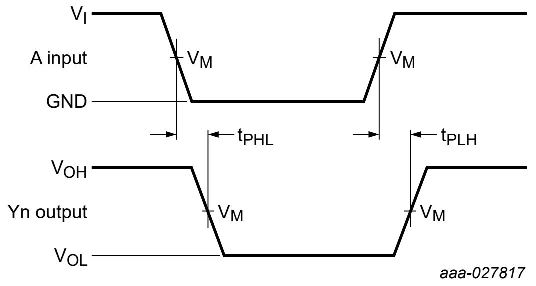
Table 14. Typical power dissipation capacitance at T_{amb} = 25 °C

Symbol [1] [2]	Parameter	Conditions	$V_{CC(A)} = V_{CC(B)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
C_{PD}	power dissipation capacitance	Yn; outputs enabled	36	36	37	37	41	46	pF
		Yn; outputs disabled	2.9	3.2	3.4	3.5	3.7	3.9	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = load capacitance in pF;
V_{CC} = supply voltage in V;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[2] f_i = 10 MHz;
V_I = GND to $V_{CC(A)}$;
$t_r = t_f$ = 1 ns;
C_L = 0 pF;
$R_L = \infty\ \Omega$.

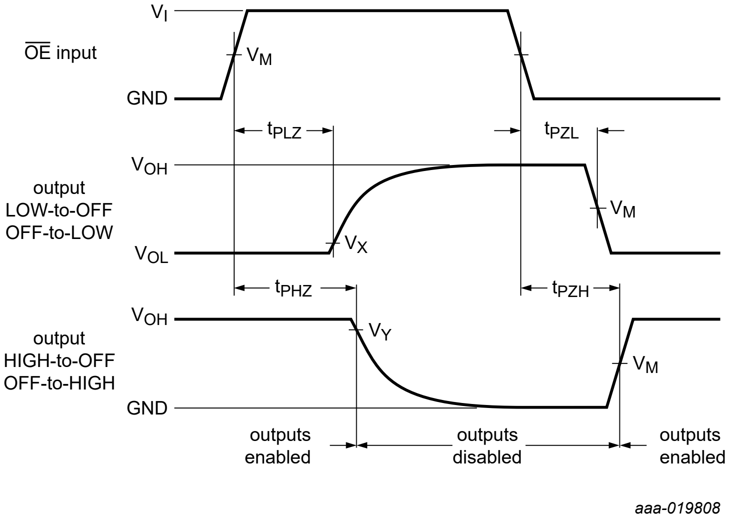
11.1. Waveforms and test circuit



Measurement points are given in Table 15.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 3. The data input (A) to output (Yn) propagation delay times



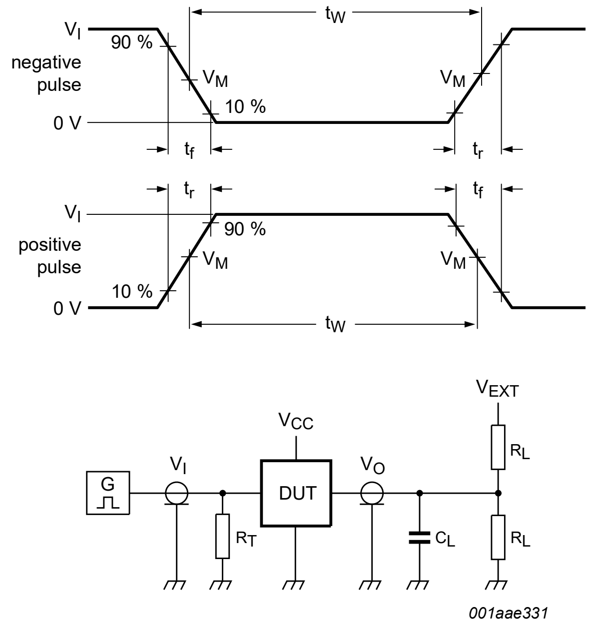
Measurement points are given in Table 15.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 4. Enable and disable times

Table 15. Measurement points

Supply voltage	Input	Output		
$V_{CC(A)}$, $V_{CC(B)}$	V_M	V_M	V_X	V_Y
0.8 V to 1.6 V	$0.5V_{CC(A)}$	$0.5V_{CC(B)}$	V_{OL} + 0.1 V	V_{OH} - 0.1 V
1.65 V to 2.7 V	$0.5V_{CC(A)}$	$0.5V_{CC(B)}$	V_{OL} + 0.15 V	V_{OH} - 0.15 V
3.0 V to 3.6 V	$0.5V_{CC(A)}$	$0.5V_{CC(B)}$	V_{OL} + 0.3 V	V_{OH} - 0.3 V



Test data is given in Table 16

Definitions test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance.

V_{EXT} = External voltage for measuring switching times.

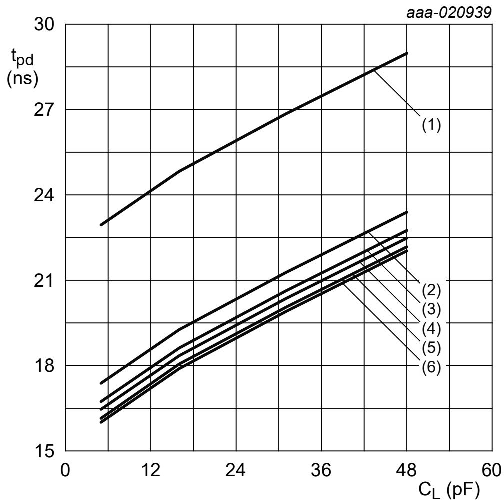
Fig. 5. Test circuit for measuring switching times

Table 16. Test data

Supply voltage	Input		Load		V_{EXT}		
$V_{CC(A)}$, $V_{CC(B)}$	V_I	Δt/ΔV [1]	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
0.8 V to 1.6 V	$V_{CC(A)}$	≤ 1.0 ns/V	15 pF	2 kΩ	open	GND	$2V_{CC(B)}$
1.65 V to 2.7 V	$V_{CC(A)}$	≤ 1.0 ns/V	15 pF	2 kΩ	open	GND	$2V_{CC(B)}$
3.0 V to 3.6 V	$V_{CC(A)}$	≤ 1.0 ns/V	15 pF	2 kΩ	open	GND	$2V_{CC(B)}$

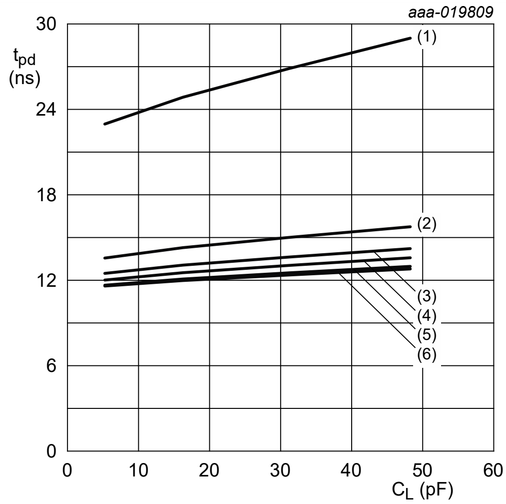
[1] dV/dt ≥ 1.0 V/ns

11.2. Typical propagation delay characteristics



a. Propagation delay (A to Yn); $V_{CC(B)}$ = 0.8 V

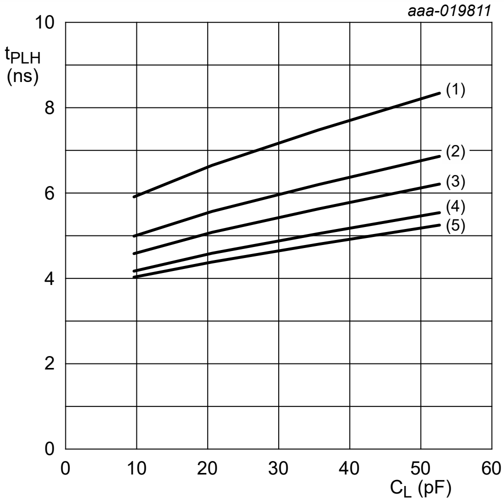
(1) $V_{CC(A)}$ = 0.8 V
(2) $V_{CC(A)}$ = 1.2 V
(3) $V_{CC(A)}$ = 1.5 V
(4) $V_{CC(A)}$ = 1.8 V
(5) $V_{CC(A)}$ = 2.5 V
(6) $V_{CC(A)}$ = 3.3 V



b. Propagation delay (A to Yn); $V_{CC(A)}$ = 0.8 V

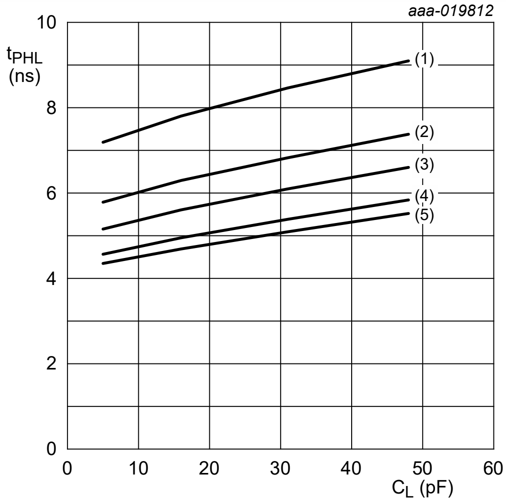
(1) $V_{CC(B)}$ = 0.8 V
(2) $V_{CC(B)}$ = 1.2 V
(3) $V_{CC(B)}$ = 1.5 V
(4) $V_{CC(B)}$ = 1.8 V
(5) $V_{CC(B)}$ = 2.5 V
(6) $V_{CC(B)}$ = 3.3 V

Fig. 6. Typical propagation delay versus load capacitance; T_{amb} = 25 °C



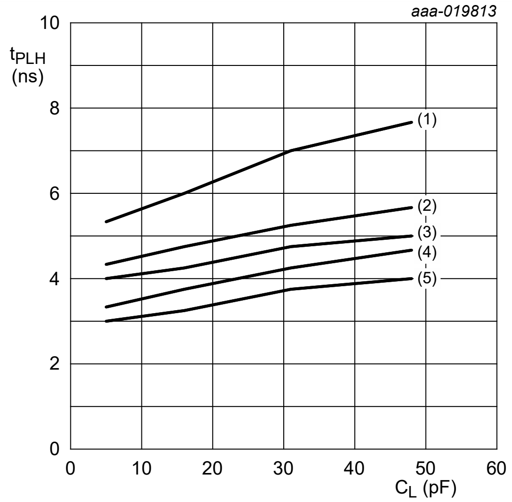
a. LOW to HIGH propagation delay (A to Yn); $V_{CC(A)}$ = 1.2 V

(1) $V_{CC(B)}$ = 1.2 V
(2) $V_{CC(B)}$ = 1.5 V
(3) $V_{CC(B)}$ = 1.8 V
(4) $V_{CC(B)}$ = 2.5 V
(5) $V_{CC(B)}$ = 3.3 V

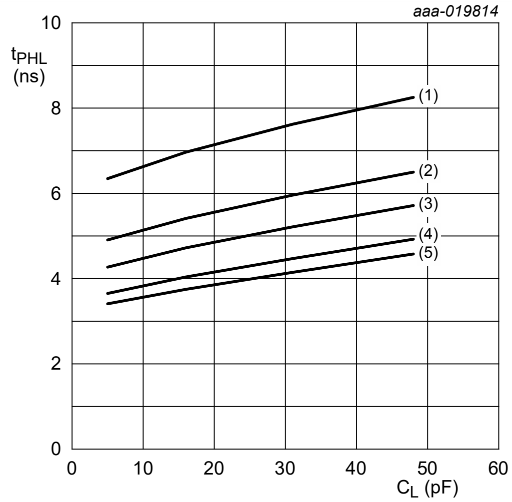


b. HIGH to LOW propagation delay (A to Yn); $V_{CC(A)}$ = 1.2 V

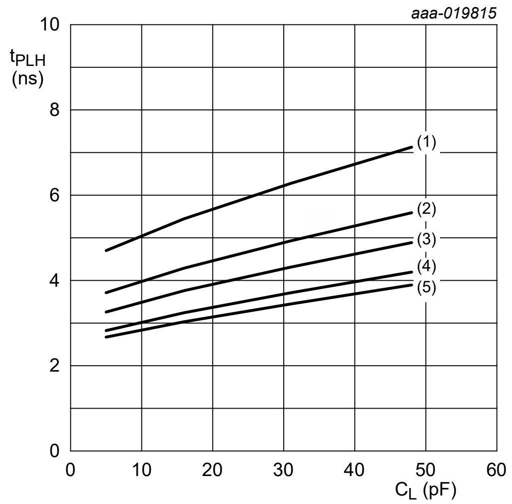
Fig. 7. Typical propagation delay versus load capacitance; T_{amb} = 25 °C



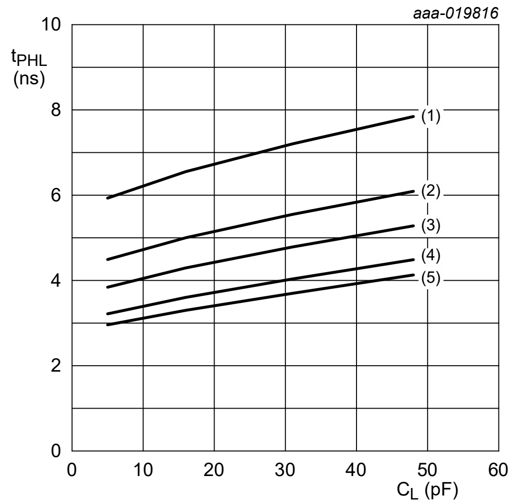
a. LOW to HIGH propagation delay (A to Yn); $V_{CC(A)}$ = 1.5 V



b. HIGH to LOW propagation delay (A to Yn); $V_{CC(A)}$ = 1.5 V



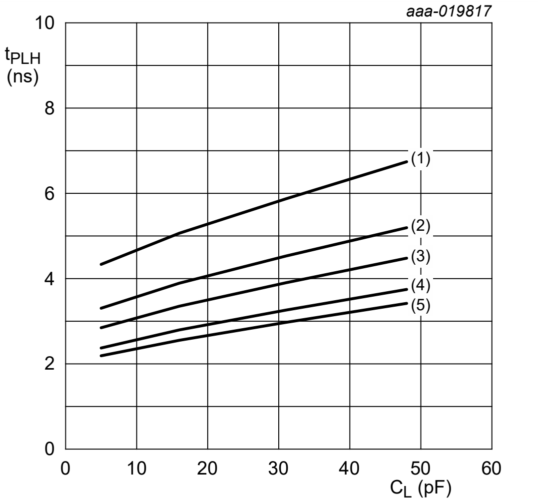
c. LOW to HIGH propagation delay (A to Yn); $V_{CC(A)}$ = 1.8 V



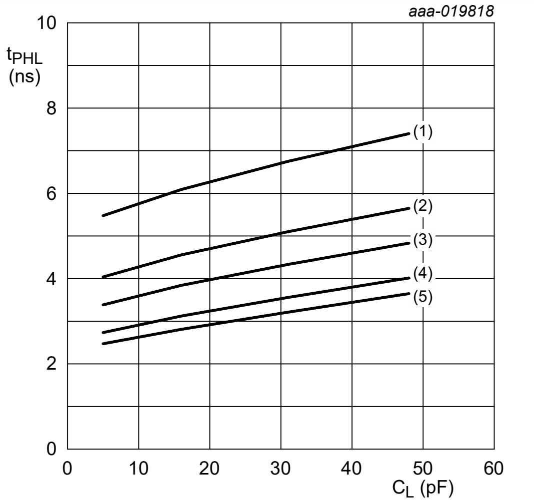
d. HIGH to LOW propagation delay (A to Yn); $V_{CC(A)}$ = 1.8 V

(1) $V_{CC(B)}$ = 1.2 V
(2) $V_{CC(B)}$ = 1.5 V
(3) $V_{CC(B)}$ = 1.8 V
(4) $V_{CC(B)}$ = 2.5 V
(5) $V_{CC(B)}$ = 3.3 V

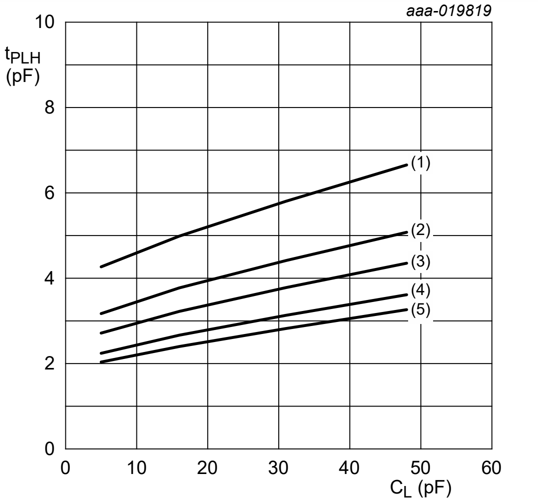
Fig. 8. Typical propagation delay versus load capacitance; T_{amb} = 25 °C



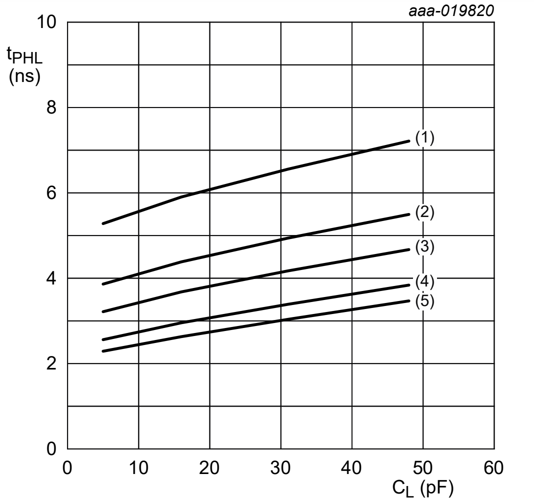
a. LOW to HIGH propagation delay (A to Yn); $V_{CC(A)}$ = 2.5 V



b. HIGH to LOW propagation delay (A to Yn); $V_{CC(A)}$ = 2.5 V



c. LOW to HIGH propagation delay (A to Yn); $V_{CC(A)}$ = 3.3 V



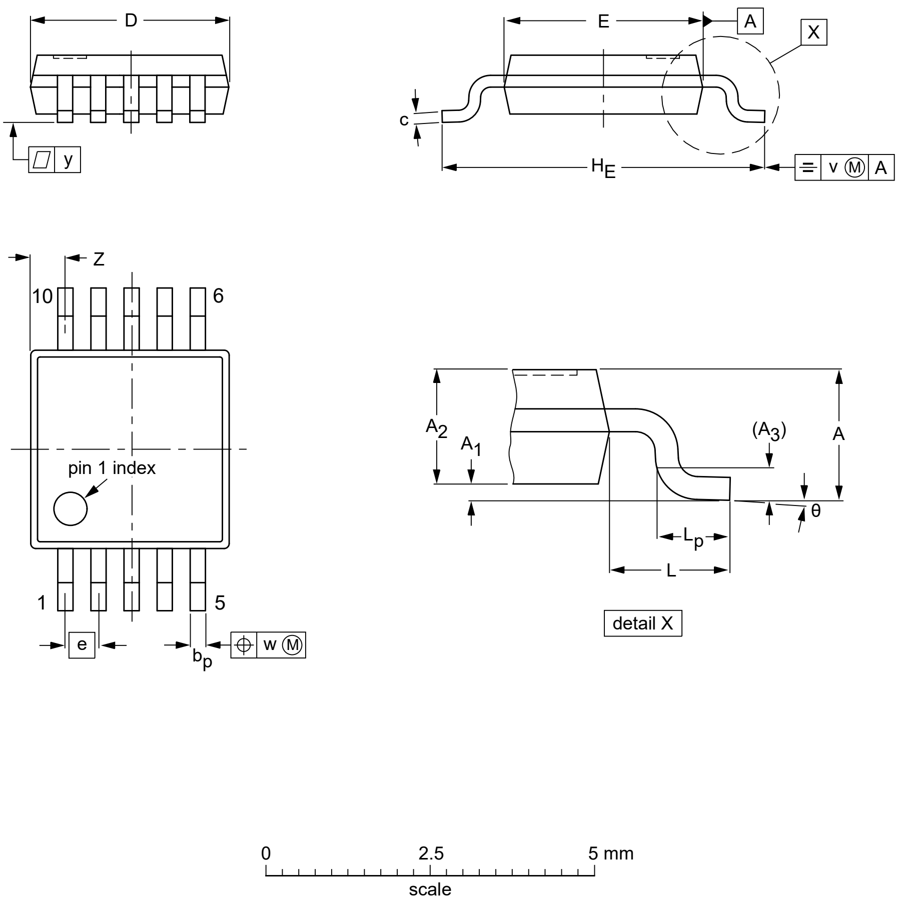
d. HIGH to LOW propagation delay (A to Yn); $V_{CC(A)}$ = 3.3 V

(1) $V_{CC(B)}$ = 1.2 V
(2) $V_{CC(B)}$ = 1.5 V
(3) $V_{CC(B)}$ = 1.8 V
(4) $V_{CC(B)}$ = 2.5 V
(5) $V_{CC(B)}$ = 3.3 V

Fig. 9. Typical propagation delay versus load capacitance; T_{amb} = 25 °C

12. Package outline

TSSOP10: plastic thin shrink small outline package; 10 leads; body width 3 mm **SOT552-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.15	0.23 0.15	3.1 2.9	3.1 2.9	0.5	5.0 4.8	0.95	0.7 0.4	0.1	0.1	0.1	0.67 0.34	6° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT552-1						~~99-07-29~~ 03-02-18

Fig. 10. Package outline SOT552-1 (TSSOP10)

13. Abbreviations

Table 17. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council

14. Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AVC1T1004 v.3	20240625	Product data sheet	-	74AVC1T1004 v.2
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard.			
74AVC1T1004 v.2	20210301	Product data sheet	-	74AVC1T1004 v.1
Modifications:	• Type number 74AVC1T1004GU33 (SOT1430-1) removed. • Section 8: Derating values for P_{tot} total power dissipation updated.			
74AVC1T1004 v.1	20180423	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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