Low-power dual function gate Rev. 12 – 28 July 2023

1. General description

The 74AUP1G885 is a dual function gate. The output state of the outputs (1Y, 2Y) is determined by the inputs (A, B and C). The output 1Y provides the Boolean function: $1Y = A \times C$. The output 2Y provides the Boolean function: $2Y = \overline{A} \times B + A \times \overline{C}$.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device ensures very low static and dynamic power consumption across the entire V_{CC} range from 0.8 V to 3.6 V.

This device is fully specified for partial power down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 0.8 V to 3.6 V
- CMOS low power dissipation
- High noise immunity
- Low static power consumption; I_{CC} = 0.9 μA (maximum)
- Overvoltage tolerant inputs to 3.6 V
- Low noise overshoot and undershoot < 10 % of V_{CC}
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 100 mA per JESD78 Class II
- Complies with JEDEC standards:
 - JESD8-12 (0.8 V to 1.3 V)
 - JESD8-11 (0.9 V to 1.65 V)
 - JESD8-7 (1.2 V to 1.95 V)
 - JESD8-5 (1.8 V to 2.7 V)
 - JESD8-B (2.7 V to 3.6 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 3A exceeds 5000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

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3. Ordering information

Table 1. Ordering information

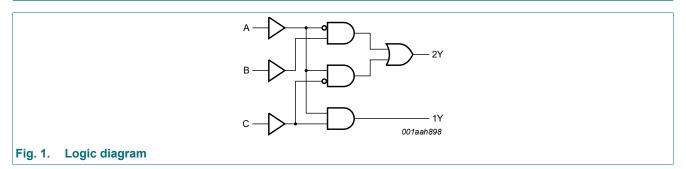
Type number	Package	Package									
	Temperature range	Name	Description	Version							
74AUP1G885DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	<u>SOT765-1</u>							
74AUP1G885GT	-40 °C to +125 °C	XSON8	 plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm 								
74AUP1G885GF	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 × 1 × 0.5 mm	<u>SOT1089</u>							
74AUP1G885GN	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.2 × 1.0 × 0.35 mm	<u>SOT1116</u>							
74AUP1G885GS	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 × 1.0 × 0.35 mm	<u>SOT1203</u>							

4. Marking

Table 2. Marking codes							
Type number	Marking code [1]						
74AUP1G885DC	pS8						
74AUP1G885GT	pS8						
74AUP1G885GF	58						
74AUP1G885GN	58						
74AUP1G885GS	58						

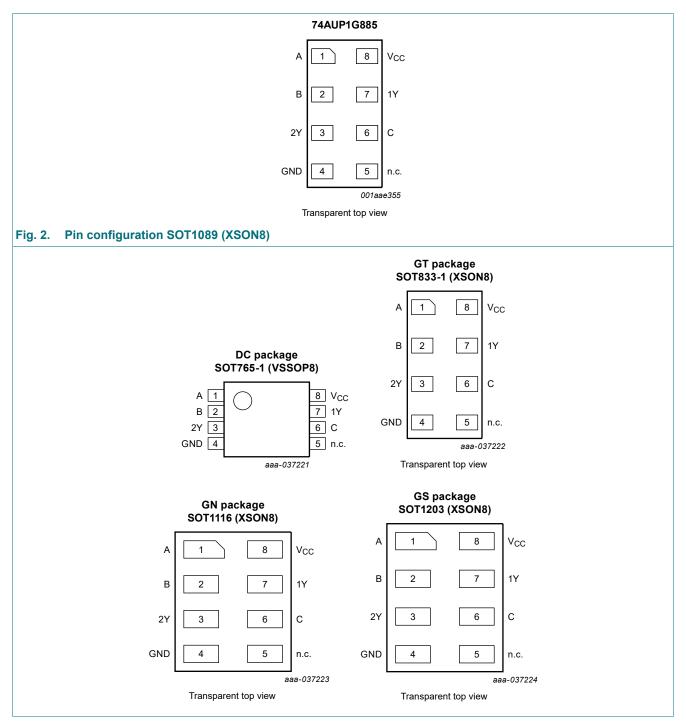
[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram



6. Pinning information





6.2. Pin description

Table 3. Pin description							
Symbol	Pin	Description					
A, B, C	1, 2, 6	data input					
GND	4	ground (0 V)					
n.c.	5	not connected					
1Y, 2Y	7, 3	data output					
V _{CC}	8	supply voltage					

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level.

Input		Output		
Α	В	С	1Y	2Y
L	L	L	L	L
Н	L	L	L	Н
L	Н	L	L	Н
Н	Н	L	L	Н
L	L	Н	L	L
Н	L	Н	Н	L
L	Н	Н	L	Н
Н	Н	Н	Н	L

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Мах	Unit
V _{CC}	supply voltage		-0.5	+4.6	V
I _{IK}	input clamping current	V ₁ < 0 V	-50	-	mA
VI	input voltage	[1]	-0.5	+4.6	V
Ι _{ΟΚ}	output clamping current	V _O < 0 V	-50	-	mA
Vo	output voltage	Active mode and Power-down mode [1]	-0.5	+4.6	V
lo	output current	$V_{O} = 0 V \text{ to } V_{CC}$	-	±20	mA
I _{CC}	supply current		-	50	mA
I _{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C [2]	-	250	mW

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT765-1 (VSSOP8) package: P_{tot} derates linearly with 4.9 mW/K above 99 °C.

For SOT833-1 (XSON8) package: P_{tot} derates linearly with 3.1 mW/K above 68 °C.

For SOT1089 (XSON8) package: Ptot derates linearly with 4.0 mW/K above 88 °C.

For SOT1116 (XSON8) package: P_{tot} derates linearly with 4.2 mW/K above 90 °C.

For SOT1203 (XSON8) package: P_{tot} derates linearly with 3.6 mW/K above 81 °C.

74AUP1G885

9. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		0.8	3.6	V
VI	input voltage		0	3.6	V
Vo	output voltage	Active mode	0	V _{CC}	V
		Power-down mode; V _{CC} = 0 V	0	3.6	V
T _{amb}	ambient temperature		-40	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 0.8 V to 3.6 V	-	200	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
T _{amb} = 2	5 °C					
VIH	HIGH-level input voltage	V _{CC} = 0.8 V	0.70V _{CC}	-	-	V
		V _{CC} = 0.9 V to 1.95 V	0.65V _{CC}	-	-	V
		V _{CC} = 2.3 V to 2.7 V	1.6	-	-	V
		V _{CC} = 3.0 V to 3.6 V	2.0	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 0.8 V	-	-	0.30V _{CC}	V
		V _{CC} = 0.9 V to 1.95 V	-	-	0.35V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 3.0 V to 3.6 V	-	-	0.9	V
V _{OH}	HIGH-level output	$V_{I} = V_{IH} \text{ or } V_{IL}$				
	voltage	I_{O} = -20 µA; V_{CC} = 0.8 V to 3.6 V	V _{CC} - 0.1	-	-	V
		I _O = -1.1 mA; V _{CC} = 1.1 V	0.75V _{CC}	-	-	V
		I _O = -1.7 mA; V _{CC} = 1.4 V	1.11	-	-	V
		I _O = -1.9 mA; V _{CC} = 1.65 V	1.32	-	-	V
		I _O = -2.3 mA; V _{CC} = 2.3 V	2.05	-	-	V
		I _O = -3.1 mA; V _{CC} = 2.3 V	1.9	-	-	V
		I _O = -2.7 mA; V _{CC} = 3.0 V	2.72	-	-	V
		I _O = -4.0 mA; V _{CC} = 3.0 V	2.6	-	-	V
V _{OL}	LOW-level output voltage	$V_{I} = V_{IH} \text{ or } V_{IL}$				
		I_{O} = 20 µA; V_{CC} = 0.8 V to 3.6 V	-	-	0.1	V
		I _O = 1.1 mA; V _{CC} = 1.1 V	-	-	0.3V _{CC}	V
		I _O = 1.7 mA; V _{CC} = 1.4 V	-	-	0.31	V
		I _O = 1.9 mA; V _{CC} = 1.65 V	-	-	0.31	V
		I _O = 2.3 mA; V _{CC} = 2.3 V	-	-	0.31	V
		I _O = 3.1 mA; V _{CC} = 2.3 V	-	-	0.44	V
		I _O = 2.7 mA; V _{CC} = 3.0 V	-	-	0.31	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.44	V

Low-power dual function gate

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
I _I	input leakage current	V_I = GND to 3.6 V; V_{CC} = 0 V to 3.6 V	-	-	±0.1	μA
I _{OFF}	power-off leakage current	V_{I} or V_{O} = 0 V to 3.6 V; V_{CC} = 0 V	-	-	±0.2	μA
ΔI _{OFF}	additional power-off leakage current	$V_1 \text{ or } V_0 = 0 \text{ V to } 3.6 \text{ V}; V_{CC} = 0 \text{ V to } 0.2 \text{ V}$	-	-	±0.2	μA
I _{CC}	supply current	V _I = GND or V _{CC} ; I _O = 0 A; V _{CC} = 0.8 V to 3.6 V	-	-	0.5	μA
ΔI _{CC}	additional supply current	$V_{I} = V_{CC} - 0.6 V; I_{O} = 0 A; V_{CC} = 3.3 V$ [1]	-	-	40	μA
CI	input capacitance	V_{CC} = 0 V to 3.6 V; V _I = GND or V _{CC}	-	0.6	-	pF
Co	output capacitance	$V_{O} = GND; V_{CC} = 0 V$	-	1.3	-	pF
T _{amb} = -4	40 °C to +85 °C			I		-
V _{IH}	HIGH-level input voltage	V _{CC} = 0.8 V	0.70V _{CC}	-	-	V
		V _{CC} = 0.9 V to 1.95 V	0.65V _{CC}	-	-	V
		V _{CC} = 2.3 V to 2.7 V	1.6	-	-	V
		V _{CC} = 3.0 V to 3.6 V	2.0	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 0.8 V	-	-	0.30V _{CC}	V
		V _{CC} = 0.9 V to 1.95 V	-	-	0.35V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 3.0 V to 3.6 V	-	-	0.9	V
V _{OH}	HIGH-level output	V _I = V _{IH} or V _{IL}				
	voltage	I _O = -20 μA; V _{CC} = 0.8 V to 3.6 V	V _{CC} - 0.1	-	-	V
		I _O = -1.1 mA; V _{CC} = 1.1 V	0.7V _{CC}	-	-	V
		I _O = -1.7 mA; V _{CC} = 1.4 V	1.03	-	-	V
		I _O = -1.9 mA; V _{CC} = 1.65 V	1.30	-	-	V
		I _O = -2.3 mA; V _{CC} = 2.3 V	1.97	-	-	V
		I _O = -3.1 mA; V _{CC} = 2.3 V	1.85	-	-	V
		$I_0 = -2.7 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.67	-	-	V
		$I_0 = -4.0 \text{ mA; } V_{CC} = 3.0 \text{ V}$	2.55	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				-
01		$I_{O} = 20 \ \mu A; V_{CC} = 0.8 \ V \ to \ 3.6 \ V$	-	-	0.1	V
		$I_0 = 1.1 \text{ mA}; V_{CC} = 1.1 \text{ V}$	-	-	0.3V _{CC}	V
		$I_0 = 1.7 \text{ mA; } V_{CC} = 1.4 \text{ V}$	-	-	0.37	V
		I _O = 1.9 mA; V _{CC} = 1.65 V	-	-	0.35	V
		$I_0 = 2.3 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.33	V
		$I_0 = 3.1 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.45	V
		$I_0 = 2.7 \text{ mA}; V_{CC} = 3.0 \text{ V}$	_	-	0.33	V
		$I_0 = 4.0 \text{ mA; } V_{CC} = 3.0 \text{ V}$	_	-	0.45	V
I _I	input leakage current	$V_{I} = GND \text{ to } 3.6 \text{ V}; V_{CC} = 0 \text{ V to } 3.6 \text{ V}$	_	-	±0.5	μA
I _{OFF}	power-off leakage current		-	-	±0.5	μA
ΔI _{OFF}	additional power-off leakage current	$V_1 \text{ or } V_0 = 0 \text{ V to } 3.6 \text{ V}; V_{CC} = 0 \text{ V to } 0.2 \text{ V}$	-	-	±0.6	μA
I _{CC}	supply current	V _I = GND or V _{CC} ; I _O = 0 A; V _{CC} = 0.8 V to 3.6 V	-	-	0.9	μA
ΔI _{CC}	additional supply current	$V_1 = V_{CC} - 0.6 V; I_0 = 0 A; V_{CC} = 3.3 V$ [1]	-	_	50	μA

Low-power dual function gate

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
T _{amb} = -4	40 °C to +125 °C					
VIH	HIGH-level input voltage	V _{CC} = 0.8 V	0.75V _{CC}	-	-	V
		V _{CC} = 0.9 V to 1.95 V	0.70V _{CC}	-	-	V
		V _{CC} = 2.3 V to 2.7 V	1.6	-	-	V
		V _{CC} = 3.0 V to 3.6 V	2.0	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 0.8 V	-	-	0.25V _{CC}	V
		V _{CC} = 0.9 V to 1.95 V	-	-	0.30V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 3.0 V to 3.6 V	-	-	0.9	V
V _{OH}	HIGH-level output	V _I = V _{IH} or V _{IL}				
	voltage	I_{O} = -20 µA; V_{CC} = 0.8 V to 3.6 V	V _{CC} - 0.11	-	-	V
		I _O = -1.1 mA; V _{CC} = 1.1 V	0.6V _{CC}	-	-	V
		I _O = -1.7 mA; V _{CC} = 1.4 V	0.93	-	-	V
		I _O = -1.9 mA; V _{CC} = 1.65 V	1.17	-	-	V
		I _O = -2.3 mA; V _{CC} = 2.3 V	1.77	-	-	V
		I _O = -3.1 mA; V _{CC} = 2.3 V	1.67	-	-	V
		I _O = -2.7 mA; V _{CC} = 3.0 V	2.40	-	-	V
		I _O = -4.0 mA; V _{CC} = 3.0 V	2.30	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I_{O} = 20 µA; V_{CC} = 0.8 V to 3.6 V	-	-	0.11	V
		I _O = 1.1 mA; V _{CC} = 1.1 V	-	-	0.33V _{CC}	V
		I _O = 1.7 mA; V _{CC} = 1.4 V	-	-	0.41	V
		I _O = 1.9 mA; V _{CC} = 1.65 V	-	-	0.39	V
		I _O = 2.3 mA; V _{CC} = 2.3 V	-	-	0.36	V
		I _O = 3.1 mA; V _{CC} = 2.3 V	-	-	0.50	V
		I _O = 2.7 mA; V _{CC} = 3.0 V	-	-	0.36	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.50	V
I _I	input leakage current	$V_{I} = GND$ to 3.6 V; $V_{CC} = 0$ V to 3.6 V	-	-	±0.75	μA
I _{OFF}	power-off leakage current	V_{I} or V_{O} = 0 V to 3.6 V; V_{CC} = 0 V	-	-	±0.75	μA
ΔI _{OFF}	additional power-off leakage current	$V_1 \text{ or } V_0 = 0 \text{ V to } 3.6 \text{ V}; V_{CC} = 0 \text{ V to } 0.2 \text{ V}$	-	-	±0.75	μA
I _{CC}	supply current	V_1 = GND or V_{CC} ; I_0 = 0 A; V_{CC} = 0.8 V to 3.6 V	-	-	1.4	μA
ΔI _{CC}	additional supply current	$V_{I} = V_{CC} - 0.6 \text{ V}; I_{O} = 0 \text{ A}; V_{CC} = 3.3 \text{ V}$ [1]	-	-	75	μA

[1] One input at V_{CC} - 0.6 V, other inputs at V_{CC} or GND.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 4.

Symbol	Parameter	Conditions		25 °C		-	°C to 5 °C		°C to 5 °C	Unit
				Typ [1]	Мах	Min	Max	Min	Max	
C _L = 5 p	F									
t _{pd}	propagation	A, C to 1Y; see Fig. 3 [2]								
	delay	V _{CC} = 0.8 V	-	17.3	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	1.1	5.2	9.7	0.9	12.8	0.9	14.2	ns
		V _{CC} = 1.4 V to 1.6 V	1.2	3.7	5.9	1.0	7.8	1.0	8.6	ns
		V _{CC} = 1.65 V to 1.95 V	1.1	3.0	4.8	0.9	6.2	0.9	6.9	ns
		V _{CC} = 2.3 V to 2.7 V	1.1	2.4	3.6	1.0	4.1	1.0	4.5	ns
		V _{CC} = 3.0 V to 3.6 V	1.1	2.1	3.1	1.0	3.6	1.0	4.1	ns
		A, B to 2Y; see Fig. 3 [2]								
		V _{CC} = 0.8 V	-	21.5	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	1.7	6.0	12.7	1.4	12.8	1.4	14.2	ns
		V _{CC} = 1.4 V to 1.6 V	1.7	4.2	7.2	1.4	7.8	1.4	8.7	ns
		V _{CC} = 1.65 V to 1.95 V	1.4	3.3	5.8	1.2	6.5	1.2	7.2	ns
		V _{CC} = 2.3 V to 2.7 V	1.2	2.6	4.1	1.0	4.7	1.0	5.2	ns
		V _{CC} = 3.0 V to 3.6 V	1.1	2.3	3.5	0.9	3.8	0.9	4.2	ns
C _L = 10	pF	· · · · · · · · · · · · · · · · · · ·				1				1
t _{pd}	propagation	A, C to 1Y; see <u>Fig. 3</u> [2]								
	delay	V _{CC} = 0.8 V	-	20.8	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	1.2	6.1	11.4	1.2	14.6	1.2	16.1	ns
		V _{CC} = 1.4 V to 1.6 V	1.4	4.3	7.2	1.2	8.7	1.2	9.6	ns
		V _{CC} = 1.65 V to 1.95 V	1.4	3.6	5.7	1.3	6.8	1.3	7.5	ns
		V _{CC} = 2.3 V to 2.7 V	1.4	2.9	4.2	1.2	4.8	1.2	5.4	ns
		V _{CC} = 3.0 V to 3.6 V	1.4	2.7	3.9	1.3	4.1	1.3	4.6	ns
		A, B to 2Y; see Fig. 3 [2]								
		V _{CC} = 0.8 V	-	25.0	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	1.8	6.9	14.4	1.7	14.6	1.7	16.1	ns
		V _{CC} = 1.4 V to 1.6 V	1.9	4.8	8.5	1.5	9.1	1.5	10.1	ns
		V _{CC} = 1.65 V to 1.95 V	1.9	3.9	6.6	1.7	7.2	1.7	8.0	ns
		V_{CC} = 2.3 V to 2.7 V	1.5	3.1	4.7	1.3	5.4	1.3	5.9	ns
		V _{CC} = 3.0 V to 3.6 V	1.4	2.8	4.3	1.3	4.6	1.3	5.1	ns

Low-power dual function gate

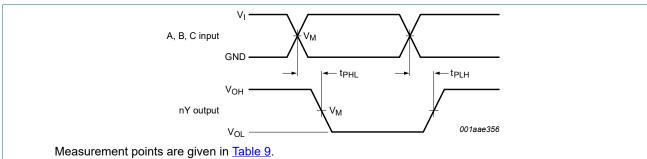
Symbol	Parameter Conditions			25 °C			°C to 5 °C	-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	Min	Max	-
C _L = 15	pF	-					1			
t _{pd}	propagation	A, C to 1Y; see <u>Fig. 3</u> [2]							
	delay	V _{CC} = 0.8 V	-	24.3	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	1.3	6.9	13.0	1.2	16.2	1.2	17.9	ns
		V _{CC} = 1.4 V to 1.6 V	1.7	4.9	8.0	1.4	9.7	1.4	10.8	ns
		V _{CC} = 1.65 V to 1.95 V	1.5	4.1	6.4	1.4	7.6	1.4	8.4	ns
		V_{CC} = 2.3 V to 2.7 V	1.7	3.4	5.0	1.6	5.4	1.6	6.0	ns
		V _{CC} = 3.0 V to 3.6 V	1.7	3.1	4.4	1.6	4.7	1.6	5.3	ns
		A, B to 2Y; see Fig. 3 [2]							
		V _{CC} = 0.8 V	-	28.5	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	2.1	7.7	16.0	1.9	16.3	1.9	18.0	ns
		V _{CC} = 1.4 V to 1.6 V	2.2	5.4	9.4	2.4	10.3	2.4	11.4	ns
		V _{CC} = 1.65 V to 1.95 V	2.0	4.4	7.4	1.8	8.2	1.8	9.1	ns
		V _{CC} = 2.3 V to 2.7 V	1.8	3.6	5.5	1.6	6.0	1.6	6.7	ns
		V _{CC} = 3.0 V to 3.6 V	1.7	3.3	4.8	1.5	5.2	1.5	5.8	ns
C _L = 30	pF	-	_			1	1			1
t _{pd}	propagation	A, C to 1Y; see <u>Fig. 3</u> [2]							
	delay	V _{CC} = 0.8 V	-	34.7	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	2.4	9.2	17.7	2.3	20.9	2.3	23.0	ns
		V _{CC} = 1.4 V to 1.6 V	2.5	6.5	10.6	2.5	12.2	2.5	13.5	ns
		V _{CC} = 1.65 V to 1.95 V	2.5	5.4	8.5	2.4	9.4	2.4	10.4	ns
		V_{CC} = 2.3 V to 2.7 V	2.6	4.5	6.4	2.4	7.0	2.4	7.7	ns
		V _{CC} = 3.0 V to 3.6 V	2.5	4.2	5.7	2.3	6.6	2.3	7.3	ns
		A, B to 2Y; see Fig. 3 [2]							
		V _{CC} = 0.8 V	-	38.9	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	2.6	10.0	20.5	2.6	21.5	2.6	23.7	ns
		V _{CC} = 1.4 V to 1.6 V	2.6	6.9	11.9	2.6	13.2	2.6	14.5	ns
		V _{CC} = 1.65 V to 1.95 V	2.7	5.7	9.5	2.7	10.5	2.7	11.6	ns
		V _{CC} = 2.3 V to 2.7 V	2.5	4.7	6.9	2.5	7.6	2.5	8.4	ns
		V _{CC} = 3.0 V to 3.6 V	2.4	4.4	6.1	2.4	7.1	2.4	7.9	ns
C _L = 5 p	F, 10 pF, 15 pF	and 30 pF	-	•						
C _{PD}	power	$f_i = 1 \text{ MHz}; V_I = \text{GND to } V_{CC}$ [3]							
	dissipation capacitance	V _{CC} = 0.8 V	-	2.7	-	-	-	-	-	pF
	Capacitance	V _{CC} = 1.1 V to 1.3 V	-	2.9	-	-	-	-	-	pF
		V _{CC} = 1.4 V to 1.6 V	-	3.0	-	-	-	-	-	pF
		V _{CC} = 1.65 V to 1.95 V	-	3.1	-	-	-	-	-	pF
		V _{CC} = 2.3 V to 2.7 V	-	3.5	-	-	-	-	-	pF
		V _{CC} = 3.0 V to 3.6 V	_	4.1	-	-	_	-	-	pF

[1] All typical values are measured at nominal $V_{\mbox{\scriptsize CC}}.$

[2] [3]

 t_{pd} is the same as t_{PLH} and t_{PHL} . C_{PD} is used to determine the dynamic power dissipation (P_D in μ W). $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where: f_i = input frequency in MHz; f_o = output frequency in MHz; C_L = output load capacitance in pF;

 V_{CC} = supply voltage in V; N = number of inputs switching; $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.



11.1. Waveforms and test circuit

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 3. The data input (A, B, C) to output (nY) propagation delays

Table 9. Measurement points

Supply voltage	Output	Input				
V _{cc}	V _M	V_M V_l $t_r = t_f$				
0.8 V to 3.6 V	0.5 × V _{CC}	0.5 × V _{CC}	V _{CC}	≤ 3.0 ns		

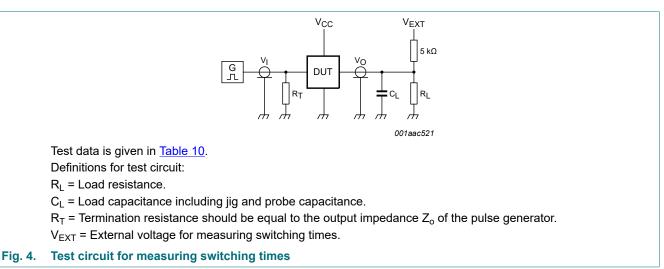


Table 10. Test data

Supply voltage	Load	V _{EXT}			
V _{cc}	CL	R _L [1]	t _{PLH} , t _{PHL}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ}
0.8 V to 3.6 V	5 pF, 10 pF, 15 pF and 30 pF	5 kΩ or 1 MΩ	open	GND	$2 \times V_{CC}$

[1] For measuring enable and disable times $R_L = 5 k\Omega$. For measuring propagation delays, set-up and hold times and pulse width $R_L = 1 M\Omega$.

12. Package outline

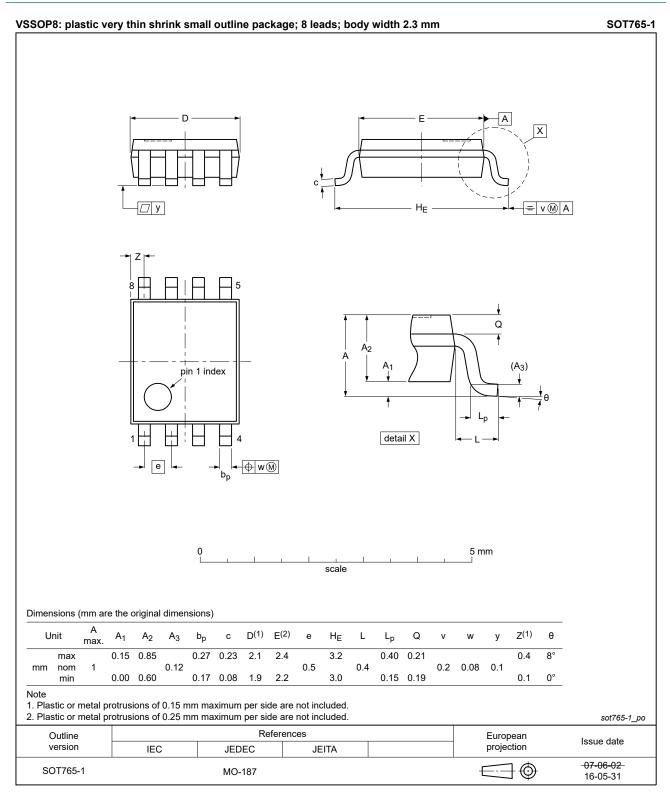


Fig. 5. Package outline SOT765-1 (VSSOP8)

Low-power dual function gate

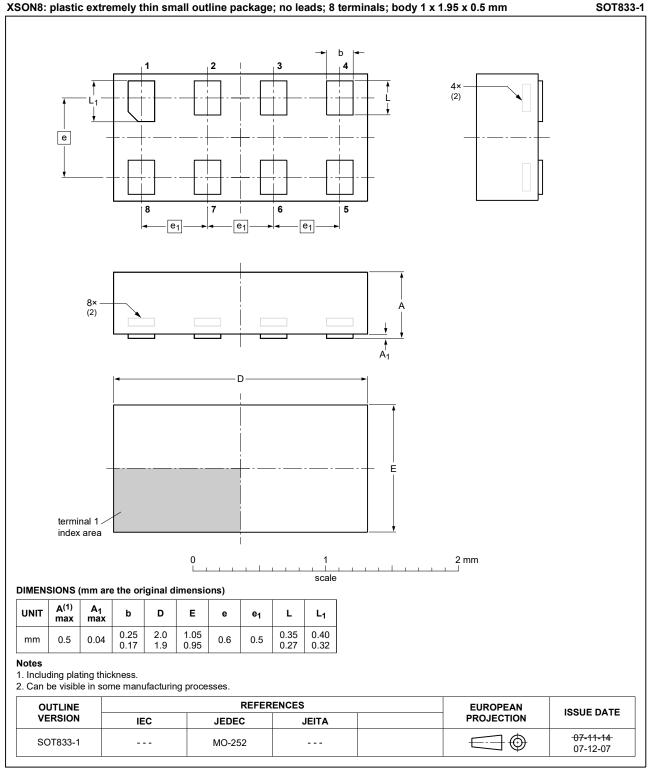
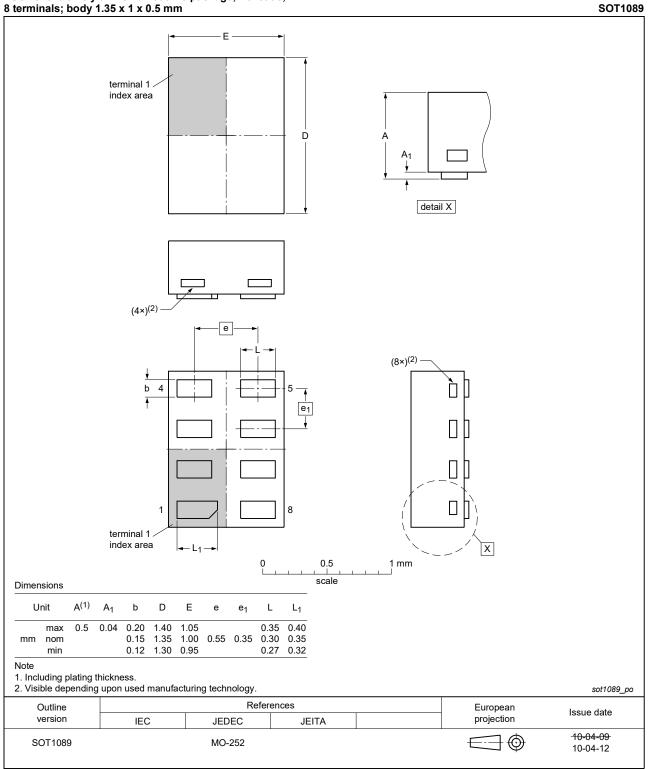


Fig. 6. Package outline SOT833-1 (XSON8)

Low-power dual function gate

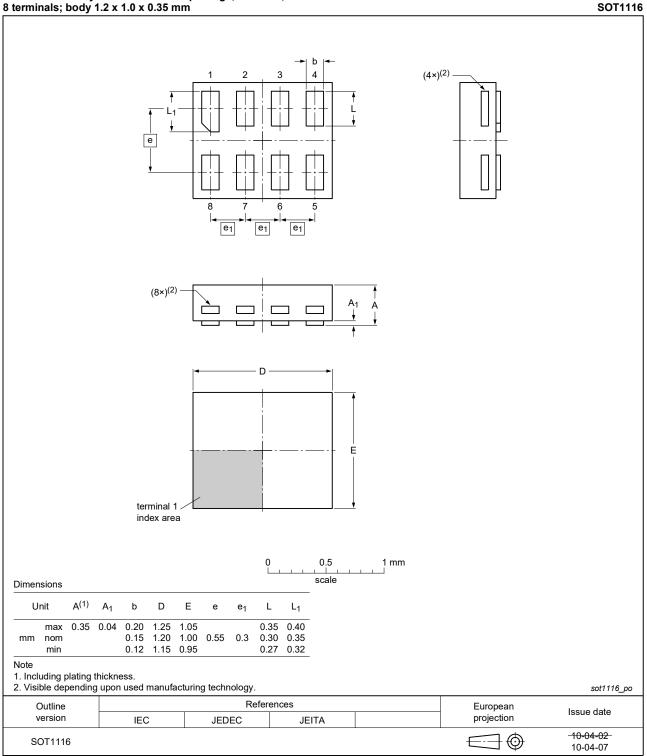


XSON8: extremely thin small outline package; no leads; 8 terminals; body 1.35 x 1 x 0.5 mm

Fig. 7. Package outline SOT1089 (XSON8)

Low-power dual function gate

XSON8: extremely thin small outline package; no leads; 8 terminals; body 1.2 x 1.0 x 0.35 mm





XSON8: extremely thin small outline package; no leads;

74AUP1G885

Low-power dual function gate

8 terminals; body 1.35 x 1.0 x 0.35 mm SOT1203 b (4×)⁽²⁾ 4 3 2 е 8 6 5 e₁e₁ e₁ $(8 \times)^{(2)}$ А С С ٦ D E terminal 1 index area 0.5 1 mm 0 1 1 1 scale Dimensions Unit A⁽¹⁾ A₁ b D Е L е e₁ L_1 0.35 0.04 0.20 1.40 1.05 0.35 0.40 max 0.15 1.00 0.55 0.35 0.30 0.35mm nom 1.35 min 0.12 1.30 0.95 0.27 0.32 Note 1. Including plating thickness. 2. Visible depending upon used manufacturing technology. sot1203_po References Outline European Issue date version projection IEC JEDEC JEITA 10-04-02 SOT1203 \blacksquare 10-04-06



13. Abbreviations

Table 11. Abbreviations			
Acronym	Description		
CDM	Charged Device Model		
CMOS	Complementary Metal-Oxide Semiconductor		
DUT	Device Under Test		
ESD	ElectroStatic Discharge		
НВМ	Human Body Model		

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes		
74AUP1G885 v.12	20230728	Product data sheet	-	74AUP1G885 v.11		
Modifications:	• <u>Section 2</u> : E	• <u>Section 2</u> : ESD specification updated according to the latest JEDEC standard.				
74AUP1G885 v.11	20190722	Product data sheet	-	74AUP1G885 v.10		
Modifications:	••	 Type number 74AUP1G885GM (SOT902-2) removed. Layout of <u>Table 8</u> Dynamic characteristics updated. 				
74AUP1G885 v.10	20190314	Product data sheet	-	74AUP1G885 v.9		
Modifications:	of Nexperia. Legal texts l Type numbe Package ou	 Type number 74AUP16885GD (SOT996-2) removed. 				
74AUP1G885 v.9	20130131	Product data sheet	-	74AUP1G885 v.8		
Modifications:	 For type nur 	For type number 74AUP1G885GD XSON8U has changed to XSON8.				
74AUP1G885 v.8	20120608	Product data sheet	-	74AUP1G885 v.7		
74AUP1G885 v.7	20111129	Product data sheet	-	74AUP1G885 v.6		
74AUP1G885 v.6	20101021	Product data sheet	-	74AUP1G885 v.5		
74AUP1G885 v.5	20090626	Product data sheet	-	74AUP1G885 v.4		
74AUP1G885 v.4	20090401	Product data sheet	-	74AUP1G885 v.3		
74AUP1G885 v.3	20080328	Product data sheet	-	74AUP1G885 v.2		
74AUP1G885 v.2	20070710	Product data sheet	-	74AUP1G885 v.1		
74AUP1G885 v.1	20061201	Product data sheet				

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

 Please consult the most recently issued document before initiating or completing a design.

- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <u>https://www.nexperia.com</u>.

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